HETEROGENEOUS INTEGRATION ROADMAP

2024 Edition

Chapter 22: Interconnects for 2D and 3D Architectures

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Chapter 22: Interconnects for 2D and 3D Architectures

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Executive Summary

With increasing interest in on-package Heterogeneous Integration (HI), there is a need to describe package architectures and their interconnect capabilities in a simple and consistent manner. This chapter has two primary objectives: to (a) define and proliferate a standardized nomenclature for package architectures covering and clearly demarcating both 2D and 3D[1] constructions and to (b) define and proliferate key metrics driving the evolution of the physical interconnects in these architectures.

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1. Introduction

Moore's Law has paced the growth of the microelectronics industry for the last 50 years by providing a template for silicon scaling and homogeneous SoC (**S**ystem **o**n a **C**hip) integration of different IP (Intellectual Property) circuits. Moving forward, HI, enabled by changes in the physical, electrical, thermal, and thermo-mechanical attributes of packages and micro-systems, increasingly complements Moore's Law to provide improved functionality [1-7]. Current and new advanced package architectures are major enablers in sustaining and enhancing growth in the micro-electronics industry [8-22]. These architectures enable novel heterogeneous SiP (**S**ystem **i**n **P**ackage) configurations for cost-performance optimized micro-electronics systems. A number of products that use advanced HI have been announced in recent years attesting to the importance of this field [23-28].

Historically, the primary purpose of the package for homogenous integration was to provide mechanical protection for the die, space transformation for silicon features, form factor scaling, low parasitic power-delivery, efficient power removal and low loss, high bandwidth signaling. Innovations in packaging for homogeneous SoCs, focused on enabling silicon size scaling, power, performance, and latency while maximizing performance opportunities made possible by Moore's Law. During the period where the primary focus was homogeneous integration, MCPs (**M**ulti-**C**hip **P**ackages) were used primarily for improved time-to-market and for critical HI needs (e.g., DRAM integration) [29].

[1] Scope of this chapter is restricted to electrical interconnects between one or more semiconductor devices.

Industry trends today show an increasing need for HI driven by a need to add diverse functionality (often realized with different IP on silicon nodes from multiple different suppliers), improved silicon yield resiliency and the continued need for rapid time to market. Additionally, compact HI sub-systems using (mostly) advanced packages substrates today enable significantly larger die area (>3x reticle equivalent). 2D and 3D package architectures are ideal heterogeneous integration platforms because they provide short, power efficient, high-bandwidth connections between components in compact form factors. As bandwidth increases, the power consumed transferring the data and the impact of delay time in transit both benefit from the shorter path lengths enabled by advanced 2D and 3D interconnects. Today's heterogeneous packaging technologies:

- Deliver power-efficient, high-bandwidth on-package IO links using different communication protocols
- Enable a diversity of off-package IO protocols
- Deliver noise isolation for single ended and differential on-package and off-package signaling
- Manage increasing cooling demands
- Support complex power delivery architectures
- Meet diverse application functionality, form factor and weight constraints ranging from high performance servers to flexible, wearable electronics
- Meet a broad spectrum of reliability requirements for different market segments and applications
- Provide cost effective, high precision and quick turn assembly to meet fast production ramps

In this respect they differ from packaging for homogeneous integration in terms of increased complexity and the increased focus on on-package bandwidth. Developing products using advanced packaging requires an integrated approach involving collaboration with product architects, system architects, process engineers, materials engineers, and reliability engineers, and a detailed understanding of the fundamental thermal, mechanical, electrical and materials characteristics of the various architectures.

2. Scope

This roadmap chapter has a two-fold purpose:

- Define and proliferate a standardized nomenclature for package architectures covering, and clearly demarcating, both 2D and 3D constructions. Currently there are a number of intermediate definitions between 2D and 3D constructions, referred to as 2.xD architectures. Experts in this road-mapping effort, representing a wide spectrum of industry, academia, and consultants, agree that the current nomenclature (e.g., 2.1D, 2.3D, 2.5D architectures) does not have a common rational basis and that there is a need to provide a comprehensive classification framework based on a common set of assumptions. The objective of this chapter is to drive clarity and provide a nomenclature framework that will house different architectures.
- Define and proliferate key metrics driving the evolution of the physical interconnects in these architectures. This chapter will list their current values (based on the state of the art) and projections for the next generations.
- The chapter is organized into 4 primary areas:
- Converged Nomenclature Framework for 2D and 3D Architectures
- Key Metrics:[2]
    - Design Attributes

[2] Other key attributes such as thermal and process attributes are covered in different chapters in this roadmap

- Electrical Attributes including Signal Integrity and Power Delivery
- Difficult Challenges
- Discussion

3. Converged Nomenclature Framework for 2D & 3D Architectures

a. A 2D architecture is defined as an architecture where two or more active silicon devices are placed side-by-side on a package and are interconnected on the package. If the interconnect is "enhanced", i.e., has higher interconnect density than mainstream organic packages, and is accomplished using an organic medium, the architecture is further sub-categorized as a 2DO (2D Organic)[3] architecture and similarly, if the enhanced architecture uses an inorganic medium (e.g., a silicon/glass/ceramic interposer or bridge) the architecture is further sub-categorized as a 2DS architecture. Architectures that include enhancements over and above traditional 2D architectures (typically 2 or more die flip-chip attached on a traditional organic package) are variously referred to as 2.x architectures to emphasize their specialness. These nomenclatures do not have any particular technical basis. It is proposed here that they all be broadly categorized as enhanced architectures.

b. A 3D architecture is defined as an architecture, where two or more active silicon devices are stacked and interconnected **without** the agency of the package.

The ideas described by this nomenclature[4] are schematically shown in Figure 1.

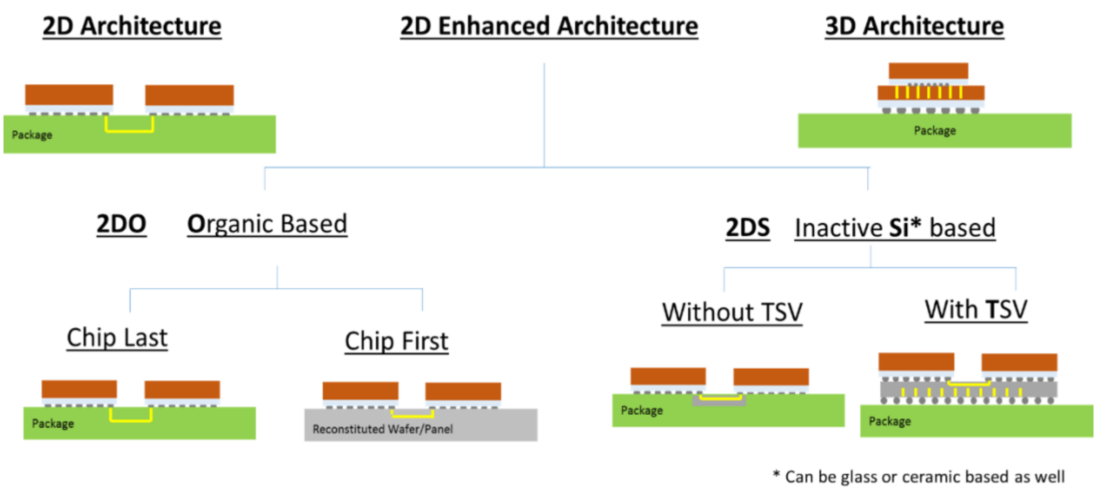

Figure 1: Schematic describing the Converged Nomenclature Framework for 2D & 3D Architectures. Note that the difference between the 2D and 2DO Chip Last schematic in this figure is in the interconnect density in the die-die links. The latter has increased interconnect density enabled by finer lines and spaces along with reduced sized vias and via pads. In the 2DS images the grey color is used for silicon (or glass)[5]

[3] Accomplished by using a monolithic high-density substrate or more likely a high density organic interposer [10, 11, 16]

[4] Figure 1 only describes a nomenclature and technology equivalence between architectures is not intended or implied.

[5] Figure 1 is expected to undergo considerable changes in an upcoming revision, likely in the second half of 2024, to reflect recent technology developments. E.g., a 2021 paper points to three categories i.e. Die-First, Die-Middle and Die-Last [30].

4. Interconnect Nomenclature

Package interconnects can be classified as:

(a) **Die-Die Interconnects:** Interconnects between stacked die for vertical connectivity between multiple dies in a 3-D stack. These may be further sub-categorized using the process these interconnects are created with, which can lead to different physical attributes, such as Die-Die interconnects created using a:

a. Wafer-to-Wafer (W2W) attach process (Wafers could be reconstituted e.g. rW2rW or W2rW)
b. Die-to-Wafer (D2W) attach process (Wafer could be reconstituted i.e. D2rW)
c. Die-Die (D2D) attach process

The roadmap for these interconnects is described in Section 5.1.1.

(b) **On-package Die-Die Interconnects[6]:** i.e., 2D and 2D Enhanced Interconnects: Interconnects between die (and/or die stacks/pre-packaged die) within the package for lateral connectivity. The roadmap for these interconnects is described in Section 5.1.1.

(c) **Die-to-Package Interconnects:** Interconnects between the die and the package (Figure 2), typically known as the first level interconnect (FLI).

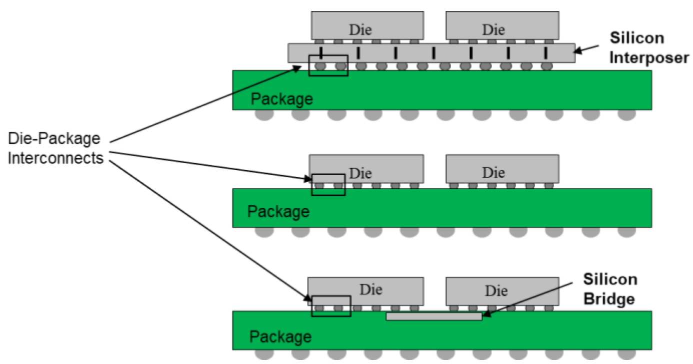

Figure 2: Schematic showing the die-package interconnects[7].

The schematic in Figure 2 only shows area-array interconnects. Wire-bond interconnects are also an important die-to-package interconnect. For details on the wire-bonding technology including discussions on multi-tier stacking that allows for considerable innovations on heterogeneous integration, the reader is referred to the chapter on Single Chip and Multi-Chip Integration in this roadmap [32].

Another key metric is the flip-chip pitch for area array interconnects. Table 1 shows a 7-year trend for the traditional flip-chip pitch. Given that the pace of change is flat, and that the utility of finer bump pitch is limited by feature sizes within the substrate (line/space, via pad, etc.) it is reasonable to assume that 2D flip-chip pitch will stay at a minimum bound of 90µm[8] (this does not cover the fine pitch scaling available in 2D Enhanced and 3D architectures).

[6] An in-depth analysis for die-to-die and die-to-wafer interconnects is also presented in a recently published report on Manufacturing Roadmap for Heterogeneous Integration and Electronics Packaging (MRHIEP) [31]. The reader is referred to chapters 1 and 2.

[7] Note that the values discussed in this section do not include the case where the organic substrate is scaled to accept fine pitch die stacks such as HBM @ 55µm, with and without EMIB. Since instances such as these are more relevant to die-die interconnects, they are discussed in Section 5.1.1.

[8] Statement limited to full area array interconnects since there have been cases (e.g. Qualcomm® Snapdragon™ 820) where 80µm pitch on embedded FLI pad has been shown for an essentially 3 rows deep peripheral interconnect.

Year of Production	2018	2019	2020	2021	2022	2023	2024
Flip chip array, low end & consumer (µm)	150	150	130	130	130	130	130
Flip chip – cost performance (µm)	110	110	110	100	100	100	90
Flip chip – high performance (µm)	110	100	100	90	90	90	90

Table 1: Die-Package Interconnect Pitch Roadmap

(d) **Within-Package Interconnects:** Interconnects within the package that enable lateral connections between two or more die. Roadmap projections of within-package interconnects are not discussed in this chapter. The reader is referred to the chapter on package substrate technologies (Chapter 8).

(e) **Package-to-Board Interconnects:** Interconnects between the package and the next level, which is typically the motherboard, are referred to as the second level interconnect (SLI). SLI connections are either socketed or ball grid array (BGA) and may be combined with on package cabling[9]. The 2015 ITRS roadmap projections for socket pin counts are reproduced below [33] in Table 2a[10]. Figure 3 shows a trend graph based on how sockets have evolved, thus far with an exponential pin count growth. While the 2015 ITRS projections are reasonable extrapolations for the cost-performance segment (minor changes are shown in Table 2b), for the high-performance segments, the projections seem to be under-projecting significantly after 2021. This is likely because the pin-count increase trend in the 2015 projections was assumed to be linear. Figure 4 shows an updated projection for the high-performance segment. The exponential pin-count growth is expected to continue for high performance compute segment due to heterogeneous integration and especially with the growth of artificial intelligence and data center applications demanding high bandwidth memory and I/O signaling with more than 15K pins projected before the end of this decade [34].

	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
Low-end, Low-cost package	550	550	550	600	600	600	600	600	650	650	650	650
Memory (MCP)	260	280	280	280	280	280	280	280	280	280	280	280
Cost-performance	3200	3300	3400	3500	3600	3700	3800	3900	4000	4100	4200	4300
Harsh	693	728	764	803	843	860	877	894	911	928	945	962
High performance	5394	5651	5934	6231	6543	6855	7167	7479	7791	8103	8415	8727

Table 2a: Socket pin count projections from 2015 ITRS [33]

[9] This chapter does not address on package cabling solutions or provide a roadmap since this class of solutions is still maturing.

[10] The ball count for Mobile packages has been removed from this table. The 2015 projections show a flat trend, and this trend needs additional study in light of the current evolution of mobile products.

	2019	2020	2021	2022	2025	2028	2031	2034
Cost performance	3200	3300	3400	3500	3800	4100	4400	4700

Table 2b: Updated projections for socket pin count in the Cost-Performance and High-Performance segments

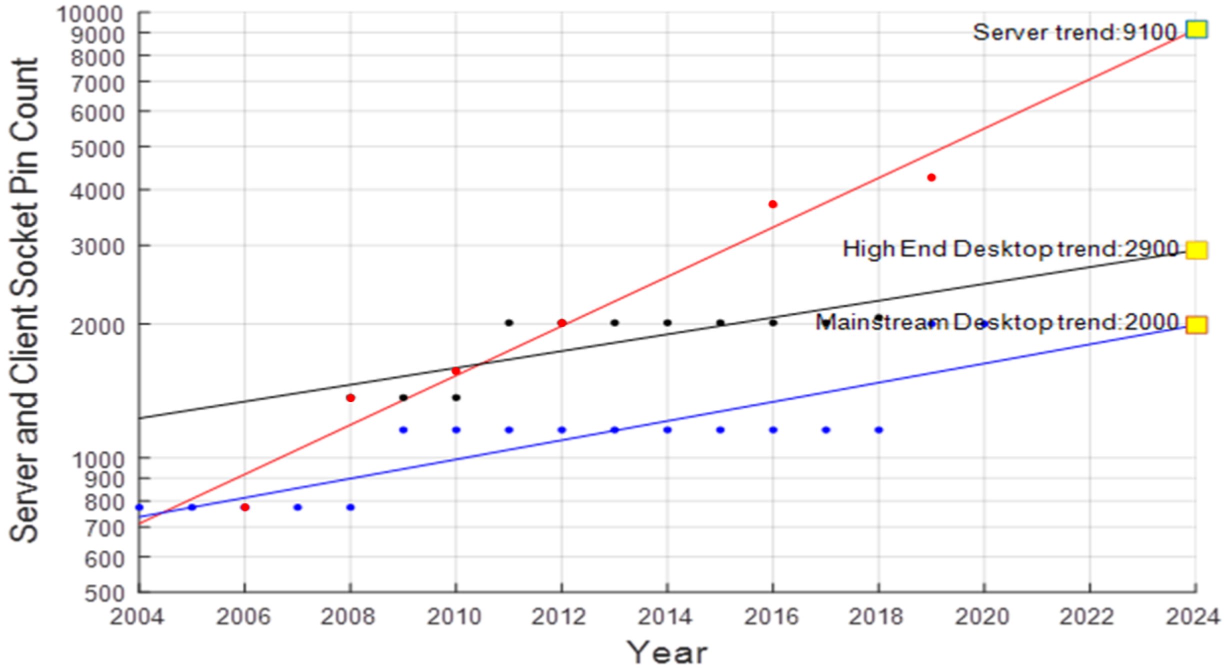

Figure 3: Socket pin count trend till 2024 (Source: Intel).

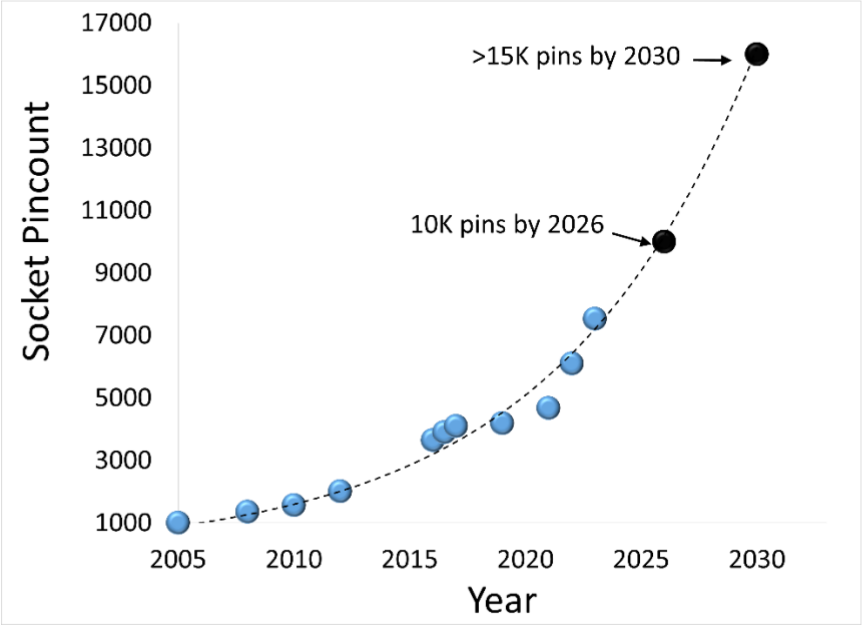

Figure 4: Historical high performance compute socket pin growth extrapolated out to the end of the decade.

As described in [35], off-package bandwidth, electrical lane speeds and ASIC IO continue to scale steadily. In addition to pin-count changes, socket constructions that minimize signaling losses should be developed. 2015 ITRS projections for BGA[11] pitch continue to be valid.

(f) **POP (Package-on-Package) Interconnects:** The PoP construction [36] allows for packages to be placed on top of other packages using peripheral package interconnects, also referred to as VI (Vertical Interconnects). It is typically used to stack memory packages on logic to create compact form factors. One such typical construction is shown in Figure 4.

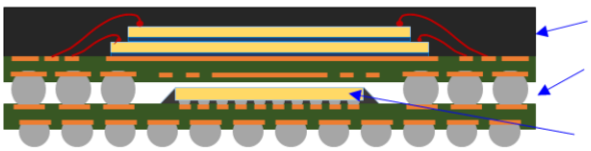

Figure 5: Typical Package-on-Package Architecture.

The VI pitch (i.e. pitch of interconnects between top and bottom package) and the overall height of the package are two key characteristics for this architecture. Currently there is no methodology to project a roadmap for these architectures and in lieu of such a roadmap, the state-of-the-art pitches and package heights, along with their projected changes, are listed in Table 3.

PoP Architectures	VI Pitch (mm)	Maximum Bottom Package Height (mm)
Bare Die PoP	0.5	0.75
Bare Die PoP with 2-Step solder resist (SR) + solder on pad (SOP)	0.4	0.75
TMV (Through Mold Via) PoP	0.4	0.78
Exposed Die TMV PoP	0.35 → 0.27	0.69
Interposer PoP	0.27 → 0.20	0.67
FOWLP PoP	0.30 → 0.20	0.50 → 0.30

Table 3: State-of-the-Art Pitches and Package Heights and their projected targets for PoP Architectures (Source: TechSearch International)

[11] The focus in BGA interconnects and more broadly in other solder joints is on low temperature solders to provide additional options within the reflow hierarchy and opportunities for reduced power usage during manufacturing (hence greater environmental friendliness). There is extensive literature in this area in recent years, however it is not covered in this chapter.

5. Key Metrics

5.1 Design Attributes[12]

The physical attributes and signaling speeds needed to enable generation over generation Bandwidth (BW) doubling are described in this section.

5.1.1 Peripheral Interconnects for 2D and 2D Enhanced Architectures (see Figure 1)

A key role of packaging is to provide physical interconnects.[13] Two design metrics that describe capability of these interconnects are linear escape density and areal escape density. These two metrics are shown in Figure 6A. Note that these two can be combined into a single metric by multiplying the two (Figure 6B). The same metric has also been described by other researchers [37]. Tables 4-6 show possible ways of physical interconnect scaling instead of only signaling speed scaling to achieve raw bandwidth doubling (or greater)[14] generation over generation. Such scaling can achieve aggressive bandwidth targets while keeping the signaling speeds relatively low, so that it is feasible to achieve a very low raw bit error rate (BER) such as 10^{-18}. This avoids the complicated error correction circuits and minimizes the I/O latency. It is important to emphasize that the physical IO dimensions listed are not bounding parameters and depend on specific business and technical demands i.e., the same bandwidth doubling can be achieved through more or less aggressive choices of the physical IO dimensions.

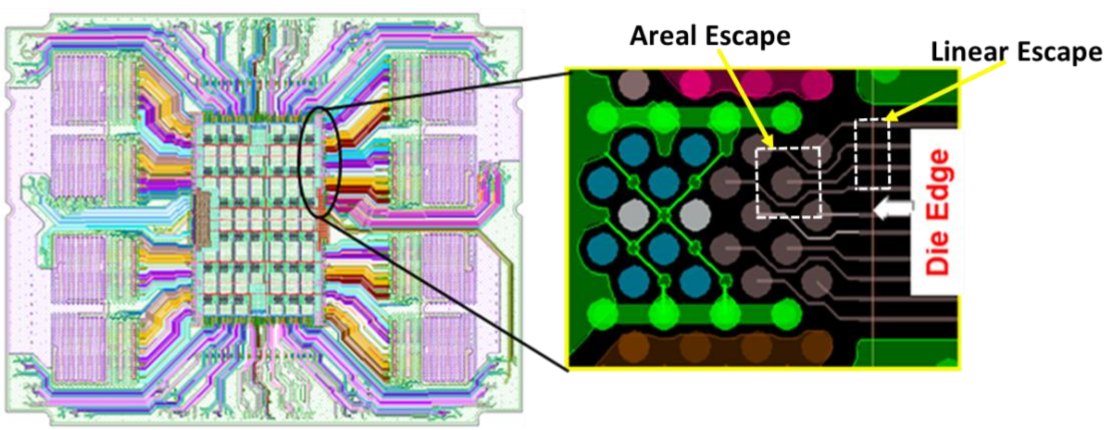

Figure 6A: Two Key Physical Design Attributes: (a) IO/mm (of die edge) – Linear Escape Density and (b) IO/mm2 (of die) – Areal Escape Density. Note that the term IO here refers to physical bumps and wires.

[12] 2D to 3D packaging architectures provide the physical construction architecture to enable signaling and power delivery. the first order, these physical constructions are agnostic to the IO protocols for which they are used. Hence all attributes described here are independent of the IO protocol.

[13] These interconnects must be designed to minimize power consumption and signal distortion in addition to provide effective interconnects [38-40].

[14] Previous revisions of the roadmap only showed bandwidth doubling. However, as this revision quantitatively shows, greater than raw bandwidth doubling is possible.

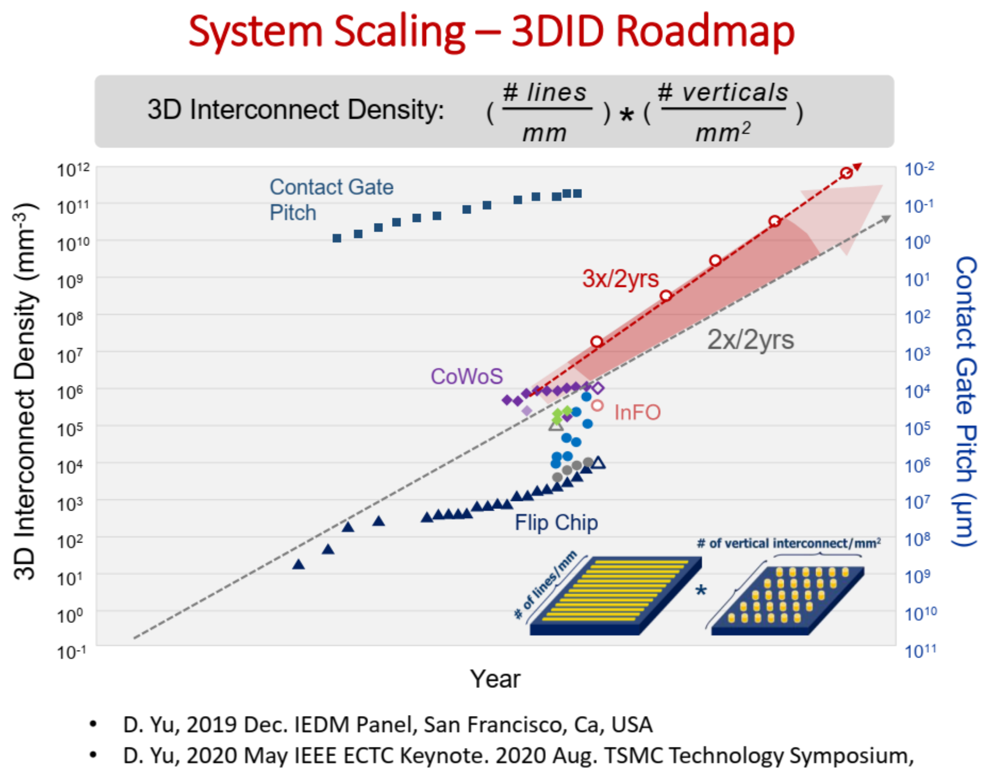

Figure 6B: Two Key Physical Design Attributes: (a) IO/mm (of die edge) – Linear Escape Density and (b) IO/mm2 (of die) – Areal Escape Density are multiplied to create a single 3D Interconnect Density (3DID). Note that the term IO here refers to physical bumps and wires. (Ack: TSMC)[15]

Generation Number[16] →		**1**	**2**	**3**	**4**	**5**
Raw Linear Bandwidth Density (GBps/mm)[17,18,19,20]		125	250	500	1000	2000
Package Technology	Minimum Bump Pitch (µm)	55	50	40	35	30

[15] Acronyms CoWoS (Chip-on-Wafer-on-Substrate) and InFO (Integrated Fan-Out) are well known in the industry.

[16] At present there is no universal understanding/agreement of the required time gap between generations. The TWG judgment is that it will be a minimum of 2 years, and from a planning perspective we recommend a maximum of 3 years, to ensure that the interconnect roadmap is competitive. Both these numbers reflect the leading edge and mainstream implementations will depend on both economic and technical factors.

[17] Per mm of die edge.

[18] Starting value of 125 GBps/mm is estimated raw bandwidth possible in an AIB style implementation.

[19] Raw Bandwidth is essentially the product of # of connections and signaling speed per connection. Achieved bandwidth will be lower since not all connections are used for data transmission. The starting point of 125 GBps/mm is a judged value.

[20] Note that @ 32Gbps UCIe-A theoretical BW@ 45um pitch is 2.2716 TBps & this roadmap states @ 3Gbps & @ 40µm pitch a theoretical BW of 0.25TBps is possible. There is no discrepancy in the numbers and modulating speed (hence power efficiency) is a knob for scaling BW.

	Linear Escape Density (IO/mm)[21]	500	667	1000	1500	2000
	Areal Escape Density (IO/mm^2)	331	400	625	816	1111
Signaling Speed (Gbps)[22]		2	3	4	5.33	8

Table 4: Physical IO Scaling Roadmap 2D and 2D Enhanced Architectures that use Solder based Interconnects. Note that bump pitch in this table is conservatively placed at 30µm in Generation 5 and lower pitch capability has been demonstrated [41] so more than 5 generations are possible. The conservative choice allows for the large die to be assembled with high manufacturing yield.

Generation Number →		**1**	**2**	**3**	**4**	**5**	**6**	**7**
Raw Linear Bandwidth Density (GBps/mm)		125	250	500	1000	2000	4000	8000
Package Technology	Minimum Bump Pitch (µm)[23]	55	40	30	20	10	5	2.5
	Linear Escape Density (IO/mm)	500	667	1000	1333	2000	4000	8000
	Areal Escape Density (IO/mm^2)	331	625	1111	2500	10000	40000	160000
Signaling Speed (Gbps)		2	3	4	6	8	8	8

Table 5: Physical IO Scaling Roadmap for 2D and 2D Enhanced Architectures that use both solder and hybrid interconnects

[21] Since multiple silicon back-end layers or package layers can be used to route the bumps, specific geometrical features of the layers are not described.

[22] Representative example showing how the BW goals are reached. These speeds are not unique.

[23] Starting value of 55µm is based on initial HBM pitch

5.1.2 Area Interconnects for 3D Architectures (see Figure 1)

Generation Number →		1	2	3	4	5	6	7	8
Raw Areal Bandwidth Density (GBps/mm^2)[15, 24]		125	250	500	1000	2000	8000	32000	200000
Package Technology	Minimum Bump Pitch (µm)	40	30	20	15	10	5	2.5	1
	Areal Escape Density (IO/mm^2)	625	1111	2500	4444	10000	40000	160000	1000000
Signaling Speed (Gbps)[25]		1.6	1.8	1.6	1.8	1.6	1.6	1.6	1.6

Table 6: Physical IO Scaling Roadmap for 3D architectures that use both solder and hybrid interconnects

5.2 Signal Integrity Attributes

5.2.1 Signal Integrity Attributes for 2D and 2D Enhanced Architectures

The short and high-density interconnects described in Section 5.1.1 become more and more RC dominated with the generational scaling. The interconnect inductance is expected to have a secondary effect on the channel performance. Table 7 shows the reduction of channel length with the bump pitch scaling. This does compensate the larger per-unit-length RC of denser routing interconnects, so that the total channel RC loss does not increase from generation to generation.

Generation Number →		**1**	**2**	**3**	**4**	**5**	**6**	**7**
Linear Bandwidth Density (GBps/mm)		125	250	500	1000	2000	4000	8000
Channel Performance	Channel Length (mm)	<2.0	<1.7	<1.4	<0.8	<0.50	<0.25	<0.15
	Bump-to-Bump Channel RC (ps)	<10	<10	<10	<10	<10	<10	<10

Table 7: Channel Signaling Characteristics for 2D and 2D Enhanced Architectures

[24] Per mm^2 of die area.

[25] Note that previous versions of this chapter had shown a range of signaling speeds. The range has been removed to simplify the table.

5.2.2 Area Interconnects

The signal integrity performance of the extremely short area vertical interconnects is dominated by their capacitance. Their resistance and inductance are expected to have a secondary impact on the channel performance with the generational scaling. Table 8 shows the scaling of bump capacitance with the bump pitch reduction. The improved capacitance is an important enabler to avoid the need for stronger driver design.

Generation Number →	1	2	3	4	5	6	7	8
Areal Bandwidth Density (GBps/mm^2)	125	250	500	1000	2000	8000	32000	200000
Bump Capacitance (fF)	<30	<22	<15	<10	<7	<5	<3	<1

Table 8: Channel Signaling Characteristics for 3D Architectures

5.3 Power Delivery Attributes: Area Interconnects for 2D and 3D Architectures

The main power consumption in microprocessors is from cores rather than the IO domains. As a result, the generational numbers used to represent interconnect scaling do not necessarily correlate to power consumption on the compute cores. As a result, we will scale the power delivery targets as a function of time. Table 9 reflects projected demand and packaging engineers will be challenged and will need to explore new materials and architectures to deliver capacitance and current carrying capabilities. Though not a focus of this chapter, it should be pointed out that with increasing HI, greater focus on power delivery is anticipated including (1) proliferation of IVR integration on package and on chip, (2) embedded inductors and capacitors displacing and or complementing board level components in some emerging architectures, (3) increased and urgent need for much more granular power delivery, and escalation of power rails in the package as "heterogenous integration" continues to increase on a single package, (4) accelerating drivers for vertical power delivery architectures in the package, and last but not the least, (5) impact of the imminent backside power delivery on chip at 2nm node and beyond. In this context, there will be a drive for both discrete passives complemented by more integrated passives.

Year	**2024**	**2026**	**2028**	**2030**	**2032**
Maximum Core Power Density (W/mm^2)	5	7	10	14	20
Sustained Core Power Density (W/mm2)	1	1.4	2	2.8	4
On-die MIM Capacitance Density (nF/mm^2)	140	210	320	520	800
VR Power Density (W/mm^2)	1	1.4	2	2.8	4
Ceramic Cap Density (µF/mm^2)[26]	10	14	20	28	40
Sustained Bump Current Carrying Capability (A/mm^2)	2.8	4.3	6.1	9.3	13.3
Sustained TSV Current Carrying Capability (A/mm^2)	2.8	4.3	6.1	9.3	13.3

Table 9: Power delivery Attributes for 2D, Enhanced-2D and 3D Architectures. It should be noted that power delivery attributes are agnostic to the architecture

[26] Errata: Ceramic cap density values in the 2020 version of this chapter had an error i.e., an extra "0" was included in Gens 4 and 5

6. Review of Different Packaging Architectures:

In this section, we tabulate the various examples seen in literature with their corresponding architecture type, interconnection materials used, tightest pitches observed and the required processes and equipment to enable them. In addition, we list the resulting applications, reliability concerns and any additional challenges resulting from the same. This is a broad overview intended to offer perspective on all the interconnect technologies.

Table 5. Examples of applications from literature as a function of the different packaging architecture and process/material attributes. [42, 43]

Architecture Type (2D / 2D Enhanced / 3D)	**Interconnect Technologies**	**Tightest Die to Package Pitch[27]**	**Typical Interconnection Process**	**Typical Equipment**	**Typical Applications**	**Key Concerns and Challenges (Partial List)**	**Advantages (Partial List)**
2D [44]	Wire-Bonding	25 µm	Wire-bonding	Wire-Bonder	Automotive, LCD drivers, Sensors, ASICs, Controllers	- Oxidation of Cu bonds - Wire-bond lift-off due to CTE mismatch	- Low cost-of-ownership - Flexible process - Easy to test / re-work wire-bonds
2D & 2D Enhanced [45]	Micro-bumps, C4s, TSVs, and passive Si Interposer	20 µm	- Thermal compression bonding (TCB) - Mass reflow	Thermo-compression bonding (TCB) tools, Reflow oven	CPUs, GPUs, FPGA, Network servers, Gaming Console Servers	- Warpage issues due to large package size - Interposer testing - Handling thinned wafers	- Packaging enables high performance - Multifunction heterogeneous integration e.g., ASIC + HBM
2D Enhanced, 3D die-to-die, die-to-wafer [46-48]	Cu pillars, passive and active Si coupons & wafers	< 10 µm	- Solderless Cu-Cu thermal compression bonding (TCB) - Mass-reflow	Modified Thermal compression bonding (TCB) tools	AI, High Performance Computing (HPC)	- Ensuring known good dies (KGD) - Test coverage - Die handling - No re-workability - Misalignment during die placement	- Already established TCB tooling with improvements - Pitch scaling - Heterogeneous integration
3D Die-to-Die, Die-to-Wafer [49-58]	Micro-bumps, TSVs, Cu-Cu Bonding	5 µm	- F2F or F2B Direct Cu-Cu bonding interconnection - Thermal compression bonding with Cu-Solder interconnection	Custom bonding equipment	AI, High Performance Computing (HPC)	- Ensuring known good dies (KGD) - Test coverage limited during wafer probing - High cost of ownership - Misalignment / Foreign Materials (FM) particles during die placement	- Pitch Scalability
3D Wafer-to-Wafer [50]	Cu-Cu Bonding	0.9 µm	F2F or F2B Direct Cu-Cu bonding interconnection	Custom bonding equipment	AI, High Performance Computing (HPC)	- Ensuring known good dies/stacks - Test coverage limited during wafer probing - High cost of ownership - Misalignment / FM particles during die placement	High 3D interconnect density with ultra-low bonding latency

[27] Reference envelope values. Values listed in Table in this chapter represent the broader mainstream envelopes

7. Difficult Challenges

The high IO/mm values listed in Tables 4 and 5 are achieved using silicon back-end technologies to create thin, closely spaced wires (Figure 6). This roadmap projects the need for increasing density, i.e., reduced line pitch. When combined with increasing signal speeds, there will be greater concerns about signal quality due to increased crosstalk, caused by the reduced line spacing. The packaging community will be challenged to develop solutions that minimize impact to signal integrity and provide physical links with improved power efficiency.[28]

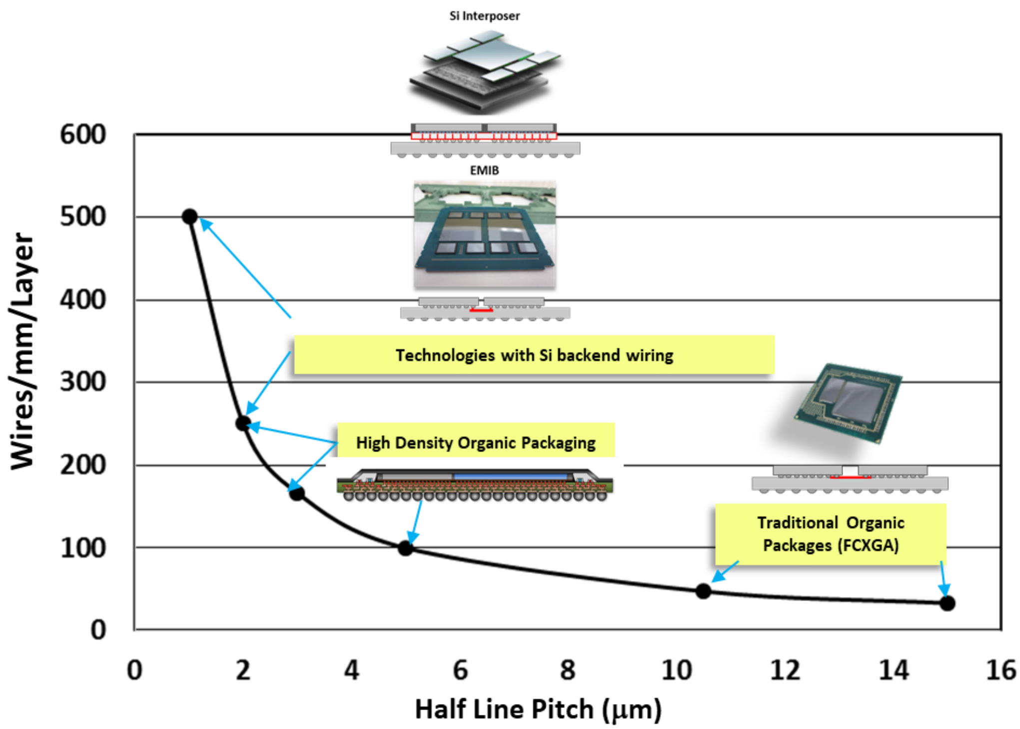

Figure 7: Technologies for different wiring features. L is the width of the line in µm, S is the minimum space between lines in µm; half line pitch is (L+S)/2. Technologies that use silicon backend wiring can achieve wiring densities of greater than 1000 with L & S ≤ 0.5µm.

There will be greater need to enable novel assembly technologies for ultra-fine pitch 2D Enhanced and 3D architectures using both solder and non-solder-based approaches. A number of researchers have demonstrated the reduced bump pitches described in Table 4 and there is a fairly good understanding of the technologies needed to transition from solder-based interconnects to solderless interconnects [22-24, 42, 43, 45-58]. Key challenges for stacked-die architectures will continue to be in fine pitch sort/test, thermal management, power delivery network development, design process co-optimization, in-line process control and equipment readiness for high volume.

8. Discussion

The primary driver for advanced 2D and 3D packaging technologies is the need for increased interconnect densities to support HI and deliver increasing bandwidth in a power efficient manner while enabling efficient power delivery. An increasing number of innovative packaging architectures deliver significantly improved HI

[28] Power efficiency (measured in pJ/bit) is a sum of Tx, Rx and link power efficiency. The die-die links need to provide reducing RC (Table 6) to ensure improved power efficiency.

envelopes. In these HI architectures physical interconnects (i.e., wires, bumps) and link RC characteristics are completely under the control of packaging technologists, and it is relatively easy to establish a non-unique scaling roadmap. Already a number of power efficient, high bandwidth (custom and standardized) IO links that take advantage of advanced packaging have been defined to further spur the proliferation of heterogeneous integration [59-71][29]. We anticipate that moving forward, this chapter will spur discussion among product architects and will help develop further clarity on various use cases that will drive the pace of technology innovation. Delivering higher interconnect densities will challenge packaging engineers to develop novel materials, assembly processes and metrologies to develop cost effective technology solutions that meet the performance demands of future HI architectures. Even though it is not the focus of this chapter, it is also important to note that the ability to integrate the right thermal features will define the physical envelope (i.e., form factor and number of die/die stacks that can be integrated on the package) and the warpage characteristics that will ensure manufacturability [72].

9. Acknowledgments

We would like to acknowledge the contributions of other TWGs.

10. References

1. Shalf J. 2020, "The future of computing beyond Moore's Law". Phil. Trans. R. Soc. A 378: 20190061, http://dx.doi.org/10.1098/rsta.2019.0061
2. https://www.darpa.mil/program/common-heterogeneous-integration-and-ip-reuse-strategies
3. https://www.eetimes.com/the-case-for-heterogeneous-integration/
4. A. B. Kelleher, "Celebrating 75 years of the transistor A look at the evolution of Moore's Law innovation," 2022 International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2022, pp. 1.1.1-1.1.5, doi: 10.1109/IEDM45625.2022.10019538.
5. D. C. H. Yu, C. -T. Wang and H. Hsia, "Foundry Perspectives on 2.5D/3D Integration and Roadmap," 2021 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2021, pp. 3.7.1-3.7.4, doi: 10.1109/IEDM19574.2021.9720568.
6. R. Agarwal et al., "3D Packaging for Heterogeneous Integration," 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2022, pp. 1103-1107, doi: 10.1109/ECTC51906.2022.00178.
7. https://hc33.hotchips.org/assets/program/tutorials/Tutorial_Mahajan_Sane_HotChips_2021_Talk_final_Formatted_1.pdf
8. Advances in Embedded and Fan-Out Wafer Level Packaging Technologies, Beth Keser (Editor), Steffen Kröhnert (Editor), ISBN: 978-1-119-31413-4 February 2019 Wiley-IEEE Press
9. 3D Microelectronic Packaging: From Fundamentals to Applications, Li, Yan, Goyal, Deepak (Eds.), Springer Series in Advanced Microelectronics, 2021.
10. J. H. Lau, "Recent Advances and Trends in Multiple System and Heterogeneous Integration With TSV Interposers," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 13, no. 1, pp. 3-25, Jan. 2023, doi: 10.1109/TCPMT.2023.3234007.
11. J. H. Lau, "Recent Advances and Trends in Advanced Packaging," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 12, no. 2, pp. 228-252, Feb. 2022, doi: 10.1109/TCPMT.2022.3144461.
12. K. Oi, et al, "Development of New 2.5D Package with Novel Integrated Organic Interposer Substrate with Ultra-Fine Wiring and High-Density Bumps," Proceedings of the 2014 IEEE 64th Electronic Components and Technology Conference, Orlando, pp. 348-353.

[29] Chapter 6 the MRHIEP report also discusses IO requirements and examples of the IO protocols (UCIe[57,58], BoW[59,60], and SuperCHIPS[63,65]) for within package interconnections in context of high performance computing applications [31].

13. R. Mahajan et.al, Embedded Multi-Die Interconnect Bridge (EMIB) – A High Density, High Bandwidth Packaging Interconnect, 2016 IEEE 66th Electronic Components and Technology Conference, DOI 10.1109/ECTC.2016.201
14. R. Mahajan et al., "Embedded Multi-die Interconnect Bridge—A Localized, High-Density Multichip Packaging Interconnect," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 9, no. 10, pp. 1952-1962, Oct. 2019, doi: 10.1109/TCPMT.2019.2942708
15. M. Sunohara, T. Tokunaga, T. Kurihara and M. Higashi, "Silicon interposer with TSVs (through silicon vias) and fine multilayer wiring," in Proc. IEEE Electronic Components and Technol. Conf. (ECTC), Lake Buena Vista, FL, May 27–30, 2008, pp. 847–852.
16. S. Miki, H. Taneda, n. Kobayashi, K. Oi, K. Nagai, T. Koyama, "Development of 2.3D High Density Organic Package using Low Temperature Bonding Process with Sn-Bi Solder," Proceedings of the 2019 IEEE 69th Electronic Components and Technology Conference, Las Vegas, pp. 1599-1604.
17. D. Ingerly, et al. "Foveros: 3D Integration and the use of Face-to-Face Chip Stacking for Logic Devices," 2019 International Electron Devices Meeting, San Francisco, CA, Dec. 2019.
18. A. A. Elsherbini, S. M. Liff and J. M. Swan. "Heterogeneous Integration Using Omni-Directional Interconnect Packaging," 2019 International Electron Devices Meeting, San Francisco, CA, Dec. 2019.
19. G. Gao et al., "Low Temperature Cu Interconnect with Chip to Wafer Hybrid Bonding," 2019 IEEE 69th Electronic Components and Technology Conference (ECTC), 2019, pp. 628-635, doi: 10.1109/ECTC.2019.00100.
20. S. Kim et al., "Ultra-Fine Pitch 3D Integration Using Face-to-Face Hybrid Wafer Bonding Combined with a Via-Middle Through-Silicon-Via Process," 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), 2016, pp. 1179-1185, doi: 10.1109/ECTC.2016.205.
21. A. Elsherbini, S. Liff, J. Swan, K. Jun, S. Tiagaraj and G. Pasdast, "Hybrid Bonding Interconnect for Advanced Heterogeneously Integrated Processors," 2021 IEEE 71st Electronic Components and Technology Conference (ECTC), 2021, pp. 1014-1019, doi: 10.1109/ECTC32696.2021.00166.
22. E. Beyne, "The 3-D Interconnect Technology Landscape," in IEEE Design & Test, vol. 33, no. 3, pp. 8-20, June 2016, doi: 10.1109/MDAT.2016.2544837.
23. https://news.samsung.com/global/samsung-announces-availability-of-its-silicon-proven-3d-ic-technology-for-high-performance-applications
24. https://3dfabric.tsmc.com/english/dedicatedFoundry/technology/SoIC.htm
25. https://www.youtube.com/watch?v=j0z4FweCy4M&t=2814s
26. https://www.youtube.com/watch?v=eieRXlaDuzo
27. https://www.youtube.com/watch?v=gqAYMx34euU
28. https://www.youtube.com/watch?v=xnMmd2zZ3RM
29. R. Mahajan, "Quiet Revolutions: How Advanced Microelectronics Packaging Continues to Drive Heterogeneous Integration," 2020 19th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (Itherm), 2020, pp. 1408-1412, doi: 10.1109/Itherm45881.2020.9190247.
30. D. C. Hu, E. H. Chen, J. C. Lee, C. P. Sun and C. C. Hsu, "2.2D Die last Integrated Substrate for High Performance Applications," 2021 IEEE 71st Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2021, pp. 157-163, doi: 10.1109/ECTC32696.2021.00036.
31. https://www.chips.ucla.edu/page/MRHIEP%20Project/MRHIEP%20Final%20Report
32. Chapter 8: Single Chip and Multi-Chip Integration, 2019 HI Roadmap, https://eps.ieee.org/images/files/HIR_2019/HIR1_ch08_smc.pdf
33. https://www.semiconductors.org/resources/2015-international-technology-roadmap-for-semiconductors-itrs/
34. S. Nekkanty, K. Meyyappan, S. Mondal and P. Tadayon, "Liquid Metal Interconnects for High Pin Count Scaling and Socketing Applications," in IEEE Transactions on Components, Packaging and Manufacturing Technology, doi: 10.1109/TCPMT.2023.3344328.
35. http://www.ieee802.org/3/cfi/1117_3/CFI_03_1117.pdf

36. R. Co et al., "High-Volume-Manufacturing (HMV) of BVA Enabled Advanced Package-on-Package (PoP)," ICEP, April 14-17, 2015.
37. https://www.imec-int.com/en/articles/view-3d-technology-landscape
38. K. Cho et al., "Design optimization of high bandwidth memory (HBM) interposer considering signal integrity," 2015 IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS), Seoul, 2015, pp. 15-18.
39. S. Jangam, A. A. Bajwa, K. K. Thankkappan, P. Kittur and S. S. Iyer, "Electrical Characterization of High-Performance Fine Pitch Interconnects in Silicon-Interconnect Fabric," 2018 IEEE 68th Electronic Components and Technology Conference (ECTC), San Diego, CA, 2018, pp. 1283-1288.
40. Ahmet C. Durgun, Zhiguo Qian, Kemal Aygun, Ravi Mahajan, Tim Tri Hoang, Sergey Yuryevich Shumarayev, "Electrical Performance Limits of Fine Pitch Interconnects for Heterogeneous Integration," accepted for publication, ECTC Las Vegas, 2019.
41. Z. Li et al., "Scaling Solder Micro-Bump Interconnect Down to 10mm Pitch for Advanced 3D IC Packages," 2021 IEEE 71st Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2021, pp. 451-456, doi: 10.1109/ECTC32696.2021.00082
42. W. H. Knausenberger and M. R. Pinnel, "Interconnection Trends and Impact on Materials," MRS Online Proc. Libr., vol. 72, no. 1, pp. 255–266, Dec. 1986, doi: 10.1557/PROC-72-255.
43. J. U. Knickerbocker et al., "Three-dimensional silicon integration," IBM J. Res. Dev., vol. 52, no. 6, pp. 553–569, Nov. 2008, doi: 10.1147/JRD.2008.5388564.
44. "Wire-bond Technology Rolls On," Semiconductor Engineering, May 08, 2017. https://semiengineering.com/wirebond-technology-rolls-on/.
45. "The Race to Next-Gen 2.5D/3D Packages," Semiconductor Engineering, Sep. 23, 2019. https://semiengineering.com/the-race-to-next-gen-2-5d-3d-packages/
46. S. C. Jangam and S. S. Iyer, "Silicon-Interconnect Fabric for Fine-pitch (≤10 µm) Heterogeneous Integration," in IEEE Transactions on Components, Packaging and Manufacturing Technology, doi: 10.1109/TCPMT.2021.3075219
47. K. Sahoo, U. Rathore, S. Chandra Jangam, T. Nguyen, D. Markovic and S. S. Iyer, "Functional Demonstration of < 0.4-pJ/bit, 9.8 µm Fine-Pitch Dielet-to-Dielet Links for Advanced Packaging using Silicon Interconnect Fabric," 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2022, pp. 2104-2110, doi: 10.1109/ECTC51906.2022.00332.
48. K. Sahoo, H. Ren and S. S. Iyer, "A High Throughput Two-Stage Die-to-Wafer Thermal Compression Bonding Scheme for Heterogeneous Integration," *2023 IEEE 73rd Electronic Components and Technology Conference (ECTC)*, Orlando, FL, USA, 2023, pp. 362-366, doi: 10.1109/ECTC51909.2023.00067.
49. B. Haba, "Die to Wafer/Die DBI Hybrid Bonding for a True 3D Interconnect," in 2019 6th International Workshop on Low Temperature Bonding for 3D Integration (LTB-3D), May 2019, pp. 18–18. doi: 10.23919/LTB-3D.2019.8735218.
50. Y. H. Chen et al., "Ultra High Density SoIC with Sub-micron Bond Pitch," in 2020 IEEE 70th Electronic Components and Technology Conference (ECTC), Jun. 2020, pp. 576–581. doi: 10.1109/ECTC32862.2020.00096.
51. Adeel A. Bajwa, SivaChandra Jangam, Saptadeep Pal, Niteesh Marathe, Tingyu Bai, Takafumi Fukushima, Mark Goorsky, Subramanian S. Iyer, "Heterogeneous Integration at Fine Pitch 10 µm) using Thermal Compression Bonding", Proc. ECTC 2017, pp. 1276-1283.
52. Eric Beyne, Soon-Wook Kim, Lan Peng, Nancy Heylen, Joke De Messemaeker, Oguzhan Orkut Okudur, Alain Phommahaxay, Tae-Gon Kim, Michele Stucchi, Dimitrios Velenis, Andy Miller, and Gerald Beyer imec, Leuven, Belgium, "Scalable, sub 2µm Pitch, Cu/SiCN to Cu/SiCN Hybrid Wafer-to-Wafer Bonding Technology, IEDM Tech. Dig., 2017, pp.729-732.
53. G. Gao et al., "Scaling Package Interconnects below 20mm pitch with hybrid bonding," 2018 IEEE 68th Electronic Components and Technology Conference (ECTC), San Diego, CA, 2018, pp. 314-322.
54. T. Uhrmann, J. Burggraf, M. Pires, "Collective D2W Hybrid Bonding for 3D SIC and Heterogeneous Integration," IMAPS DPC, March 5th 2020, www.imapsource.org

55. L. Mirkarimi, “Hybrid Bonding: Fueling Advanced Memory and High-Performance Compute Roadmaps,” IMAPS 2020.
56. S. Suhard et al., "Demonstration of a collective hybrid die-to-wafer integration," 2020 IEEE 70th Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2020, pp. 1315-1321, doi: 10.1109/ECTC32862.2020.00208.
57. J. H. Lau, "Recent Advances and Trends in Cu–Cu Hybrid Bonding," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 13, no. 3, pp. 399-425, March 2023, doi: 10.1109/TCPMT.2023.3265529.
58. J. H. Lau, "Recent Advances and Trends in Multiple System and Heterogeneous Integration With TSV-Less Interposers," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 12, no. 8, pp. 1271-1281, Aug. 2022, doi: 10.1109/TCPMT.2022.3194374.
59. Sergey Y. Shumarayev, Conor O’Keeffe, Tim T. Hoang, David Kehlet, Sangeeta Raman, Benjamin Esposito, A SiP Standard for Reusable Chiplet Enabled Platforms, GOMACTech Conference, March 25-28, 2019 - Albuquerque, NM, http://www.gomactech.net/.
60. https://github.com/chipsalliance/AIB-specification
61. https://www.eetimes.com/intel-shows-next-steps-in-packaging/#
62. M. Lin, et al, “A 7nm 4GHz Arm-core-based CoWoS chiplet design for high performance computing”, VLSI Symp., Kyoto, Japan, June 9-14, 2019
63. S. S. Iyer, "Chips, Dies, Chiplets and Dielets and Heterogeneous Integration," 2022 6th IEEE Electron Devices Technology & Manufacturing Conference (EDTM), Oita, Japan, 2022, pp. 8-11, doi: 10.1109/EDTM53872.2022.9798163.
64. D. Das Sharma, G. Pasdast, Z. Qian and K. Aygun, "Universal Chiplet Interconnect Express (UCIe): An Open Industry Standard for Innovations With Chiplets at Package Level," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 12, no. 9, pp. 1423-1431, Sept. 2022, doi: 10.1109/TCPMT.2022.3207195.
65. D. D. Sharma, "System on a Package Innovations With Universal Chiplet Interconnect Express (UCIe) Interconnect," in IEEE Micro, vol. 43, no. 2, pp. 76-85, 1 March-April 2023, doi: 10.1109/MM.2023.3235770.
66. R. Farjadrad, M. Kuemerle and B. Vinnakota, "A Bunch-of-Wires (BoW) Interface for Interchiplet Communication," in IEEE Micro, vol. 40, no. 1, pp. 15-24, 1 Jan.-Feb. 2020, doi: 10.1109/MM.2019.2950352.
67. R. Krishna et al., "Signal and Power Integrity Design and Analysis for Bunch-of-Wires (BoW) Interface for Chiplet Integration on Advanced Packaging," 2023 IEEE 73rd Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2023, pp. 1004-1011, doi: 10.1109/ECTC51909.2023.00171.
68. High-performance, power-efficient three-dimensional system-in-package designs with universal chiplet interconnect express | Research Communities by Springer Nature
69. High-performance, power-efficient three-dimensional system-in-package designs with universal chiplet interconnect express | Research Communities by Springer Nature
70. S. Jangam, A. A. Bajwa, K. K. Thankkappan, P. Kittur and S. S. Iyer, "Electrical Characterization of High Performance Fine Pitch Interconnects in Silicon-Interconnect Fabric," 2018 IEEE 68th Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2018, pp. 1283-1288, doi: 10.1109/ECTC.2018.00197.
71. K. Sahoo, B. Vinnakota, S. Ardalan and S. S. Iyer, "Co-optimizing signaling protocol with semiconductor and packaging technology," *2021 IEEE 30th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)*, Austin, TX, USA, 2021, pp. 1-3, doi: 10.1109/EPEPS51341.2021.9609161.
72. G, Refai-Ahmed, H. Wang, S, Ramalingam, N. Karunakaran, K. Pan, S.B. Park, A. Soundarajan, S. Kanaran, C. Chung and Y. L. Huang, ``Lidless and lidded Flip Chip Packages for Advanced Applications'', 978-1-7281-8911-6/20, 2020 IEEE 22nd Electronics Packaging Technology Conference (EPTC), IEEE.