IEEE Transactions on Components, Packaging and Manufacturing Technology

Special Section Call for Papers

"Advances in Heterogeneous Integration for Neuromorphic Computing"

Artificial intelligence (AI) is currently in its third wave of development, while the traditional von Neumann architecture faces challenges in highly parallel computing, energy efficiency, and ultra-low power consumption. **Neuromorphic computing** provides a solution by mimicking the structure and functions of the human brain to potentially overcome the limitations of traditional computer architecture and enhance the computing capabilities for AI tasks. The human brain demonstrates remarkable efficiency, with over 100 billion neurons and approximately 100 trillion synapses, all while consuming only about 20 Watts of power. Replicating this biological marvel in hardware involves numerous different components (sensors, memory, computing, communication macros) and various technologies (PCM, RRAM, different technology nodes, analog/digital designs). Heterogeneous integration provides the opportunity to integrate various functionalities into neuromorphic computing systems.

This Special Section will focus on neuromorphic computing systems by providing space for cutting edge research addressing challenges, opportunities, and trends in their modeling, measurement, and design. **We encourage all techniques and applications within the realm of neuromorphic computing systems, encompassing materials, devices, circuits, packaging, and their electrical, thermal, and reliability performance.** Suggested areas include the development and evolution of

A. Novel intelligent materials and devices, along with integration techniques at the device level for neuromorphic computing.
B. Advanced analog, digital, and mixed-signal circuits, and architectures to achieve high-performance neuromorphic computing applications.
C. Novel system integration techniques for neuromorphic computing, focusing on advanced 2.5D and 3D packaging technologies.
D. Techniques addressing electrical, thermal, and reliability challenges, such as I/O routing, heat dissipation, and signal and power delivery as they pertain to neuromorphic systems.
E. Co-design approaches across multiple disciplines, spanning materials, devices, circuits, architectures, and integration, for neuromorphic chips.

Paper submission deadline: **August 31, 2024.**

Final manuscripts due: January 31, 2025.

Planned publication date: **May 2025.**

On-line submission procedure for the authors: Authors should use the IEEE T-CPMT Author Portal to submit the manuscripts and **select "Special Section on Neuromorphic Computing" when submitting the papers**. Please note the same in the cover letter to ensure that the manuscript is assigned correctly. All papers are to conform to IEEE TCPMT Guidelines.

Guest Editors:

Prof. Hanzhi Ma
Zhejiang University, Hangzhou, China
mahanzhi@zju.edu.cn

Prof. Shaloo Rakheja
University of Illinois Urbana-Champaign, USA
rakheja@illinois.edu