Co-Design for Chiplets at EPEPS 2022

The special session "**Co-Design for Chiplets**" was held during the 31st Conference on Electrical Performance of Electronic Packaging and Systems at the San Jose Marriot Hotel on October 10, 2022.

Heterogeneous integration (HI) is bringing a revolutionary change rather than an evolutionary one. The electronic design automation (EDA) will need to undergo transformational changes to manage these new challenges and simple incremental changes to their existing infrastructure may not be sufficient. To address these concerns and others related to HI, several visionaries from industry presented their perspectives at the panel session.

Prith Banerjee, chief technology officer at Ansys, presented his talk entitled "*Future of Simulation Driven Innovation in Nanotechnology*". He reviewed 50 years of innovation in electronics and how they were influenced and supported by design automation. Simulation is at the core of virtual prototyping and its role can only increase with the growing trends in system complexity.

John Park, product management group director at Cadence Design Systems presented his talk on "*When Chips Become Systems; The Challenges of Designing Advanced 2.5D and 3D Packages*". He defined the multi-chiplet 3D ecosystem challenges. He predicted that heterogenous integration will leverage multiple packaging technologies with complex design flows and discussed the advent of ADK's (assembly design kits) in addition to PDKs (process design kits). There is a need for a common platform for co-design/co-analysis of the system level design. Finally he touched upon capacity and performance impact on tools and support of existing and emerging 3DHI standards.

The third presentation was by Nithya Sankaran, principal engineer at NVIDIA. In her talk on "*Chiplet Based Designs: An SI/PI Perspective*", she addressed interface connectivity across chiplets and the impact on SI. Other technical aspects included channel impedance optimization, power delivery network (PDN) design and power supply arrangement on platforms. She discussed signal and power integrity evaluation for chiplet based designs and the trade-offs involved across different SI parameters vs. interface layout constraints. She recognized that many of the existing approaches for channel SI and PDN are applicable for chiplet based analysis. Some requirements need adapting the current methodologies to chiplet based designs. Her observation is that more interesting and unique requirements/challenges could be on the roadmap for chiplet based designs.

The fourth presentation was by Bapi Vinnakota, Project Lead for ODSA entitled "*An Open interface for Die Disaggregation*". Bapi gave a perspective on the chiplet marketplace. The vision is to integrate best-in-class chiplets from multiple vendors through open interfaces. His talk next touched upon the bunch of wire (BoW) standard and emphasized on its key attributes for economies of scale as a specification optimized for maximum applicability. He believes that in order to support the CHIPS act, there is a need to translate the HIR blueprint for on-shore manufacturing that can drive materials, equipment, manufacturing with a trained workforce in the USA.

The presentations were followed by a panel session which was joined in addition by Ravi Agarwal, of the Infrastructure Group at META. The panel was moderated by Jose Schutt-Aine and

entertained several questions from the audience. The panel members recognized that in order to develop and improve the chiplet design ecosystem, discussions such as those in the panel session must continue in order to engage researchers in academia and industry.

Panel members. From left to right: Ravi Agarwal, Bapi Vinnakota, Jose Schutt-Aine, John Park, Nythia Sankaran, Prith Banerjee.