

The IEEE EPS Packaging Benchmark Suite

Committee Members:

Heidi Barnes, Vladimir Okhmatovski, Kemal Aygün, Alexander Pelger, Ali Yilmaz, Jonatan Aronsson, Yan Fen Shen, Stefano Grivet-Talocia, Jose Schutt-Aine, Kaisheng(Klaus) Hu, Benjamin Silva, Wui-Weng Wong, Tingdong Zhou, Dale Becker, Michael J. Hill, Elmar Griese, Pavel Roy Paladhi, Feng Ling, Rohit Sharma, Fei Guo, Evan Fledell, Thomas Michael Winkel, Jose A. Hejase, Chang Liu,

Affiliations:

Keysight Technologies, University of Manitoba, Intel, IBM, Univ. of Texas at Austin, CEM Works, Politecnico di Torino, Univ. Illinois Urbana-Champaign, Ciena, AMD, NXP, University of Siegen, Xpeedic, Indian Institute of Tech. Ropar, Nvidia, Cadence

I. INTRODUCTION

The remarkable advances in computational science and engineering (CSE) fueled in part by the persistent increases in the capabilities of computer hardware and software have produced a large and expanding set of computational methods to quantify the electrical performance of electronic packages. Methods such as FEM, MoM, PEEC, FDTD etc. are available through various commercial, academic, freeware, and proprietary simulation tools and continue to be developed, refined, marketed, and applied to the electromagnetic analysis and design of packages. While these tools advance, the expectations from these simulation tools continue to escalate partly because the requirements from and complexity of electronic packages continue to increase. Recognizing

- the importance of simulation tools and computational methods to the development of electronic packages,
- the necessity of verification, validation, and objective comparison to the proper use and further advancement of these tools and methods,
- the obstacles that potential and actual users, developers, and researchers of such tools and methods encounter, and
- the dearth of benchmarks to evaluate the performance of existing and novel tools and methods,

the IEEE Electrical Packaging Society (EPS) technical committee on electrical design, modeling, and simulation (TC-EDMS) initiated a joint industrial-academic effort in late 2018 to assemble a set of modern benchmarks. This article reviews the goals of this effort, and the current state of the Packaging Benchmark Suite.

II. SCIENTIFIC BENCHMARKS AND BENCHMARKING

The Merriam-Webster dictionary defines *benchmark* as “a standardized problem or test that serves as a basis for evaluation or comparison”. In science and engineering, *benchmarking* something of interest is to subject it to a process that invites the participants to collect specific data (using benchmarks), identify similarities and differences relative to reference data, make

objective comparisons, and deduce facts about the thing of interest. This process has all the hallmarks of the scientific method and requires the release of sufficient information to (present and future) scientists and engineers to independently and empirically corroborate, reproduce, vary, replicate, or repeat it [1], ultimately enabling them to verify or falsify the deductions and claims of others. Benchmarks and the benchmarking they enable “have a lasting positive impact on a scientific discipline” when they “emerge through a synergistic process of technical knowledge and social consensus proceeding in tandem” [2].

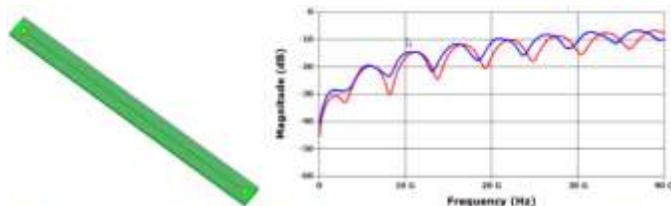
Physical benchmarks serve numerous purposes in measurement campaigns; they are used to, e.g., calibrate equipment, train personnel, verify protocols, or quantify measurement uncertainties. Physical benchmarks—*together with their digital models/ representations*—are used in CSE to also compare different theoretical/computational methods (particularly in terms of their predictive power, accuracy, and cost), reveal their strengths and weaknesses, and provide information for their appropriate use and further development [3]. Compared to typical case studies used in publications to test simulation tools and computational methods, benchmarks must include significantly more information and clear a higher bar of precision, reliability, and independent reproducibility.

The mission of the Packaging Benchmarks Committee is to produce a Packaging Benchmark Suite that will encourage research & development by providing information about the electromagnetic, electrical, and circuit modeling and simulation problems encountered, and the state-of-the-art solution methods used when analyzing and designing electronic packages.

III. STATE OF THE SUITE

As of Oct. 2022, the Packaging Benchmarks Committee elevated 4 benchmarks into the Suite and are available to the public on the website <http://www.packaging-benchmarks.org> [4]. The site requires a simple sign-up and encourages users to publish on the results of using the benchmarks to further the state of the art for EM simulation tools and computational methods for electronic packaging. A summary of each of the benchmarks is listed below.

A. Benchmark I: Single-ended Microstrip Transmission Line



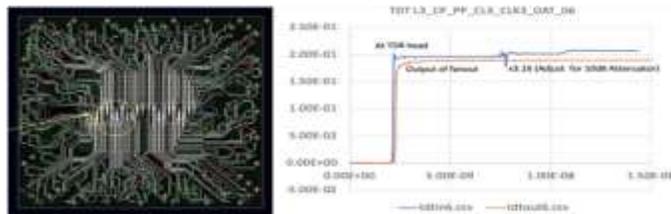
I. Single-ended Microstrip Transmission Line (version 1.0)

Single-ended Microstrip Transmission Line Benchmark Problem

Benchmark I contains measurements and representative modeling data for a microstrip package transmission line test structure. Over the last decade, this particular problem has been shared with various research groups as a test example; e.g., see [5],[6]. This is a *basic* benchmark that can serve as a suitable entry problem for CSE researchers new to the area of electronic packaging. Furthermore, even though the physical structure is relatively simple by today’s EDMS standards, i.e., “a single package transmission line”, an accurate electromagnetic analysis of it requires tackling some of the fundamental ingredients common to many other packaging problems. These include multiple lossy dielectric layers with different electrical properties, metal layers with finite thicknesses and rough surfaces, and vias. As a result, the Committee decided that this test structure would make a good first benchmark for the Packaging Benchmark Suite.

One somewhat inevitable shortcoming of using an older example is the inability to collect additional data and perform additional experiments as the physical measurement parts are no longer available. Some of the recent EDMS research has focused on systematic measurement and modeling uncertainty quantification to improve the overall measurement-to-modeling correlation process [7]. This, together with the frequency range of interest (currently limited to 40 GHz), are two potential areas of improvement that can be addressed by a future benchmark submission.

B. Benchmark II: Plasma Package



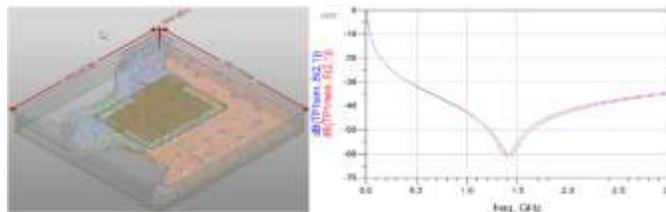
II. Plasma Package (version 1.0)

Plasma Package Benchmark Problem

Plasma is the name given to an eight-metal-layer laminate substrate in a so-called 3-2-3 construction which has three build-up layers on top and bottom of a two-metal-layer core. Plasma is a fully wired design that was originally offered as a challenge problem for an EPEP 2006 special session [8] because the design data volume was beyond the capability of computer resources available at that time. Benchmark II provides the full Plasma design file and identifies four traces for extraction and time-domain simulation that includes the full path of pads, vias, traces, and the reference return paths from the pad on the top for

die attach to the pads on the bottom for BGA attach. The time domain measured waveforms of reflection and transmission delay of a trace are provided along with the near-end and far-end crosstalk observed from three adjacent traces. This gives a benchmark problem for modeling these quantities in an actual design.

C. Benchmark III: Power-Integrity Test Package

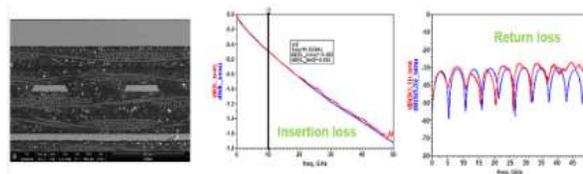


III. Power-Integrity Test Package (version 1.0)

Package Power Integrity Benchmarking Problem

Benchmark III is about impedance characterization and modeling of a power plane VDD and return ground plane VSS test structure in a flip chip package. Transfer impedance converted from S-parameters collected using conventional 2-port shunt through characterization is introduced on this test structure with thousands of power and ground bumps. Qualitatively good correlation between simulation and measurement data has sufficiently validated the models. The developed models utilize realistic dimensions from cross-sectional analysis along with the removal of residual measurement parasitics.

D. Benchmark IV: PCB Laminate Parameter Extraction for Simulation



IV. PCB Laminate Parameter Extraction for Simulation (version 1.0)

PCB Laminate Parameter Extraction for Simulation Benchmark Problem

Benchmark IV is about characterizing the transmission line interface from a host PCB to an electronic package. PCB material parameters (Dk, Df and surface roughness) are key factors for RF and signal integrity analysis. By using the parameters within vendor’s datasheets directly, the simulation result always has a big offset compared with lab measurement results due to different manufacturing variations. To improve the accuracy of simulation and guarantee a design to be successful for the first-time, a test coupon board is designed, fabricated, and measured for the purpose of improving the accuracy of the material parameters for simulation.

The measurement results for the test coupon single ended (S/E) and differential (Diff.) striplines are provided as a benchmark. Simulation results with industrial EDA tool are provided as reference. The user is expected to extract PCB laminate parameters of Dk, Df and surface roughness with their own method, based on the lab measurements of S parameters

and SEM cross-sections. With the extracted parameters and same stack up, the user is encouraged to run simulation with their own tool and verify the simulation accuracy up to 50 GHz by comparing with the lab measurement result.

IV. CONCLUSION AND FUTURE WORK

The joint industrial-academic effort initiated by the IEEE EPS TC-EDMS has attracted a large number of expert volunteers, who have formed the Packaging Benchmarks Committee and collaborated over the last four years to establish and publicly release a modern Packaging Benchmark Suite [9]. The committee continues to develop the Suite, which currently consists of 4 publicly available benchmarks.

Various scientists and engineers, including some of the committee members, have already started using the benchmarks in the Suite to evaluate existing simulation tools and support the development of novel computational methods for electronic packaging. The Packaging Benchmark Suite is expected to advance scientific benchmarking of simulation tools and computational methods and ultimately lead to advances in CSE and EDMS of electronic packages.

The Packaging Benchmark Committee encourages both academia and industry to participate in the use of the benchmarks by registering on the www.packaging-benchmarks.org website. The IEEE EPS sponsored conferences SPI, EPEPS, and EDAPS are all interested in submissions that utilize these benchmarks to further the state of the industry for simulation tools and computational methods.

REFERENCES

- [1] D. G. Feitelson, "From repeatability to reproducibility and corroboration," *ACM SIGOPS Oper. Sys. Rev.*, vol. 49, no. 1, pp. 3-11, Jan. 2015.
- [2] S. E. Sim, S. Easterbrook, and R. C. Holt, "Using benchmarking to advance research: A challenge to software engineering," in *Proc. IEEE 25th Int. Conf. Software Eng.*, pp. 74-83, May 2003.
- [3] J. W. Massey, C. Liu, and A. E. Yilmaz, "Benchmarking to close the credibility gap: A computational bioEM benchmark suite," in *Proc. URSI Int. Symp. Electromagn. Theory (EMTS)*, Aug. 2016.
- [4] IEEE EPS TC-EDMS Packaging Benchmark Suite, 2021. [Online]. Available: <https://packaging-benchmarks.org>
- [5] C. Liu, K. Aygün, and A. E. Yilmaz, "A parallel FFT-accelerated layered-medium integral equation solver for electronic packages," *Int. J. Num. Model.: Electron. Net., Devices Fields*, vol. 33, no. 2, Mar./Apr. 2020.
- [6] B. Zhou, H. Liu, and D. Jiao, "A direct finite element solver of linear complexity for large-scale 3-d circuit extraction in multiple dielectrics," in *Proc. 50th Design Automation Conf. (DAC)*, June 2013.
- [7] C. S. Geyik *et al.*, "Measurement uncertainty propagation in the validation of high-speed interconnects," in *Proc. IEEE EPEPS*, Oct. 2020.
- [8] Special Session, 2006 IEEE Electrical Performance of Electronic Packaging, 2006, pp. 286-310.
- [9] F. Guo, A. Yilmaz, *et al.* "The IEEE EPS Packaging Benchmark Suite" IEEE EPEPS Conference, Oct. 2021.