Reliability Concerns in Through Silicon Via based 3D Integration: Fabrication to Packaging

Maya Chandrakar[1], Kamal Solanki[1], Manoj Kumar Majumder[1] and Rohit Sharma[2, 3]

[1]International Institute of Information Technology, Naya Raipur, CG, 493661
[2]Department of Electrical Engineering, Indian Institute of Technology Ropar, Rupnagar, PB, 140001
[3]School of Electrical Engineering and Computer Science, Pennsylvania State University, University Park, PA, 16801

***Abstract*—Chips are converted into reliable electronic devices through the process of electronic packaging throughout the process of electronics fabrication. 3D electronic packaging architectures with heterogeneous integration techniques have witnessed considerable demand as package density and functional diversity have increased. Despite the new architectural possibilities and enhanced performance offered by 3D integration, signal integrity and reliability problems still exist since packaging systems usually exhibit geometric discontinuities due to through silicon vias (TSVs), free edges, and multiple interfaces. Hence, manufacturing of high quality and reliable TSVs was and will remain a major enabler for the adoption of new 3D packaging technologies. TSV faults must be screened promptly during the manufacturing process because they could cause critical challenges during the initial phases of fabrication. Consequently, the mechanical stress and chip-package interaction are addressed as being major threats for 3D TSV IC failures. The emergence of various defects in 3D TSV ICs from fabrication to packaging is outlined and discussed in this article. Also, several defect mechanisms and fault structures causing unstable package performance and impaired device reliability are explained.**

***Index Terms*—Coefficient of Thermal Expansion (CTE), Electromigration (EM), Redistribution Layer (RDL), Through Silicon Via (TSV), Three-Dimensional Integrated Circuit (3D IC).**

I. Introduction

TO cater with the growing demand for the miniaturization of electronic devices, the trend in the semiconductor industry is progressively transitioning from two (2D) to three dimensional (3D) packaging constructions for integrated circuits. The research and prototyping of revolutionary 3D electronic packaging are receiving a lot of attention in order to facilitate higher packaging density, functional diversity and provide new opportunities for present and future applications. Compared to earlier packaging methods, the features of through silicon via (TSV) based 3D packaging technology include a small aperture, fine pitch, and a significant aspect ratio [1]. Besides the benefits and prospects of 3D integration, the reliability issue due to unstable fabrication process is a key concern. Defects potentially originate at the TSV or in the entire 3D integrated circuit (IC) package during the various steps of manufacturing and packaging of ICs. These faults can induce many problems, particularly inconsistent package performance, and impaired product reliability. Defects can arise from unique processing steps of TSV-based 3D IC packaging such as TSV formation, via filling, wafer thinning, and die stacking [2]. However, the electrical failures are likely to become more prevalent in 3D ICs as interconnection density scales up gen-over-gen. Moreover, the via assembly can undergo electromigration (EM), temperature changes, and mechanical stress because of the ageing effects, that can cause more instability [3]. Some of the faults in TSVs are unavoidably induced by the intricate and immature fabrication and packaging procedures. The probable defects (as delineated in Fig. 1) during the fabrication process can impede the technology for further advancement that primarily includes the formation of voids in TSVs and bumps that emerge by improper etching and filling, inadequate sidewall coverage of the various layers, and impurities in soldering powder [4] as shown in Fig. 1(a). It further incorporates the crack formation due to poor vapor deposition technique and mechanical loadings [5] as illustrated in Fig. 1(b). After liner deposition, the formation of pinholes occurs in the liner owing to differences in the thermal expansion coefficients (CTE) of the copper (Cu), liner and silicon (Si) substrate, irregular liner deposition and contaminants [6] as shown in Fig. 1(c). Proceeding to packaging procedures, a probability of occurrence of numerous imperfections such as short defects between bumps and redistribution layers (RDLs) are normally carried by the physical press during the stacking and fine-pitch interconnection processes [7] as depicted in Fig. 1(d). It further includes leakage shorts between the coupled TSVs due to an ineffective removal of seed layer [8], disconnection failures in a 3D package with multi-stacked chips due to deformed or missing bumps and thermal stress problems [7] as demonstrated in Fig. 1(e). Additionally, the misaligned chips due to the usage of a reducing agent, non-uniformity of bump size, and oxidation of the bottom-side surface of TSVs or bumps [9] may add to the process of imperfections, as presented in Fig. 1(f). Furthermore, an interfacial crack formed by an undesirable stress during the die stacking [10] (Fig. 1(g)), diffusion of Cu over the liner and the Si due to large CTE mismatch can lead to the degradation of the RDLs [11] as shown in Fig. 1(h). The failures enumerated above can emerge concurrently with a significant impact on one another. These deformations predominantly impact the electrical continuity (open and short circuits, higher resistance, parasitic effects), insulation, and structural rigidity of the TSV structure, which adversely impacts the 3D package reliability. Even though recent research has improved the effectiveness of TSV assessment, it may still be necessary to develop new strategies that perform more effectively in terms of fault

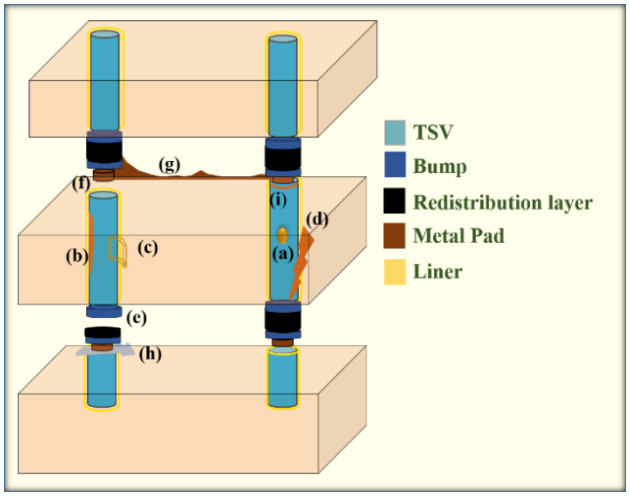


Fig. 1. Different TSV defect types (a) Air void, (b) Interfacial crack, (c) Pinhole fault, (d) Short defect b/w fine-pitched bumps, (e) Disconnection b/w bump & die, (f) Open defect b/w TSV & metal via in a 3D TSV package, (g) Delamination extending into liner & Si substrate, (h) Cu pumping, (i) Circumferential crack.

coverage, area overhead, and test application time. However, accurate fault models need to be developed by considering an exact shape, size, and fault location, as these defects can occur at any arbitrary location with irregular dimensions. Thus, TSV testing is vital since a single TSV failure can result in the complete failure of 3D stacked IC. Consequently, to prevent severe degradation and ensure proper functioning, the utilization of redundant TSVs to replace faulty ones is the most effective solution [12]. Moreover, early manufacturing stages [4-11] place a strong emphasis on reliability assessments to avoid expensive target system redesigns. The reliability and feasibility of TSVs are significantly impacted by the diverse variety of via-related faults. Therefore, a thorough investigation of via is still required to examine the aforementioned manufacturing and packaging related defects. In light of this, the article provides a review of the emergence, impact, and solutions for overcoming numerous defect mechanisms to lessen the failure of the entire 3D TSV IC package. Additionally, the significance of mechanical stress and immature fabrication/packaging processes as a main threat for failures in 3D technology is emphasized.

II. Defect Mechanisms: Fabrication To Packaging

This section provides a thorough analysis of the numerous manufacturing and packaging stages, in addition to all the fabrication strategies adopted to fabricate the TSVs on a Si wafer. A comprehensive analysis of the anticipated faults that can arise during the fabrication to packaging processes is provided. Firstly, to design and fabricate a TSV, it is essential to integrate and optimize the entire manufacturing sequence that includes the conventional steps involved in both back-end (BE) packaging and wafer processing [13]. After adopting this integrated approach, the performance of the TSV can be maximized in terms of yield and reliability.

Before filling the TSV material, it is required to create a deep trench in the silicon that demonstrates an extremely high aspect ratio. This procedure can be accomplished using a specialized method known as highly anisotropic deep reactive ion etching (DRIE) that employs Sulphur hexafluoride (SF_6) gas [14]. Thereafter, operating octafluorocyclobutane (C_4F_8) gas at a high velocity of 10 μm/min, a sidewall passivation step is accomplished. Concurrently, plasma enhanced chemical vapor deposition (PECVD) is employed to develop the isolating layer, enabling a strong adhesion with the barrier layer material [15]. Subsequently, the barrier layer is deposited using physical vapor deposition (PVD) process that enables consistent step coverage [16]. The seed layer acts as a nucleation site for the subsequent deposition of Cu metal. The barrier and seed layers serve the purpose of preventing the diffusion of Cu into the oxide layer.

In addition, the manufacturing of TSVs involves usage of the via-first, via-middle, and via-last design techniques [17]. Figure 2(a) presents a detailed fabrication step of via-last that permits the placement of TSVs on a silicon wafer after the fabrication of other components, provides a higher yield, greater flexibility, and a high aspect ratio with regard to positioning and design rule. Moreover, this process includes high temperature fabrication techniques at the front-end (FE) and back-end (BE) stages before the TSV formation as shown in steps (i) and (ii) of Fig. 2(a). Consequently, the wafer is thinned using a back grinding process, followed by etching that creates a groove on the surface of the silicon material, as shown in steps (iii) and (iv) of Fig. 2(a). After completing the etching process [18], a barrier and seed layer is deposited to ensure the protection of the metal layer. Subsequently, Cu can be used as the filler material due to its low resistivity, as depicted in step (v) of Fig. 2(a).

The locations of commonly found defects from fabrication to packaging are presented in Figs. 2(b) and 2(c), respectively. A void refers to a defect that occurs due to EM induced cavities in via metal or insulating material of a 3D TSV assembly, as depicted in step (vi) of Fig. 2(c). It can be caused by a variety of factors, including improper deposition, or etching of TSV materials and inadequate copper filling speed or cleaning processes used during fabrication [9]. Similarly, delamination in TSVs can occur due to the CTE mismatch and poor adhesion between the different materials, and mechanical stress during various processing as illustrated in step (vii) of Fig. 2(c). Whereas a pinhole defect refers to a small hole or opening in the TSV structure that extends towards the Si substrate illustrated in step (viii) of Fig. 2(c). It can emerge during the lithography or improper Chemical Mechanical Planarization (CMP) process. Subsequently, during packaging process, the short and open effects in TSV devices are two major kinds of electrical faults that can influence the performance and reliability of the device presented in steps (ix) and (x) of Fig. 2(c). A short defect occurs due to a variety of reasons, such as incomplete etching or filling of TSVs, contamination during the TSV manufacturing process, or issues with the isolation materials used to separate the TSVs from other metal layers in the chip. Likewise, an open defect results in a breakage or discontinuity in a conductive path, air cracks or non-uniform bump sizes resulting in attenuation or even complete distortion of the TSV signals. The impact of immature fabrication and packaging processes are demonstrated in the following subsections.

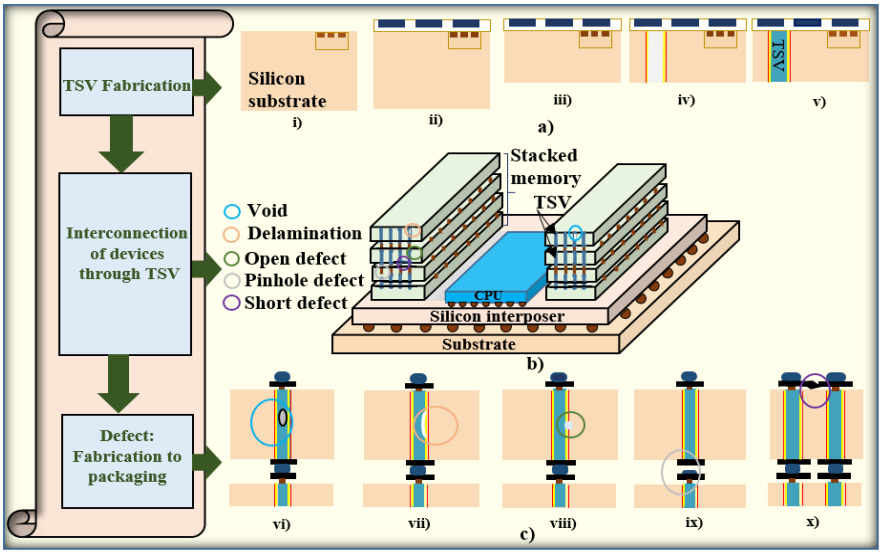


Fig. 2. (a). TSV fabrication steps in via-last method (i) front-end process (transistors), (ii) back-end process (metallization layers), (iii) wafer thinning, (iv) etching, insulating layer, and barrier layer deposition, and (v) TSV fill, (b) Interconnection of devices through TSV, (c) Defects arises during fabrication of packaging (i) Void formation, (ii) Interfacial delamination, (iii) Pinhole defect, (iv)Open defect, and (v) Short defect.

A) Impact of Fabrication:

The impacts of several open/short failure mechanisms that originate in the electroplated copper, dielectric, barrier layers, and bumps during their fabrication processes are classified as:

1) Voids in TSVs and Bumps:

Depending on the level of severity of the defect, the micro-voids may cause a slight delay to resistive opening through the defective TSV/bump or infrequently, these can allow the holes to expand and result in a disconnected TSVs or bumps. It also causes the impedance to an abrupt change in the range of (0.596-27.061 Ω) and leads to a partial reflection of the transmitted signals. Moreover, a capacitor is formed by the air dielectric and the nearby Cu metal that raises by almost 2.62% of the transmitted signal retardation while consuming an additional power of 0.39% [4].

2) Delamination and Cracks:

Thermal stress within and around TSVs has the potential to cause cohesive cracks in silicon substrates as well as interfacial delamination/cracks between the TSV and the liners. Functional failures owing to leakage, attenuation, or even complete distortion of the TSV transmission signal (V_{peak}/V_{rms} = 4.13 to 5.82), poor consistency of liners and barriers, and other potential consequence of a TSV interfacial crack along with the problems regarding mechanical reliability such as an energy release rate of 0.3-0.9 J/m^2 [10].

3) Pinhole defect:

Pinhole formation results in an undesired leakage current flow between the TSV and the Si substrate that lowers the breakdown voltage and raises the possibility of a resistive short (as large as 17.5 MΩ at h_{pin}=0.5 μm) [6]. In addition to an increasing power consumption and self- heating of the device, the associated leakage current also worsens the operational capability and potentiality of the device resulting in malfunction.

4) Cu pumping:

Electrical failures primarily occur as Cu diffuses to the silicon substrate through the insulating and barrier layers. Cu is plastically deformed at high temperatures that may cause Cu pumping. However, due to the removal of plastically deformed Cu, the reduction in Cu expansion in the range of (50.3-20.4 nm) can be observed while increasing post-anneal temperature (100-400℃) [11]. Additionally, it also affects the reliability and integrity of the Back End of Line (BEOL) structures above the TSV during later fabrication process.

B) Impact of Packaging:

Considering the unstable packaging processes, this subsection presents an in-depth analysis of various kinds of defects related to an entire 3D TSV assembly. Progressing forward with packaging processes to build a complete 3D TSV package, several other probable defects are summarized in the packaging as follows:

1) Disconnection Failure:

Disconnection failures are caused by impurities between the TSV and the micro bump or between adjacent micro-bumps that increases the *RC* parasitics and delay. The signal transmission across the appropriate TSVs might be unavailable if one or more bumps are much smaller than the anticipated. Such malfunctions lead to a substantial degradation in chip performance with an increased voltage spike ranging from 0-500 mV [6].

2) Misalignment of TSV, Bump, and Contact Pad:

The partially aligned TSV-bump leads to high contact

TABLE 1 EMERGENCE AND EFFECTS OF VARIOUS DEFECT MECHANISMS

Defect	Location of Occurrence	Reasons of Failure	Expected Failure	During Fabrication	During Packaging	Effects of Failure
Micro-void/ Underfillings [4]	TSV and bumps	EM, poor layer deposition, incomplete fills	Resistive open	√	√	Ineffective signal transmission, more Impedance
Interfacial Delamination and Cracks [5], [10]	TSV metal, Si substrate, liner & barrier layers, and (RDLs)	CTE mismatch, improper etching, nonuniform bump size	Open faults	√	√	Signal attenuation, poor consistency of liners and barriers
Disconnection between multi-stacked chips [9]	Between TSV and bump, two dies	Nonuniform bump size, oxidation of TSVs or bumps, loading temperature, reducing agent	Increased contact resistance	√	√	Degradation in chip Performance
Pinhole [6]	Liner layer	CTE mismatch, impure liner, ineffective seed layer Removal	Resistive shorts and leakages	√	√	Undesirable leakage current, breakdown voltage, signal attenuation
Cu diffusion [11]	Across the barrier & liner layers to the Si substrate	Large CTE mismatch b/w Cu and Si, current crowding, EM	Shorts and leakages	√		Electrical failures
EM-induced defects [4]	TSV and bumps	TSV geometries, mechanical stress, more current density	Resistive opens and shorts		√	Voids and hillocks in TSVs
Short defects [7],[8]	RDLs and bumps	Fine-pitch interconnections, non-uniform bump sizes	Shorts and leakages		√	Undesired electrical paths, low impedance value

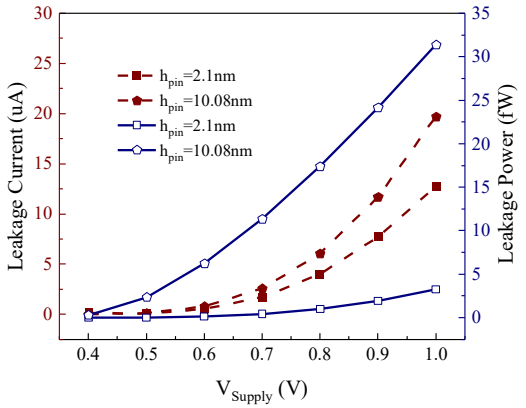
resistance ranging from 107 kΩ to infinite of the TSV-bump network [9]; transmission across the appropriate TSVs might be unavailable if one or more bumps are much smaller than the anticipated. Such malfunctions lead to a substantial degradation in chip performance with an increased voltage spike ranging from 0-500 mV [6].

3) Electromigration:

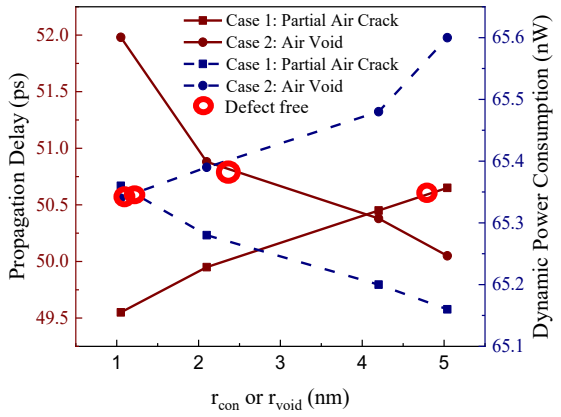
Electromigration has an impact on the micro-bumps and vertical interconnect links among silicon layers that results in an open link or a disconnected channel. Additionally, by forming voids and hillocks in vias and bumps, it changes the intended connectivity of components. Moreover, it may result in short failure by expediting the dissolution of Cu into solder. The various failure mechanisms outlined in TABLE-I impact one another and possibly emerge concurrently rather than individually. Owing to the feasibility and reliability concerns of the above-mentioned failure mechanisms, the defect analysis considering via electrical performance is represented in the subsequent section.

III. DEFECT ANALYSIS

This section examines a comparative analysis of propagation delay, leakage current, and power consumption of open (partial air crack with a cylindrical connector and air void) and short (pinhole) defects. Considering a CNTFET driven driver-via load (DVL) setup at 7 nm technology with the via height (h_{TSV}) of 30 nm, Figs. 3(a) and 3(b) present the electrical performance of coupled vias with short and open defected cases, respectively. From Fig. 3(a), it can be observed that the leakage current and power dissipation increases for a higher pinhole height (h_{pin}) due to a low impedance path between the TSV metal and the Si substrate. From Fig. 3(b), it can be inferred that, approaching to an ideal condition (when r_{con} = 5.04 nm *and* r_{void}=1.05 nm and become closed to $r_{TSV(defect\ free\ via)}$ as 5.25 nm), a spherical air void defected TSV takes larger propagation delay as 2.62%; however, there is an insignificant improvement in delay in case of a partial air cracked TSV. Furthermore, considering pinhole defected TSVs, more leakage current and power can be observed as 95.45% at h_{pin}=10.08 nm compared to h_{pin} =2.1 nm for V_{supply} of 0.7 V.



(a)



(b)

Fig. 3. Electrical performance in terms of (a) Leakage current and power *w.r.t.* supply voltage (V_{supply}) (b) Propagation delay and dynamic power consumption *w.r.t.* connector radius (r_{con}) or void radius (r_{void}) in case of partial air crack or air void defected TSVs respectively.

IV. CONCLUSION

This article summarizes numerous failure mechanisms in a 3D package that uses TSVs, from the aspects of immature fabrication and associated packaging structure. The opens and shorts have been identified as potential reliability threats throughout the fabrication and packaging processes. Additionally, both stacking-related defects (misaligned chips, disconnection failures, etc.) and fabrication-related issues (Cu pumping, pinholes, voids, delamination, wafer thinning, etc.) are expected to be prospective failures. However, as the technology node advances, these imperfection will be progressively more important. In light of the aforementioned research studies, the solutions to overcome the reliability risks of a complete 3D TSV package can be summarized in the following manner: use of low CTE filler to avoid Cu pumping, addition of inorganic filler in an organic substrate to reduce its CTE value, composite liners filled with nano-conduction particles offering low dielectric loss, carbon nano-materials as fillers, solder columns to increase interconnect density, and optimization of chip-stack structures. Furthermore, based on the thorough analysis and investigation considering fabrication and packaging aspects, it can be inferred that the via-last process is the most suitable method for manufacturing of TSVs with conventional Cu filler because it offers more flexibility to incorporate the TSVs on a silicon wafer after BEOL and FEOL processes. Therefore, it can be anticipated that the adoption of recent technologies along with proper manufacturing processes can improve the 3D TSV packaging reliability.

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