IEEE ELECTRONICS PACKAGING SOCIETY Newsletter

JANUARY 2023
VOL. 45 NO. 1
ISSN 1077-2999

Driving Innovation in Microsystem Packaging /// EPS.IEEE.ORG

PRESIDENT'S COLUMN

Kitty Pearsall
Boss Precision. Inc.
Austin, TX

Happy New Year!

I hope everyone's year ended on a peaceful and healthy note as mine did.

Before I address EPS contributions in 2022, I want to comment on what the environment today looks like for the electronic packaging industry segment. We continue to experience a fast paced ever changing industry. IEEE and hence the Electronic Packaging Society is being met with both opportunities and challenges as we move forward. Silicon IC technology continues to evolve quickly, which dramatically influences current and new package architectures such as substrate-based (wirebond and BGA), multichip (2.5D, 3D, and SIP), WLP (Fan-out and Fan-in), Chiplets, and Panel/Embedded Die.

As electronic packaging engineers, you are acutely aware that there are six key applications that are driving the growth of these architectures. These are AI/ML, Industrial IOT, High Performance Computing, 5G Communications, Mobile Technology, and Automotive. The IMARC Group notes "that these expanding applications of packaging in the electronics sector and the increasing demand for various consumer electronics, including wearables, desktops, smartphones, laptops miniaturized devices, etc., are among the key factors augmenting the advanced packaging market." Furthermore, per Gartner, "While 2021 was the beginning of a recovery, 2022 stabilized the segment," and they feel that "2023 will see demand and supply come into balance." The Gartner models show that "2024 will bring a surplus of capacity, where supply will exceed demand." Bearing all this in mind, what is/has EPS been doing to maintain our relevance in this industry sector? What have we accomplished this past year?

As I look back on the past twelve months I do so with pride. I hope that you do too. As a collaborative team within IEEE, we have accomplished so much. I am pleased to report that EPS has met nearly 90% of its twenty-four strategic goals in 2022. Since there are way too many to list, I will share notable highlights with you.

The EPS ***Technology Functional Team*** has increased the number of eNews articles to a total of 17 in 2022. These are peer reviewed papers authored by subject matter experts from the 12 TCs and are being considered for potential Xplore inclusion. The EPS TC members have also increased the EPS representation on IEEE TAB Councils (5 reps), TAB Committees (1 rep), TAB Initiatives (5 reps), and EPS Activities (5). Four of the sixteen representatives have voting rights. While these are volunteer positions above and beyond their TC volunteer work, it is essential to ensure that our EPS members are involved so that EPS maintains our relevance to our electronic packaging industry.

The **Heterogeneous Integration Roadmap** (HIR) held 14 outreach events during 2022 including an annual conference in February 2022 as well as workshops at ICEP, ECTC, SEMICON West, ESTC, IMAPS Boston, ASME InterPACK, and EPTC. The next revision of the HIR chapters is planned for February 2023.

The EPS ***Conference Functional Team*** sponsored/cosponsored over 25 conferences in 2022. In addition to our annual conference series events, EPS introduced several new conferences, workshops, and education events through partnerships within IEEE and with organizations outside of IEEE. For example:

- EPS sponsored its first Conference in Africa, DTMES (Design and Technology of Modern Electronic Systems), located in Addis Ababa, Ethiopia. This event was held in February 2022 and organized through collaboration with AAiT (Addis Ababa Institute of Technology). There were eight live presentations and 14 virtual presentations and 83 registrants. The AAIT ECE department hopes to strengthen their ties with EPS. As a result, an EPS student branch chapter was formed. The 2023 DTMES is being hosted next month.
- EPS partnered with IESA (India Electronics & Semiconductor Association) for a 2-day Semiconductor Packaging Workshop

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NEWSLETTER SUBMISSION DEADLINES

15 June 2023 for Summer issue 2023

1 December 2023 for Winter issue 2023

Submit all material to d.manning@ieee.org

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2025 Term End: Regions 1-6, 7, 9—Jose Schutt-Aine, Luu Nguyen, Region 8—Karlheinz Bock, Tanja Braun, Grace O'Malley, Region 10—Shaw Fong Wong

Publications

Transactions on Components, Packaging and Manufacturing Technology

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Lecturers: Ramachandra Achar, Ph.D., Mudasir Ahmed, Kemal Aygün, Ph.D., Muhannad Bakir, Ph.D., W. Dale Becker, Ph.D., Wendem Beyene, Ph.D., Karlheinz Bock, Ph.D., Bill Bottoms, Ph.D., Chris Bower, Ph.D., William T. Chen, Ph.D., Xuejun Fan, Ph.D., Philip Garrou, Ph.D., Madhu Iyengar, Ph.D., Subu Iyer, Ph.D., Beth Keser, Ph.D., Pradeep Lall, Ph.D., John H. Lau, Ph.D., Ravi Mahajan, Ph.D., James E. Morris, Ph.D., Rajen Murugan, Ph.D., Mervi Paulasto-Kröckel, Ph.D., Eric D. Perfecto, Mark Poliks, Ph.D., Gamal Refai-Ahmed, Ph.D., Jose Schutt-Aine, Ph.D., Rohit Sharma, Ph.D., Nihal Sinnadurai, Ephraim Suhir, Ph.D., Chuan Seng Tan, Ph.D., Andrew Tay, Ph.D., Rao Tummala, Ph.D., E. Jan Vardaman, Paul Wesling, C.P. Wong, Ph.D., Jie Xue, Ph.D.

Chapters and Student Branch Chapters

Refer to eps.ieee.org for EP Society Chapters and Student Branch Chapters list

IEEE Electronics Packaging Society Newsletter is published semi-annually by the Electronics Packaging Society of the Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016-5997. US $1.00 per member per year is included in Society fee for each member of the Electronics Packaging Society. Printed in U.S.A. Periodicals postage paid at New York, NY, and at additional mailing offices. Postmaster: Send address changes to IEEE EPS Newsletter, IEEE 445 Hoes Lane, Piscataway, NJ 08854. For circulation information call IEEE Customer Service 800-701-4333, or FAX 908-981-9667.

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Guoqi (Kouchi) Zhang Receives the 2023 IEEE Rao R. Tummala Electronics Packaging Award

Guoqi (Kouchi) Zhang
Chair Professor, Delft University of Technology, the Netherlands

"For scientific and technological leadership in "More than Moore" (MtM) packaging, codesigning, and reliability."

Prof. Zhang made outstanding technical contributions to More than Moore (MtM) packaging, co-designing, and reliability. His technical achievements enabled many key applications including energy saving via LED packaging, IoE via sensor packages, 5G via AiP, and much more. He is one of the persistent leaders of developing co-designing methods that lays down the foundation for designing for reliability, lifetime diagnostics and prognostics, virtual prototyping/qualification, and digital twin of packaging. Zhang developed an accelerated test method for LED systems that substantially reduced testing time. His accelerated test method opened the way to commercialization of LED technology and has been a key technology in reducing global energy consumption.

An IEEE Fellow, Zhang is a chair professor at Delft University of Technology, Delft, the Netherlands.

2022—Douglas C. H. Yu
"For contributions to the development of advanced packaging technologies and their implementation in high-volume manufacturing."

2021—Chin C. Lee
"For contributions to new silver alloys, new bonding methods, flip-chip interconnect, and education for electronics packaging."

2020—Mitsumasa Koyanagi and Peter Ramm
"For pioneering contributions leading to the commercialization of 3D wafer and die level stacking packaging"

2019—Ephraim Suhir
"For seminal contributions to mechanical reliability engineering and modeling of electronic and photonic packages and systems."

2018—William Chen
"For contributions to electronic packaging from research and development through industrialization, and for his leadership in strategic roadmapping."

2017—Paul Ho and King-Ning Tu
"For contributions to the materials science of packaging and its impact on reliability, specifically in the science of electromigration."

2016—Michael Pecht
"For visionary leadership in the development of physics-of-failure-based and prognosticsbased approaches to electronic packaging reliability."

2015—Nasser Bozorg-Grayeli
"For contributions to the advancement of microelectronic packaging technology, manufacturing, and semiconductor ecosystems."

2014—Avram Bar-Cohen
"For contributions to thermal design, modeling, and analysis, and for original research on heat transfer and liquid-phase cooling."

2013—John Lau
"For contributions to the literature in advanced solder materials, manufacturing for highly reliable electronic products, and education in advanced packaging."

2012—Mauro J Walker
"For advancing electronic manufacturing, technology and packaging worldwide through technical innovation and cooperative leadership in industry, government, academia, and professional organizations."

2011—Rao R. Tummala
"For pioneering and innovative contributions to package integration research, cross-disciplinary education and globalization of electronic packaging."

2010—Herbert Reichl
"For contributions to the integration of reliability in electronics systems, and leadership in research and education in electronics packaging."

2009—George G. Harman
"For achievements in wire bonding technologies."

2008—Karl Puttlitz Sr. and Paul A. Totta
"For pioneering achievements in flip chip interconnection technology and for semiconductor devices and packages."

2007—Dimitry Grabbe
"For contributions to the fields of electrical/electronic connector technology, and development of multi-layer printed wiring boards."

2006—C. P. Wong
"For contributions in advanced polymeric materials science and processes for highly reliable electronic packages."

2005—Yutaka Tsukada
"For pioneering contributions in micro-via technology for printed circuit boards, and for extending the feasibility of the direct flip-chip attachment process."

2004—John W. Balde
"For lifetime contributions to tantalum film technology and the introduction of new electronic packaging technology to development and manufacturing."

For additional information on this and other IEEE Technical Field Awards and Medals, to view complete lists of past recipients or to nominate a colleague or associate for IEEE Technical Field Awards and Medals, please visit http://www. ieee.org/awards

New Appointments for 2023

At the November 2022 EPS Board of Governors meeting, the following appointments were made for 2023.

President-Elect

PATRICK THOMPSON (M'87, SM'92) earned his BS, MS and PhD degrees in Chemical Engineering at the University of Missouri-Rolla. He has more than 25 years of experience in advanced packaging research, development and transfer to manufacturing, contributing to technologies ranging from flip chip fabrication and packaging, flip chip on board and chip scale packages, to multi-chip packaging, MEMS, optoelectronic packaging, and high-performance portable packaging. He has led teams at Bell Labs, AMI Semiconductors, and Motorola (now Freescale). Since 2001, he has been a Senior Member of the Technical Staff at Texas Instruments, where he currently leads fine pitch Cu pillar interconnect and TSV packaging technology development.

Pat is active in industry-consortia and industry-university partnerships, including mentoring SRC custom projects and PhD students.

Pat has five patents and over two dozen publications. He has presented packaging tutorials and given invited talks at leading packaging conferences. He is a member of the Electronic Components and Packaging Technology Conference technical program committee, where he has held multiple positions, including General Chair of the 2006 ECTC, and continues to serve as Financial Chair. He has served at both the local and Society level of EPS holding positions including Vice President of Finance, Member-at-Large of the Board of Governors, Administrative Vice President, and Vice President of Technology.

Vice President, Finance

JEFFREY C. SUHLING (AF '94, M '01, SM '17) Jeffrey C. Suhling received his Ph.D. degree in Engineering Mechanics in 1985 from the University of Wisconsin. He then joined the Department of Mechanical Engineering at Auburn University, where he currently holds the rank of Quina Distinguished Professor and Department Chair. From 2002-2008, he served as Center Director for the NSF Center for Advanced Vehicle Electronics. He was appointed Department Chair of the Department of Mechanical Engineering in 2008.

His research interests include solid mechanics, stress and strain analysis, material characterization, experimental mechanics, advanced and composite materials, finite element analysis and computational mechanics. He works primarily on applications of these fields to electronics packaging, including silicon sensors for stress and temperature measurement, and materials characterization and constitutive modeling of microelectronic solders and encapsulants. Dr. Suhling has authored or co-authored over 600 technical publications, and he has advised over 100 graduate students at Auburn University. He is a Fellow of ASME, and is a member of IEEE, SMTA, IMAPS, SEM, ASTM, and TAPPI.

In ASME, Dr. Suhling served as Chair of the Electrical and Electronic Packaging Division during 2002–2003, and was on the EPPD Executive Committee from 1998–2003. Dr. Suhling was the Technical Program Chair of the ASME InterPACK '07 Conference, and General Chair of the ASME InterPACK '09 Conference. He also served the InterPACK Conference Series as Finance Chair (2003), Track Chair for Modeling and Characterization (1999), Track Chair for Reliability (2005), and Honors and Awards Chair (2011). He was Associate Editor of the ASME Journal of Electronic Packaging from 2014–2019.

In IEEE, Dr. Suhling has been a member of the Electronics Packaging Society (formerly CPMT Society) for the past 30 years. He has served on the ECTC Program Committee (Applied Reliability) from 2003-present, and as Co-Chair of the ECTC Professional Development Course Committee from 2007-present. He was first elected to the IEEE Electronics Packaging Society Board of Governors in 2014, and has served as Member at Large (2014-2016), Director of Membership Services (2016-2018), and Vice President, Education (2019-present). Dr. Suhling has served in several roles in the ITherm Conference Series including Conference Program Vice Chair (2017), Conference Program Chair (2018), and Conference General Chair (2019). He is currently serving as Chair of the ITherm PDC Committee, and Co-Chair of the ITherm Best Paper Committee.

Vice President, Education

ERIC PERFECTO (M'95, SM'01, F'17) has extensive experience working in microelectronics. At IBM, Eric has led the development of multi-level Cu-polyimide advanced packages for high-end systems, followed by the introduction of Pb-free solder interconnects and 2.5D wafer finishing. As part of the IBM Microelectronics Division divestiture, Eric moved to GLOBALFOUNDRIES where he established a Si Photonics packaging development line. In

2019 he returned to IBM part time to establish a heterogeneous integration line in Albany. He holds a M.S. in Chemical Engineering from the University of Illinois and a M.S. in Operations Research from Union College.

An author of more than 80 technical papers and three book chapters, Eric received two Best Conference Paper Awards (2006 ESTC and 2008 ICEPT-HDP) and the 1994 Prize Paper Award from CPMT Trans. on Adv. Packaging. He holds 55 US patents and has been honored with two IBM Outstanding Technical Achievement Awards.

Eric served as the 57th ECTC General Chair, the 55th ECTC Program Chair and is the current ECTC Publicity chair. For the last 12 years, Eric's popular Flip Chip Fabrication and Interconnection course has been given at ECTC to great reviews. He is an EPS Distinguish Lecturer, an IEEE Fellow, and has achieved IMAPS and SPE senior membership.

Eric has represented the EPS members previously, elected 4 times to the BoG. For 3 years he served as the EPS Strategic Director of Global Chapters and Membership where he focused on enhancing the EPS membership value. Through his efforts, the CPMT Transactions are now part of the EPS membership. For 8 years, Eric has chaired the EPS Awards Committee responsible for the EPS Mayor Awards, the Regional Awards, the PhD Fellowship, the ECTC Student Travel Awards and the ECTC Volunteer Award. He is the current chair of the Rao Tummala Electronics Packaging Award. At a local level, Eric is the membership Chair of the Mid-Hudson IEEE Section and founding member of the EPS Mid-Hudson EPS Chapter where he serves as membership chair.

Newly Elected Members of the Electronics Packaging Society Board of Governors

In 2022, EPS members elected new Members-at-Large to the EPS Board of Governors for the three-year term of 1 January 2023 through 31 December 2025:

REGIONS 1-6, 7 & 9

LUU NGUYEN (AM '92, M '96, SM '99, F '01) is the Director of Quality and Reliability at PsiQuantum since 2019, a start-up based in Palo Alto, CA, that aims at building the first large-scale, error-corrected, general-purpose silicon photonics-based quantum computer. I drive the quality and reliability efforts around integrating a complex quantum optical system-on-a-chip, based on scalable foundry manufacturing processes. As an integrated system, the technical challenges span control systems, cryogenics, optical design, non-linear quantum optics, optoelectronic packaging, process development, software, test and measurement, and supply chain and logistics. I co-lead IEEE Quantum, an IEEE Future Directions initiative launched to serve as IEEE's leading community for all projects and activities on quantum technologies. A project plan was developed to address the current landscape of quantum technologies, identify challenges and opportunities, leverage and collaborate with existing initiatives, and engage the quantum community at large. I serve on the Steering Committee for IEEE Quantum Week, the flagship conference on all quantum computing and engineering topics, and participate in many technical committees (ECTC Packaging Technologies, TC on Reliability, TC on Emerging Technologies, Rel. for Electronics & Photonics Packaging Symposium), award committees (CPMT Field Award, SMTA Society Awards, and ASME Allan Kraus Thermal Management Award, EPPD Awards), and EPS Fellows Nomination committee. I am currently an Associate Editor for T-CPMT, and have been a Guest Editor for three past issues (Drop Testing (2007), Wafer Level Packaging (2008, 2009).)

I retired as a Fellow at Texas Instruments in 2019, where I worked on various strategic initiatives that included sensors, printed electronics, high voltage packaging, wafer-level packaging, thermal management, design-for-manufacturability, and design-for-reliability. I graduated with a Ph.D. in Mechanical Engineering from MIT and worked at IBM Research, Philips Research, and National Semiconductor. I have co-edited two books on packaging technologies. I have written several book chapters, have over 70 patents and invention disclosures, and over 200 publications. I am a Fellow of IEEE and ASME, a Fulbright Scholar (Finland 2002), a Fannie and John Hertz Fellow, and an AAAS Mass Media Science and Engineering Fellow. I received two Best Paper of Conference Awards, one Best Poster of Conference Award, and eight IMAPS and IEMT Best Session of Conference Awards. I have received the 2004 IEEE CPMT Outstanding Sustained Technical Contributions Award, the 2015 IEEE Outstanding Engineering Manager Award for the IEEE Region 6, and the 2018 Surface Mount Technology Association Member of Technical Distinction. Other awards also include the 2003, 2014, 2015, and 2016 Mahboob Khan Outstanding Mentor Award from the Semiconductor Research Corporation to recognize contributions to student mentoring, research collaboration, and technology transfer. I co-led the efforts at National Semiconductor to garner the Electronic Product Design (UK) e-Legacy "Investment in Training Award" (2007), the "Investment in Education Award" (2007), and the European Electronics Industry "Investing in People" Elektra Award (2006) for the most innovative company training scheme to foster professional development, practical training, best practices sharing, mentoring, cross-training, and e-learning among more than 2,500 engineers worldwide.

STATEMENT OF INTEREST

As a Member-at-Large, I bring a diverse packaging background to the BoG, and can help in many areas such as encouraging member engagement (focusing on member retention, increasing participation in professional activities, networking services, career development, and industry engagement) and guiding the technical committees on megatrends and emerging technologies.

JOSE SCHUTT-AINE (M 82-86, StM 86-88, M 88-98, SM '98, F'07) received his B.S. degree in electrical engineering from the Massachusetts Institute of Technology, Cambridge, in 1981, and the M.S. and Ph.D. degrees from the University of Illinois at Urbana-Champaign (UIUC), Urbana, in 1984 and 1988, respectively.

He joined the Hewlett-Packard Technology Center, Santa Rosa, CA, as an Application Engineer, where he was involved in research on microwave transistors and high-frequency circuits. In 1983, he joined UIUC, and then joined the Electrical and Computer Engineering Department as a member of the Electromagnetics and Coordinated Science Laboratories, where he is currently involved in research on signal integrity for high-speed digital and high-frequency applications. He is a consultant for several corporations. His current research interests include the study of signal integrity and the generation of computer-aided design tools for high-speed digital systems.

Dr. Schutt-Ainé was a recipient of several research awards, including the 1991 National Science Foundation (NSF) MRI Award, the National Aeronautics and Space Administration Faculty Award for Research in 1992, the NSF MCAA Award in 1996, and the UIUC-National Center for Superconducting Applications Faculty Fellow Award in 2000. He is an IEEE Fellow, EPS Distinguished Lecturer, and served as Co-Editor-in-Chief of the IEEE Transactions on Components, Packaging and Manufacturing Technology (T-CPMT) from 2007 to 2018.

STATEMENT OF INTEREST

Vision is to advance the state of the art in co-design for heterogeneous integration through the use of novel methods and algorithms. Objective is to make tools available to the electronic design and semiconductor industries.

REGION 8

KARLHEINZ BOCK (M'96, SM'17) since 2014 has served as Professor and chair of electronics packaging and director of the institute of electronics packaging (IAVT) at the TU Dresden. Since 2008 he has served as a Professor of Polytronic Microsystems at the faculty of Communication and Electronics Engineering at the University of Berlin. He earned his Diploma on electrical and communication engineering from the University of Saarbrücken, Germany in 1986 and his Dr.-Ing. (Ph.D.) for RF microelectronics from the University of Darmstadt, Darmstadt, Germany in 1994. From 1996 to 1999 he worked in the materials packaging and reliability department of IMEC vzw. in Leuven Belgium. He received the "Japan Society for Promotion of Science (JSPS) Award" in 1994 for his PhD thesis and worked as post-doc from 1994 to 1995 at the Tohoku University in Sendai, Japan. He received two Doctor honoris causa, in 2012 from the Polytechnical University of Bukarest in Romania for his work on organic and flexible electronics and heterointegration and in 2019 from the Sikorsky-Polytechnical University of Kiew, Ukraine for his work in electronics packaging. Since 2017 he serves as a vice dean and since 2021 he serves as the dean of the faculty of electronics engineering and information sciences at the TU Dresden as well as in the rector of the TU Dresdens advisory boards for research and managing diversity as well as in the TU Dresden commission for environmental sustainability.

He served in the Fraunhofer Gesellschaft, from 2001 until 2014 where he has been employed as head of the Polytronic and Multifunctional Systems department at the Fraunhofer Institute for Reliability and Microintegration (IZM, Munich branch, from 2010 named EMFT) and as deputy director from 2006 until 2010 of IZM and from 2010 until 2012 as acting director of Fraunhofer EMFT.

Karlheinz Bock has contributed more than 300 publications and more than 20 patents. He co-authored 16 best paper awards. (see Google Scholar and Research Gate) He is engaged in developing the technological community of 3D systems, heterosystem integration and packaging and organic and flexible electronics, advanced packaging and reliability. He serves on the emerging technology TPC of IEEE ECTC since 2008, as sub-committee member and vice chair 2011 and chair 2012; as member of IEEE IEDM since 2008 on TPC for display sensors MEMS (DSM) and as chair of DSM TPC in 2010; as the European arrangements co-chair 2011, chair 2012 of IEEE IEDM executive committee; furthermore he served on the IEEE ESTC conference technical program committee since 2012; 2016 he has served as the program chair of IEEE ESTC 2016 and as the general chair of IEEE ESTC 2018. Since 2015-2018 he served as vice chair and from 2018-2020 as chair of the technical committee of emerging technologies of the IEEE EPS. Since 2020 he serves on the IEEE EPS ECTC executive committee and as a program chair of IEEE ECTC 2022 and at present as the vice general chair of ECTC2023. Since 2014-2018 and re-elected from 2020 he serves on the board of governors BoG of IEEE EPS for region 8.

STATEMENT OF INTEREST

As BoG member, Karlheinz Bock would like to extend CPMT presence and excellence in advanced packaging i.e. multi-functional, chiplet and advanced 3D systems heterointegration and emerging technologies, in particular additive manufacturing, materials and process co-integration and non-destructive characterization and condition monitoring and related structural health monitoring, chip package interaction CPI, advanced materials modelling and simulation, since these topics are of paramount importance to transfer new technologies to industrial use.

In highest priority, he would like to advance the inclusion and diversity as well as the securing of work force process in our packaging community, promote the student education and international exchange and support and mentor the young professionals in electronics packaging and their integration to our community of packaging. In this background he has been the initiator and organizer of

the IEEE EPS future packaging vision competition for young professionals in 2019 and 2020. In this background we need to extend our activities to schools and pupils at even younger age, in order to seed their interest in electronics packaging engineering for our society. He would also further support the initiatives for life-long education for engineers in the field. He would be deeply graceful if given the opportunity to continue to contribute to the organisation of our international collaboration and joint activities in IEEE EPS region 8 and above regions and societies.

TANJA BRAUN (AM '02, M'03, SM '17) studied mechanical engineering at Technical University of Berlin with a focus on polymers and micro systems and joined Fraunhofer IZM in 1999. In 2013 she received her Dr. degree from the Technical University of Berlin for the work focusing on humidity diffusion through particle-filled epoxy resins. Tanja Braun is head of the group Assembly & Encapsulation Technologies. Recent research is focused on fan-out wafer and panel level packaging technologies and Tanja Braun is leading the Fan-out Panel Level Packaging Consortium at Fraunhofer IZM Berlin.

Results of her research concerning packaging for advanced packages have been presented at multiple international conferences. Tanja Braun holds also several patents in the field of advanced packaging.

In 2014 she received the Fraunhofer IZM research award and in 2021 the Exceptional Technical Achievement Award from IEEE Electronics Packaging Society (EPS) and the IMAPS Sidney J. Stein Award.

Tanja Braun is an active member of IEEE. She is member of the IEEE EPS Board of Governor (BOG) and Technical Chapter "Materials & Processing" as well as the IEEE EPS Region 8 Program Director.

STATEMENT OF INTEREST

Coming from Europe I would like to represent Region 8 in IEEE EPS as well as representing EPS in Europe. This also includes the recruiting of new members to strengthen the European but also the worldwide network. Working in an institute for applied research I am able to connect academia and industry. Additionally, I would like to increase the participation of women within IEEE EPS and support higher visibility of women in engineering.

GRACE O'MALLEY (M '93) is Vice President of Technical and Project Operations for the International Electronic Manufacturing Initiative (iNEMI). Based in Limerick, Ireland, she manages the portfolio of cross-industry collaborative iNEMI projects, development of the iNEMI strategy and interactions with the wide technical community in Europe.

Grace's background is in electronics materials and manufacturing research. Prior to iNEMI, she worked for Motorola in the US on the development and deployment of flip chip capabilities and low-cost assembly processes. She also spent two years establishing and leading a multidisciplinary research team at Motorola's site in Jaguariuna, Brazil, supporting the volume manufacturing of cell phones, radios and cellular infrastructure for the Latin America markets. Grace started her career as a research engineer, focused on electronics packaging and board assembly, at the Tyndall National Institute, Cork, Ireland.

Grace has an honours bachelor's degree in electrical engineering from University College Cork (Ireland), and a Master of Science in materials and manufacturing engineering from the Illinois Institute of Technology (Chicago, U.S.A.). She holds eight U.S. patents. Throughout her career she has authored presentations for many conferences including IMAPS and ECTC. Grace has been a member of IEEE-EPS since the start of her career, supporting many events in the region. She served as a member-at-large in the EPS BOG for Region 8 for 2018-2020.

STATEMENT OF INTEREST

The electronics packaging industry is experiencing a period of very rapid development impacting all aspects of humanity. EPS plays an important role in ensuring the success of our industry by helping alignment on the challenges that need to be addressed through the technical committees and the HIR Roadmap activities, by showcasing the latest technical developments through supporting conferences, webinars and lecture series across the globe and by creating a strong and vibrant network to foster developments in the industry and in the personal careers of EPS members.

As a membership organization EPS should endeavour to reach out and understand the needs of the existing membership and the industry, while also working to attract new thought leaders from other regions and industry segments. Based on my previous experience on the BOG and skillset I would like to work on enhancing the member feedback processes, as well as promoting more opportunities to identify and engage new members, while communicating the benefits of membership particularly to those in Region 8. Fostering engagement with students and young professionals earlier in their careers, as well as engaging non-traditional electronics organizations in the technical work of EPS is a key interest area for me.

Continuous development of a strong technical workforce is a key enabler for our industry. EPS can play a significant role by leveraging its large network of technical leaders and content to help enhance the knowledge base and careers of its members globally. I would like to contribute to promoting and improving access to this knowledgebase; enabling members to gain valuable recognition through the EPS certification process for taking these courses and also developing course content in relevant areas of strength in the region.

Conferences and EPS sponsored events are proven valuable forums for members to learn and network. I want to continue to work to develop and grow the relevancy and value of the EPS sponsored conferences in Region 8, in particular the flagship conference of ESTC. These events are very important to growing the electronic packaging ecosystem, its related supply chain and research activities in the region. They are also of great importance to EPS members, as they provide opportunities to showcase their work in the region to a worldwide technical audience, while being kept up to date on the latest developments in all aspects of electronics packaging.

REGION 10

SHAW FONG WONG (M '07, SM '11) is currently the Probe Card Module Department Director in one of the Kulim Campus' factories. He joined Intel Technology, Malaysia as the ATD-Malaysia Q&R Engineer back to Y2001. Over the years, he assumed different positions and portfolios related to packaging process, assembly, test and material technology developments. During his tenure, Shaw Fong supported multiple chipset development programs specialized in warpage and SJR testing development. He later harness competencies related to packaging process, assembly, test and material technology developments. In 2009, he was promoted to manage the ATTD-Malaysia Core Competency Laboratory and led a team of lab engineers and technicians working on mechanical and structural testing in supporting various package platform developments, virtual factory support and customer/industry engagements. His engagement spread across APAC factories and dealing with standard transfer, direct startup of product level warpage characterization. He played significant role in dealing with coplanarity and warpage related review boards to ensure the right fixes are in place. Shaw Fong received his Bachelor and Master's Degree in Mechanical Engineering from National University of Malaysia (UKM) and Science University of Malaysia (USM) respectively. Lately, Shaw Fong also obtained a PhD degree from University of Kuala Lumpur (UniKL) in electronic packaging research. Shaw Fong has total of 8 patent fillings and Intel Trade Secrets and published more than 70 articles both in internal and external conference or technical journals. In his personal capacity, Shaw Fong has held multiple roles in IEEE/EPS organization, chairing many local or regional IEEE/EPS conferences in Malaysia and had been served as IEEE/EPS Malaysia Chapter chair since Y2016. He was nominated to receive the Outstanding Young Engineer Award and Region-10 Contribution Awards in 2010 and 2019 respectively by IEEE/EPS society too. Shaw Fong's is very much into sports especially football (soccer) of which his favorite team is Liverpool and he is a strong believer in: You Never Walk Alone!

STATEMENT OF INTEREST

A long-term IEEE/EPS member that is very enthusiastic in the contributing to the electronic packaging operations, including manufacturing, research, and technology development. He has been one of the founding members in supporting the development of Malaysia EPS Society since Y2003. He always instrumenting himself on engagement both local academia and industry through technical collaboration, conferences, and student development activities. He is also driving a very good and close collaboration among R10 chapters by significantly engage and promote technical activities to enhance the long-term strong partnership within the region. Since Y2021, as the Junior Past Chair for EPS Malaysia Chapter, he is committing himself to strike for further and more engagement and contribution to the BoG thought his great influences in Malaysia and R10 region. Hence, he has been very active and interested in membership and chapter development for IEEE EPS regional chapter. He is very committed to ensure that the EPS chapter is relevant to packaging community through dissemination of technical knowledges in technical conferences or webinar. He is looking to provide more opportunities for all who are interested in electronic packaging, this includes a potential sponsorship and development of a potential newly form chapter from Vietnam with strong electronic industry development.

Congratulations to New IEEE EPS Senior Members

The members listed below were elevated to the grade of Senior Member between June and November 2022.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields for a total of 10 years and have demonstrated 5 years of significant performance. For additional information or to apply online: https://www.ieee.org/membership/senior/

Vinod Arjun Huddar, Bangalore Section
Tanj Bennett, Seattle Section
Liqiang Cao, Beijing Section
C. Key Chung, Taipei Section
David Conway, Boston Section
Gang Duan, Phoenix Section
Xiaomin Duan, Germany Section
Fengze Hou, Beijing Section
Jin-Ho Kim, Seoul Section
Sarah Kim, Seoul Section
Pamela Leatherwood, Phoenix Section
Ru Li, Benelux Section
Goran Miskovic, Austria Section
Julio Navarro, Seattle Section
Naoya Okamoto, Tokyo Section
Paul Paret, Denver Section
Yang Peng, Wuhan Section
Rene Poelma, Benelux Section
Sandeep Razdan, Oakland-East Bay Section
Ramon Santo-Tomas, Melbourne Section
Bidyut Sen, Santa Clara Valley Section
John Shalf, Oakland-East Bay Section
Spyridon Skordas, Schenectady Section
Rajinder Tiwari, Uttar Pradesh Section
Boris Vaisband, Montreal Section
Geert Van Steenberge, Benelux Section
Teong Guan Yew, Malaysia Section
Qiming Zhang, Hong Kong Section

Congratulations to the 2023 Newly Elevated IEEE EPS Fellow

Listed below is the new IEEE Fellow who is a member of the EPS. See a list of all EPS members who are IEEE Fellows in the IEEE Fellows Directory. The grade of Fellow recognizes unusual distinction in the profession and shall be conferred by the Board of Directors upon a person with an extraordinary record of accomplishments in any of the IEEE fields of interest. (Bylaw I-104:11) Nominees shall:

- have accomplishments that have contributed importantly to the advancement or application of engineering, science and technology, bringing the realization of significant value to society;
- hold Senior Member or Life Senior Member grade at the time the nomination is submitted;
- have been a member in good standing in any grade for a period of five years or more preceding 1 January of the year of elevation.

The year of elevation to the grade of Fellow is the year following approval by the Board of Directors conferring the grade of Fellow.

Members elevated to the Fellow grade may use the title immediately following approval by the Board of Directors. The IEEE Fellows, an elite global group with international recognition, are called upon for guidance and leadership as the world of electrical and electronic technology continues to evolve.

Andrew Tay
"For contributions to hygro-thermo-mechanical failure prevention of semiconductor packaging."

MEMBERSHIP NEWS

Society Member Digital Library—Renew Your Membership

EPS has launched a new Member Digital Library (MDL) which provides EPS members online access to EPS' full archive of sponsored technical content, including conference proceedings and journals at no additional charge. This includes ECTC, HOLM, ESTC, EPTC, the IEEE Transactions on Components, Packaging and Manufacturing Technology and much more!

Sign into Xplore to access the Digital Library.

The MDL is available to members who join EPS or renew membership for 2023.

EPS Student Chapter Promotion Programs

To promote the formation and continuation of EPS student chapters, EPS continues to support a couple of promotion programs. The Student Chapter Promotion Program (SCPP) is aimed at the formation of new student chapters while the Student Chapter Continuation Program (SCCP) is aimed at helping existing student chapters to remain viable.

Student Chapter Promotion Program (SCPP)

Under the SCPP, six students from any university which has an IEEE student branch who are willing to serve as executive committee (excom) members in a new student branch chapter (SBC) will be given complimentary IEEE+EPS student memberships.

Additionally, faculty members who are willing to serve as Advisors to new SBCs will also be given complimentary IEEE+EPS eMemberships where available, otherwise regular memberships will be provided. The Advisor's duties include advising the excom on student chapter activities, endorsing financial statements where necessary, ensuring that annual election/appointment of new student excom members are held before end December, and that required reports are submitted by the student excom in a timely manner every year.

Student Chapter Continuation Program (SCCP)

Another program, the Student Chapter Continuation Program (SCCP) has also been initiated to facilitate the continuation of existing EPS student chapters. Similar complimentary IEEE+EPS memberships will be given to six students in a university with an *existing* EPS SBC who are willing to serve as executive committee (excom) members in the student chapter, and to a faculty who agrees to serve as the Advisor to the student chapter.

To qualify for subsidy under the SCCP, the excom and Advisor must ensure that their SBC remains viable for the year. This includes the organization of at least two technical activities per

calendar year, formation of new excom for the following year, and timely submission of required activity and financial reports for the year.

An evaluation on the performance of subsidized student excom members and Advisors will be conducted in December each year based on reports submitted. Non-performing students and Advisors will not be subsidized for another year. While Advisors may be subsidized every year, student excom members may normally be subsidized for up to 2 years, in order to encourage a healthy succession of student leaders in the chapter. However, if the Advisor can report some extenuating circumstances, the subsidy for an excom student can be extended for up to 4 years, subject to the approval of the Student Program Director.

Annual Subsidy for Student Chapters

To support the organisation of technical activities by SBCs, existing SBCs may apply for subsidies of up to US$1000 per annum from EPS. For new SBCs in their first year, the subsidy can be up to US$1500.

PUBLICATIONS NEWS

Electronics Packaging Society Section Within IEEE Access

The Electronics Packaging Section within IEEE *Access* will draw on the expert technical community to continue IEEE's commitment to publishing the most highly-cited content. The Journal peer-review process targets a publication period of 6 weeks for most accepted papers. This journal is fully open and compliant with funder mandates, including Plan S.

This is an exciting opportunity for your research to benefit from the high visibility of IEEE *Access*. Your work will also be exposed to 5 million unique monthly users of the IEEE *Xplore*® Digital Library.

Scope

The IEEE Electronics Packaging Society section in IEEE Access covers the scientific, engineering, and production aspects of materials, components, modules, hybrids and micro-electronic systems for all electronic applications, which includes technology, selection, modeling/simulation, characterization, assembly, interconnection, packaging, handling, thermal management, reliability, testing/control of the above as applied in design and manufacturing. Examples include optoelectronics and bioelectronic systems packaging, and adaptation for operation in severe/harsh environments. Emphasis is on research, analysis, development, application and manufacturing technology that advance state-of-the-art within this scope.

Get Published in the New Electronics Packaging Society Section of IEEE Access

Go to: https://mc.manuscriptcentral.com/ieee-access

Select the Electronics Packaging Society (EPS) Section from the pull-down menu of "Manuscript type" in the first page of the submission process.

Author Information and Instructions

EPS is committed to supporting authors and researchers with IEEE Author Tools including the IEEE Publication Recommender, IEEE Graphics Analyzer, LaTeX Analyzer and more. Discover the tools available at the IEEE Author Center—https://ieeeauthorcenter.ieee.org/ieee-author-tools/.

The EPS is regarded as a trusted and unbiased source of technical information for dialog and collaboration to advance technology within the computing community. EPS is led by researchers and technology professionals who are at the center of respected electronics packaging communities where readers and authors already come together.

The articles in this journal are peer reviewed in accordance with the requirements set forth in the IEEE Publication Services and Products Board Operations. Each published article is reviewed by a minimum of two independent reviewers using a single-blind peer review process, where the identities of the reviewers are not known to the authors, but the reviewers know the identities of the authors. Articles will be screened for plagiarism before acceptance.

Article Processing Charge (APC): US$1,850

IEEE Members receive a 5% discount.
IEEE Society Members receive a 15% discount.
These discounts cannot be combined.

Topical Editors

Ravi Mahajan, Intel Corporation, USA
Wendem Beyene, Meta, USA
Muhannad Bakir, Georgia Institute of Technology, USA
Koneru Ramakrishna, Private Consultant, USA
Hsien-Chie Cheng, Feng Chia University, Taiwan
Yogendra Joshi, Georgia Institute of Technology, USA

Most Popular Articles according to Xplore® Usage Statistics

Recent Advances and Trends in Advanced Packaging
John H. Lau
Publication Year: 2022, Page(s): 228–252

Universal Chiplet Interconnect Express (UCIe): An Open Industry Standard for Innovations With Chiplets at Package Level
Debendra Das Sharma; Gerald Pasdast; Zhiguo Qian; Kemal Aygun
Publication Year: 2022, Page(s): 1423–1431

A Review of 5G Front-End Systems Package Integration
Atom O. Watanabe; Muhammad Ali; Sk Yeahia Been Sayeed; Rao R. Tummala; Markondeya Raj Pulugurtha
Publication Year: 2021, Page(s): 118–133

CPU Overclocking: A Performance Assessment of Air, Cold Plates, and Two-Phase Immersion Cooling
Bharath Ramakrishnan; Husam Alissa; Ioannis Manousakis; Robert Lankston; Ricardo Bianchini; Washington Kim; Rich Baca; Pulkit A. Misra; Inigo Goiri; Majid Jalili; Ashish Raniwala; Brijesh Warrier; Mark Monroe; Christian Belady; Mark Shaw; Marcus Fontoura
Publication Year: 2021, Page(s): 1703–1715

Embedded Multidie Interconnect Bridge—A Localized, High-Density Multichip Packaging Interconnect
Ravi Mahajan; Zhiguo Qian; Ram S. Viswanath; Sriram Srinivasan; Kemal Aygün; Wei-Lun Jen; Sujit Sharan; Ashish Dhall
Publication Year: 2019, Page(s): 1952–1962

President's Column (*Continued from page 1*)

in Bengaluru, India in December 2022. The event was aimed at creating leadership and encouraging innovation in India. A follow-on event is planned for 2023.

- EPS is joining the EPS Japan Chapter, IMAPS, and the JIEP (Japan Institute of Electronic Packaging) as a Technical Sponsor for the International Conference on Electronics Packaging (ICEP) to be held in Kumamoto, Japan in April 2023. This was a collaborative effort will yield a quality set of papers to be available through the IEEE Xplore digital library.
- A Mini-Workshop on "Emerging Trends in Semiconductor IC Packaging" was hosted by IEEE EDAPS (Electrical Design of Advanced Packaging and Systems) and the University of Mauritius in November 2002. There were 30 participants, and the intent was to set the stage for the EDAPS annual conference held subsequently in December 2022.

The EPS ***Educational Functional Team*** managed a diverse portfolio of continuing education offerings in 2022 including 30 Distinguished Lecturer events held across the globe, over 30 Professional Development Courses (PDCs) held in collaboration with our EPS conferences, and 60 webinars hosted by Society Chapters and Technical Committees. Participants in these events were eligible to receive continuing education certificates and CEU/PDH hours. In addition, EPS continues to offer a multi-tiered Certificate Program to recognize documented professional development by EPS Society members, as well as longer-term significant contributions in the areas of technical leadership/expertise and professional engagement/service. To date, 40 unique society members have been recognized with one of these certificates.

The EPS education team also organized two Electronics Packaging Education Workshops held as general sessions at our EPS flagship conferences in 2022 in Europe and Asia. The first workshop was held in Sibiu, Romania in September 2022 and featured 6 speakers from European universities and industry, and 150 attendees. The second workshop was held in Singapore in December 2022 and featured 5 speakers from Asian Universities and 100 attendees. Future workshops are being planned for our 2023 conferences.

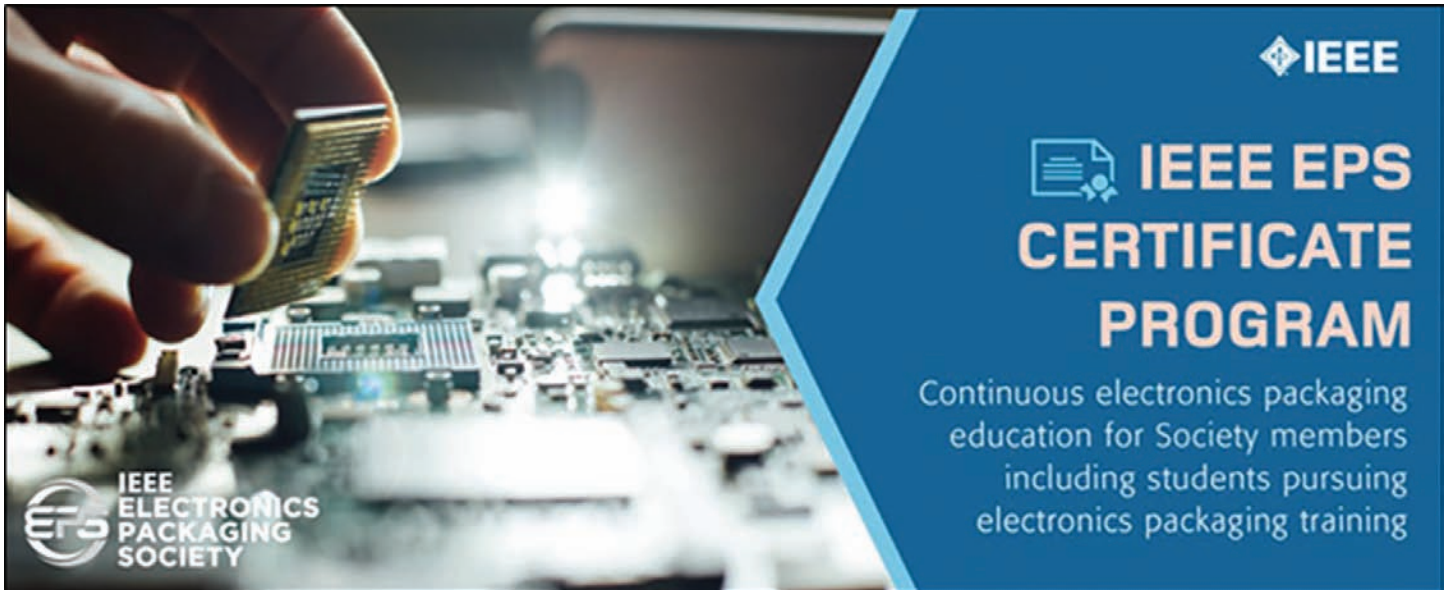
The EPS ***Publication Team*** received exciting news in November. The EPS Transactions on Components, Packaging, and Manufacturing Technology (T-CPMT) was rated as a high performing journal by IEEE TAB Periodicals in 2022. This rating recognized high performance in the average weeks between article submission and first decision, as well as the average weeks to online publication of accepted articles.

The EPS ***Awards Team*** created the new EPS William Chen Distinguished Service Award. This award will recognize and honor outstanding service and leadership to the Electronics Packaging Society and its sponsored activities. The first presentation of this Award will be at ECTC 2023.

The EPS ***Membership Functional Team*** developed a new significant membership benefit for IEEE EPS members. The "EPS Digital Library" went live in November 2022, and now all EPS members have free access in IEEE Xplore to T-CPMT articles as well as to papers published at our technically sponsored conferences including ECTC, EPTC, ESTC, EDAPS, ITHERM, 3DIC, HOLM, IEMT, ICEPT, EMPC, NordPac , IMPACT, THERMINIC, EuroSimE, IWLPC, and others. Membership in EPS is growing, and today we have 38 EPS Chapters and 21 EPS Student Chapters.

Finance: While EPS is a relatively small society in IEEE, it ranks 20th out of 46 Societies and Councils in intellectual property revenue generated through IEEE Xplore, demonstrating the value of transactions and conferences.

We had a great year! I am sure that working together we will continue to grow our accomplishments.



EPS Certificate Program

The IEEE Electronics Packaging Society Certificate Program provides a pathway for early and mid to late-career professionals to highlight their accomplishments.

Criteria for all Certificates: Must be an IEEE Electronics Packaging Society Member.

There are three Certificates you may apply for, which are noted below.

EPS Achievement Certificate

The first level **EPS Achievement Certificate** is aimed at early-career professionals working in the field of electronics packaging. It is especially intended to encourage the career development of young professionals including advanced graduate students.

Criteria: Current EPS Member


IEEE

EPS CERTIFICATE OF ACHIEVEMENT

Is hereby granted to

[recipient.name]

In Recognition of
Having Completed 15 Hours of Professional Development
Continuing Education in the Field of Electronics Packaging
Awarded on [custom.course_date]

IEEE ELECTRONICS PACKAGING SOCIETY

To receive your certificate, 15 professional development hours (PDHs) must be completed. This can be obtained from a combination of the following:

1) IEEE EPS Webinar (1 PDH) – must complete **PDH evaluation**.
2) Professional Development Courses – must complete survey and CEU credit form. Previous ECTC PDCs from the last 10 years can be used towards this if the CEU application was completed at the time of the course. PDCs from ESTC and EPTC 2018 and forward can be used.
   - Electronic Components and Technology Conference (USA) = 4 PDHs
   - Electronic Systems-Integration Technology Conference (Europe) = 3 PDHs
   - Electronic Packaging Technology Conference (Asia) = 4 PDHs
3) Author of IEEE T-CPMT and/or EPS conference paper(s) (5 PDHs) – paper must be published in IEEE Xplore within the last 5 years.
4) Reviewer for IEEE T-CPMT (3 Reviews = 5 PDH) within the last 5 years.

Once you have completed any combination of the above and received 15 PDHs, please complete the certificate form to request your Electronics Packaging Society Certificate of Achievement.

EPS Distinguished Achievement Certificate for Technical Leadership and Expertise

Criteria: Must be a current EPS member

There are five high-level focus areas for this new certificate. These areas include:

1) Being a recognized authority of technical expertise in electronics packaging. Examples include being an advanced member of the technical staff at a company (e.g. Fellow, Senior Technical Staff, Distinguished Engineer, etc.), making technical contributions as a Member or Fellow of professional associations/societies related to electronics packaging

(e.g., IEEE, IMAPs, SMTA, ASME, etc.), and being an invited speaker at companies, technical conferences, and EPS Chapter meetings.

2) Being a subject matter expert (SME) in electronics packaging at conferences, keynotes, webinars, blogs.

   Methods to demonstrate participation as a SME include abstracts accepted and papers presented at conferences, giving keynote lectures at conferences or professional society meetings, presenting webinars for EPS and other IEEE Societies, and serving on technical panels at conferences and other venues.

3) Demonstrating sustained technical contributions to the electronics packaging.

   Demonstrating sustained technical contributions to industry including publishing well-cited technical papers at conferences and in journals, book chapters, and patents; serving as an editor of a journal or reference book; and being a leader or participant in industry blogs, focus groups, technical roadmaps, newsletters, and forums.

4) Documenting advanced technical recognitions in electronics packaging.

   Methods to document technical recognitions include receiving technical awards from a company, institute, professional society, or academic institution; being the acknowledged inventor of a seminal technology or process important to industry; serving as the point person for global high-level task force activity; and being elected to be a Member of an organization such as the US National Academy of Engineering, Royal Academy of Engineering, Chinese Academy of Engineering, IBM Academy of Technology, etc.

5) Provide at least one endorsement letter.

   Nominations for the Distinguished Achievement Certificates will be accepted two times per year: Jan 1–June 30 and Aug 30–Oct 31.

EPS Distinguished Achievement Certificate for Professional Engagement and Service

Criteria: Must be a current EPS member

There are four high-level areas of focus for this new certificate. These areas include:

1) Demonstrating leadership in the electronics packaging field.

   Leadership and broad impact activities in electronics packaging can be documented from outstanding accomplishments during industry employment or for notable volunteer contributions to the profession and society.

2) Illustrating broad impact/influence in the electronics packaging field.

   Examples of significant professional service include serving as an officer in a technical society at the international, national, or local chapter level; participating in packaging related technical committees, councils, or affinity groups; contributing to technology roadmaps such as the Heterogeneous Integration Roadmap (HIR); and receiving a professional society or industry award based on service contributions.

3) Providing extensive service and "give back" to the profession and/or industry; and

   Documentation of "give-back" to one's technical community can be accomplished via demonstrations of coaching and mentoring of co-workers, young professionals, and students.

4) Provide at least one endorsement letter.

   Nominations for the Distinguished Achievement Certificates will be accepted two times per year: Jan 1–June 30 and Aug 30–Oct 31.

More details on the Certificate Program are available on the EPS website at https://eps.ieee.org/education/eps-certificate-program.html.

The EPS Certificate Program is sponsored by the IEEE EPS VP Education and is offered only to EPS members. For questions, please contact Eric Perfecto (eperfecto@gmail.com).

EPS Achievement Certificate

Congratulations to these EPS Members on receiving the IEEE Achievement Certificate from the IEEE Electronics Packaging Society and completing the required number of professional development hours.

Faxing Che, Micron Semiconductor Asia Operations Pte. Ltd
Ankit Kaul, Georgia Institute of Technology

Congratulations to the EPS Member on receiving the IEEE Certificate of Distinguished Achievement from the IEEE Electronics Packaging Society for having made exemplary contributions to the areas of professional engagement and service in the field of Electronics Packaging.

Daniel Donahoe, 1000 Kilometers, LLC

Santa Clara Valley Chapter-EPS Upcoming Events

Electronics Packaging Chapter
Thermal and Failure Analysis of Advanced Sub-Micron Devices
—thermal imaging, fine-geometry, static/dynamic, high-resolution, thermoreflectance, near-ultraviolet to infrared, examples ...

Speaker: Dr. Mo Shakouri, Microsanj Corp.

Date: Thursday, January 26, 2023

Location: in person at SEMI World Hdqtrs, Milpitas, CA USA (and via WebEx)

Time: Check in at SEMI (sandwiches and drinks) at 11:30 AM; Presentation at noon (PST). WebEx at noon.

Cost: none

vTools Information: https://events.vtools.ieee.org/m/336546

Registration: https://r6.ieee.org/scv-eps/?p=2998

Summary: Performance requirements for today's semiconductor and optoelectronic devices are leading to shrinking geometries, more complex 3-dimensional structures, and new materials. High temperatures, hot spots and temperature spikes can have a major impact on reliability. It is essential that one have a thorough understanding of static and dynamic thermal performance under operating and static conditions. This has traditionally been complex, time consuming, and often lacked the resolution required to detect thermal anomalies that could lead to early device failures. Fortunately, advances in thermal imaging techniques that combine the benefits of thermoreflectance-based analysis with illumination wavelengths from near-ultraviolet to near infrared coupled with infrared thermography can support thermal, spatial, and transient resolution consistent with today's advanced complex device structures and shrinking geometries. In addition, equipment has advanced to considerably reduce the time and cost to get accurate results. Many examples will be shared to fully illustrate the device thermal behaviors that can be detected with these advanced thermal analysis techniques.

Electronics Packaging Chapter
Chiplet Design and Heterogeneous Integration Packaging
—SoC, AMD, Intel, TSMC, IBM, interposer, substrates, attach, assembly, trends ...

Speaker: John H Lau, Unimicron Technology Corporation

Date: Thursday, March 9, 2023

Location: in person at SEMI World Hdqtrs, Milpitas, CA USA (and via WebEx)

Time: Check in at SEMI (sandwiches and drinks) at 11:30 AM; Presentation at noon (PST). WebEx at noon.

Cost: none

vTools Information: https://events.vtools.ieee.org/m/336549

Registration: https://r6.ieee.org/scv-eps/?p=2991

Summary: Performance requirements for today's semiconductor and optoelectronic devices are leading to shrinking geometries, more complex 3-dimensional structures, and new materials. High temperatures, hot spots and temperature spikes can have a major impact on reliability. It is essential that one have a thorough understanding of static and dynamic thermal performance under operating and static conditions. This has traditionally been complex, time consuming, and often lacked the resolution required to detect thermal anomalies that could lead to early device failures. Fortunately, advances in thermal imaging techniques that combine the benefits of thermoreflectance-based analysis with illumination wavelengths from near-ultraviolet to near infrared coupled with infrared thermography can support thermal, spatial, and transient resolution consistent with today's advanced complex device structures and shrinking geometries. In addition, equipment has advanced to considerably reduce the time and cost to get accurate results. Many examples will be shared to fully illustrate the device thermal behaviors that can be detected with these advanced thermal analysis techniques.

EPS Resource Center

The IEEE EPS Resource Centers contains valuable, technical content from reputable experts to enhance research or industry work, implement trainings, or earn CEU/PDH credits–all of which are universally available on demand.

IEEE EPS Resource Centers benefits include:

- Access to valuable technical community content
- Access to content 24 hours a day, 7 days a week through an easy-to-use global portal
- Available at no cost for EPS members
- Opportunities to earn CEUs and PDHs

Top webinars:

- The Evolution of Lead-Free Solder Alloy
- Powering Heterogeneous Integration: An overview of the Integrated Power Electronics Chapter of the HIR Roadmap
- Thermal Management Challenges and Opportunities for Heterogeneous Packages
- Recent Advances and Trends in Advanced Packaging
- Chiplet Design and Heterogeneous Integration Packing

https://resourcecenter.eps.ieee.org/

SPRING 2023 COURSE

CHANGING THE WORLD WITH CHIPS:

ENGR 103 - INTRO TO SEMICONDUCTORS

1-CREDIT COURSE (CRN 15199)
WEDNESDAYS • 4:30 PM - 5:20 PM • WALC 1018

Open to all students in the College of Engineering, Polytechnic Institute, and College of Science (Departments of Chemistry, Computer Science, Math, and Physics).

This course will introduce students to semiconductor technology and the broad range of opportunities within the semiconductor industry. Speakers from some of the largest companies in the world including Apple, Tesla, Intel and others will engage students on a weekly basis. Students in the course will develop their personal networks while being presented with resources and opportunities to prepare for exciting careers within the semiconductor industry. The following are some of the topics that may be covered in this course:

- Logic microprocessors
- Memory technology
- Designing semiconductor electronics
- Manufacturing facilities
- Semiconductor modeling tools
- Sustainable semiconductor manufacturing processes
- Non-silicon semiconductor electronics
- Automobile industry and semiconductors
- Digital healthcare technology and semiconductors

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Electron Devices Society
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Office of Professional Practice

Sixth Annual Heterogeneous Integration Roadmap (HIR) Symposium

All times are Pacific Standard Time
Pre-Symposium Tutorials: Wednesday, 22 February 2023 (1:00–4:30 PM)

- Tutorial on Chiplets (including UCIe and BoW)
- *or:* Tutorial on three NIST-sponsored Roadmaps
- No cost to attend just the Wednesday Tutorials
- In-person only (at SEMI Hdqtrs, Milpitas, CA, USA)

Symposium Dates: Thursday & Friday, 23–24 February 2023 (*schedule below*)

- Four Invited Plenary Presentations each morning – Critical Issues in Electronics Resurgence for next decade & beyond
- Key messages from groupings of the HIR Chapters (with cross-TWG panels)
- Cross TWG Collaborations & Dialogues
- Planning for 2023 conference events, workshops & collaborations

Download chapters from the Heterogeneous Integration Roadmap (no cost).

More info and registration
https://r6.ieee.org/scv-eps/?p=3003

IEEE EPS 73rd ECTC – Conference Organizing Meeting 3–4th November, Dallas

Dear IEEE 73rd ECTC Attendees,

A group of dedicated industry leaders and top researchers gathered in Dallas and worked over two days to prepare the exciting premier packaging conference in the world: the IEEE Electronic Packaging Society sponsored ECTC 2023. The subcommittees met and created the conference sessions drawing from 618 abstracts received, of which 335 include a first-time ECTC author. We want to thank all authors who submitted their abstracts. Fortunately, we can accommodate the majority of them in our next program; soon, the authors of the selected papers will be notified. Additionally, the executive committee discussed conference details, including the changes to the program. The authors who submitted abstracts this year may have already noticed that we have updated our abstract submission platform. One of the updates is the requirement that the authors provide the novelty of their work and their abstract.

Before the Advance Program announcement in February 2023, we are happy to share some details of what to expect next year:

- 16 Professional Development Courses, including 4 for the first time.
- There will be 9 Special Sessions and Panels, one dedicated to the CHIPS and Science Act.
- As with previous conferences, the attendees will have a chance to participate and contribute to the Heterogenous Integration Roadmap Workshop.
- 36 Oral and 5 Interactive Presentation (IP) Sessions, including 1 Student IP session.
- Exhibits with Technology Corner and more than 100 exhibitor booths.
- Multiple possibilities to network through various receptions.
- And finally, there will be the famous ECTC Raffle during Friday's Lunch.

During the Technical Program Committee meeting in Dallas, lively discussions took place on how to make the conference more engaging to all ECTC participants. Here are some of the novelties:

- Technical presentations will be shortened to 20 minutes including Q&A
- Breaks will be extended between technical sessions. This will give all ECTC participants more chances for networking.
- Join us early at ECTC 2023—this year, we have a full program of exciting special sessions on Tuesday.
- On Wednesday morning at 8 AM, we will have for the first time, a plenary session with our ECTC 2023 keynote speaker. Our 6 parallel technical sessions will follow at 9:30 AM.
- Other plenary sessions will be organized at 8 AM on Thursday with our EPS Seminar, and on Friday with our EPS President's Panel session.

Thanks to the authors who have submitted abstracts, more than 250 volunteer experts involved in the review and selection process, and the many working in the background, the next ECTC is shaping up very well. We want to express our gratitude to all involved for all their efforts and dedication to ECTC.

To check the latest news, please join our LinkedIn group https://www.linkedin.com/groups/1916290/ or regularly visit www.ectc.net.

Registration for the 73rd ECTC will be open in January 2023.

We look forward to meeting you at the 73rd ECTC in Orlando from the 30th of May to the 2nd of June, 2023!

Inaugural IEEE EPS-IESA Workshop on Electronics Packaging

For the very first time, IEEE EPS joined hands with IESA (India Electronics & Semiconductor Association) to conceive and organize a two-day event "2022 IEEE EPS-IESA International Workshop on Electronics Packaging". The objective of the Workshop was to focus on a set of broad topics spanning education, research, government policy, workforce development, and state-of-the-art technology, manufacturing, test & design aspects of semiconductor packaging.

The event was a resounding success demonstrating excellent planning and execution - with IEEE EPS members, IESA team, and volunteers from Industry and Academia coming together and collaborating effectively. The team evolved over the course of time since middle of 2022.

In the context of the India Semiconductor Mission (ISM), a strategic initiative by the Government of India, the workshop was significant in creating a platform for the Academia, Policy Makers, Industry, Investors, and Researchers to deliberate on semiconductor packaging and test technology, design, and manufacturing roadmap for India. The workshop provided the much-needed impetus to R&D and skills development in advanced packaging – across multiple disciplines. This workshop was conducted on 1st and 2nd of Dec'22, at Taj MG Road, Bengaluru. There were 254 participants, which included 41 speakers and 21 students; except for 4 speakers and 2 students, all were in-person – a significant accomplishment for the maiden workshop co-hosted by IEEE EPS and IESA.

On Day 1, the workshop commenced with the inaugural speeches by Dr. Ashwath Narayan C N, Karnataka State Government Minister for Higher Education, IT & BT, Science and Technology, Skills Development, Entrepreneurship and Livelihood, and Ms. Gunjan Krishna, Commissioner, Department of Industries and Commerce, Government of Karnataka. The inauguration session began with Welcome Addresses by Mr. K. Krishna Moorthy, President and CEO, IESA, and Mr. Sam Karikalan, VP of Conferences, IEEE EPS & Sr. Manager, Package Engineering., Broadcom. Mr. Suresh Subramanyam, General Chair for the workshop & Sr. Director, Intel, concluded the inauguration session with a vote of thanks.

Thereafter, Mr. Vishram Pandit, the session chair who had introduced the guests and speakers prior to the inauguration, took over and introduced the speakers and moderated the 'Technology Session' which had 7 Keynote and 2 Panel sessions. Industry Leaders from Applied Materials, Samsung, Micron, Intel, and HCL delivered keynotes and led a panel session. Dr. Subi Kengeri, VP, Applied Materials, USA, delivered the first keynote "Heterogeneous Package Integration in the AI Era.". This was followed by Prof. Rao Tummala's keynote "Vision for a globally-competitive Indian Electronics and Semiconductors". After each keynote the delegates had the opportunity to ask questions to the speakers. The Technology session continued post a coffee break.

The Second session of the day was chaired by Dr. Sameer Mahajan, which comprised of keynote presentations from Samsung Electronics, Micron Technology, and Intel corporation. Dr. Seung Wook Yoon kicked off the session virtually with his keynote on "Advanced package fab solutions for chiplet integration", which was followed by the presentation by Mr. Harry Singh on "Leading methodologies provide the foundational building blocks across the industry for the continued growth and expansion over the next decade". Dr. Ravi Mahajan concluded the session with his keynote on "The value of packaging and heterogeneous integration". Morning sessions were well received by the audience with active participation during Q&A sessions. The delegates continued their interactions with the presenters during lunch break and as well had opportunities to network.

Mr. Praveen Y. and Dr. Sameer Mahajan co-chaired the third session of the day which comprised of two keynote presentations and two panel discussions. Mr. Amudhan Balasubramanian of HCL Technologies presented on "Advancements in package design and need for package qualification" while Professor Srinivasan Raghavan of IISc Bangalore presented on "'Centre for Nano Science and Engineering' – From science to society". Dr. Suraj Rengarajan moderated the panel session on "Ecosystem needs for

manufacturing collaboration with global entities". Elite panelists from Element Solutions, Micron Technology, and Invest India shared their thoughts and had engaging discussions. Professor Rao Tummala moderated the second panel session on "Emerging educational and research programs in India". Prominent academicians from IIT-Kharagpur, IIT-Hyderabad, IIT-Kanpur, IIT-Bombay, IIT-Madras, and IISc Bangalore contributed to the session and provided their valuable perspectives. After a brief refreshment break, there was the fourth session co-chaired by Dr. Parthasarathy Ramaswamy and Mr. Vishram Pandit. It started off with the panel discussion on "Opportunities and needs for ATMP in India - the India perspective". This session was moderated by Mr. Suresh Subramanyam. Industry leaders from Broadcom, Tessolve Semiconductor, and Würth Electronik shared diverse views on the subject. After the panel session, Mr. Harsha Adya from Würth Electronik presented a keynote on "PCB technology trends and opportunities for India". Overall, both the sessions clearly brought out focus areas from industry and academic experts.

The final session of the first day started off with Banquet Speech by Mr. Sam Karikalan of Broadcom "IEEE EPS- bringing together the world's best in electronic packaging technologies". Ms. Jan Vardaman of TechSearch International shared her views in her virtual keynote "Driving packaging volumes and market segments: where can India focus in near term?" Mr. K Krishna Moorthy presented "Overview of IESA". First day of the workshop concluded with a dinner and cocktail session where all the delegates got an opportunity to interact with global packaging community and network with the delegates and speakers.

On the second day of the workshop, the morning session was chaired by Ms. Kavitha Nagarajan and Ms. Vineela Gedela, which included five keynote presentations from Cadence, India Semiconductor Mission, Broadcom, and Tessolve Semiconductor. Mr. Harsha started off the session with sharing various videos of packaging technology and IEEE EPS (the EPS videos were shared by Dr. Ravi Mahajan). Mr. Vijay Kumar Patil presented a talk on "3D IC is the new system" which was followed by a virtual presentation by Mr. Amitesh Kumar Sinha on "ISM- the semiconductor fab and packaging in India- How critical it is?" Mr. Vivek Raghuraman shared the latest status of Si Photonics in his presentation on "Co-packaging of silicon photonics based optical interconnects". Mr. Sudarshan Sarma and Mr. Anand Muthaiah presented their perspectives in two presentations named "Advances in package design" and "Test & manufacturing challenges with advanced package design", respectively.

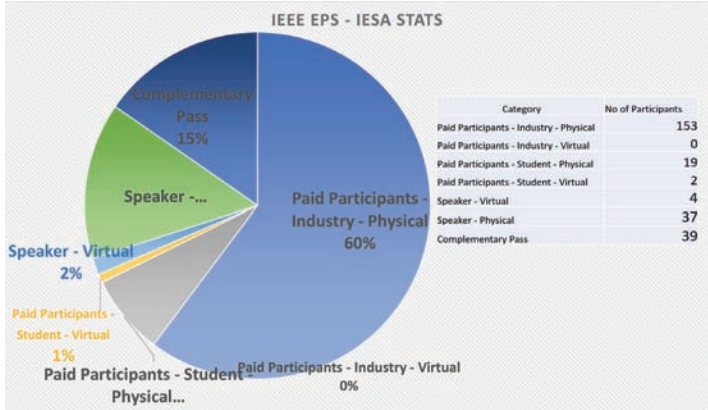
The Second session of the Day 2 was conducted by Dr. Nilesh Badwe, which involved four keynote presentations from LAM Research (2), IIT-Kharagpur, and SLN technologies. Dr. Anandroop Bhattacharya presented "Thermal management challenges and technology development- a focus on alternative air movers" while Mr. DS Suhas presented "Embedded Systems Design, Engineering and Manufacturing Services for Strategic Sectors". Mr. Chee Ping Lee shared the latest equipment innovations in his keynote on "Enabling heterogeneous integration with innovative equipment solutions" while Mr. Andrew Goh shared his views in his keynote on "What does India need strategically in chip level & system level packaging?".

The third session on the second day consisted of two keynotes and one panel session which was co-chaired by Ms. Kavitha Nagarajan and Ms. Juhi Garg. Mr. Ranjay Laha of Bharat Electronics Limited shared his perspectives in his keynote "Strategic electronics defense and space special packaging needs". Miss Sunita Verma from Ministry of Electronics and Information Technology presented a virtual keynote on the "ATMP/OSAT in India- government of India's skilling plans for capacity creation". This was followed by a panel session which was moderated by Mr. K Krishna Moorthy on "Manufacturing workforce training and education". Elite panelists from CMTI, SCL, Global Foundries, and Western Digital shared their views during the discussion and interacted with the audience. Professor Rao Tummala presented "Tutorials roadmap for India which will be conducted in 2023".

In the final session, Mr. Suresh Subramanyam, General Chair, Mr. Sam Karikalan, Executive Chair, and Mr. K Krishna Moorthy, Executive Chair, presented the "Closing Remarks". Volunteer members with active participations and contributions, audience, speakers, panelists, and various committee members were acknowledged. Apart from IEEE EPS team members, this event would not have been successful without the significant efforts from IESA team including Mr. K Krishna Moorthy, IESA president, Ms. Gowthami S, and Ms. Sophia, and other IESA team members.

The initial discussions about the IEEE-EPS and IESA collaboration had started way back in January 2022, with Dr. Ravi Mahajan and Mr. Sam Karikalan taking the lead. The proposal for this two-day workshop was discussed and the initial plan was to combine a five-day Tutorials led by Prof. Rao Tummala with the workshop. In March 2022, a tentative decision was made to arrange a two-day workshop jointly hosted by IEEE EPS and IESA. A small set of volunteers were identified. Thanks to Prof. Rao Tummala, Prof. Andrew Tay, Dr. Chris Bailey, and Mr. SLN Moorthy for their guidance during the initial brainstorming phases as well as throughout the planning phase. In May 2022, an organizing committee of about 16 volunteers was formed. The conference dates of December 1st and 2nd were finalized by IESA Board and IEEE EPS by end of May.

The first planning meeting took place on 31st of May and thereafter regular sync up meetings started. Various committees including finance committee, publicity committee, speakers committee, and sponsorship committee were formed. In mid-July, Mr. Suresh Subramanyam was elected as a General Chair for the conference, and the bi-weekly planning committee meetings started. Various online meetings were organized and volunteers including Arun Chandrasekhar, Nikita Ambasana, Yoginder Negi,



Anant Devi, and Vasanth R D actively participated. There was first face-to-face meeting with volunteers on 28th of July hosted by Prof. Rao. Over the next three months, Mr. Suresh (IEEE EPS) and Mr. Krishna (IESA) worked hand in hand with team members to determine the workshop topics, objectives, technical aspects, financial aspects, sponsorships, government engagement and so on. Various academia and industry experts were contacted based on the proposed agenda and preliminary structure of the conference was put in place by mid of October. By the first week of November, the invitations to the speakers were sent. Depending on the response, the agenda was finalized. The committee members worked with potential sponsors and finalized the generous sponsorships from Intel, Applied Materials, Tessolve, Würth Electronik, CMTI, Government of Karnataka, HCL Tech, Micron, Cadence, and Lam Research.

Various aspects of the workshop went smoothly because of the dedicated efforts of IEEE-EPS and IESA team members. The keynotes and panel discussions were covering various aspects of electronic packaging including design, manufacturing, assembly, various strengths, opportunities, government policies, technical challenges, financial aspects, ecosystem, current and future trends, and so on. The workshop was very successful, which received encouraging feedback to do better in 2023! This workshop has created a platform to enable the academia, industry, investors to focus on short-term and long-term plans working closely with Government policy makers.

Here is some feedback from key leaders:

Prof. Andrew Tay, Region 10 Program Director, IEEE EPS BoG: It has been a fantastic workshop and it is amazing to see all the stakeholders from government, private sector, universities, skills training agencies, EPS, and students, participating so actively in the program. I congratulate you all for the great success of the Workshop!

Mr. Raja Manickam, CEO, Tata OSAT: Good show … meaningful, appropriate timing, energizing… a lot of Indian youth and smart folks will be engaged in packaging 2.0.

Prof. Rao Tummala, Distinguished Prof. and Director Emeritus, PRC, Ga Tech USA: Thanks to the organizers, like Krishna, Sam, Suresh, Vishram, Gowthami and many others, India is on its way to be a global player, Well done, proud and happy to be part of

Dr. Kitty Pearsall, President, IEEE EPS BoG: A very hearty congratulations to you and your team in making this happen. A first for EPS and IESA collaboration, and a first for a conference held in India. I am very proud of all of you and the team that made this happen.

1st face-to-face meeting, hosted by Prof. Rao (28th of July 2022)

The conference was cited in over 20 media reports:

CNBCTV18, Times Tech, MSN, India Education Diary, Business News This Week, Business News Week, Biz News Desk, Times Tech, AdGully, APN News, Mix Point, FM Live, City Air News, KNN, Free Lists, Media Bulletins, Content Media Solutions, Online Media Cafe, Web Media Solutions, Smart Business, Mena FN, NCN

9th edition of the Electronic System-Integration Technology Conference ESTC 2022, the Premier European Event in the Field of Microelectronics Packaging and Integration, a Very Successful One

This 2022 edition, after a long period of online events and social distancing, ESTC 2022 took place in Sibiu (Hermannstadt), an important medieval European Burg, located in Transylvania, a magnificent geographical region of Romania. Starting with 2006, the conference was held in areas located in the west/northwest of the European continent, in well-known locations such as Dresden, London, Berlin, Amsterdam, Helsinki, Grenoble and Vestfold.

Sibiu city guilds and highly regarded intellectuals to today's Sibiu in which, among many other, companies in the field of electronics and microelectronics have found the perfect location to develop, the city has always given science and craftsmanship the place they rightfully deserve as development vectors. This city was in 2007, the year Romania has joined the European Union, the Cultural Capital of Europe. Here in Sibiu, we know how to appreciate curiosity and enlightened minds, as Sibiu is an academic city, embracing the new and innovative.

The current edition brings together, after a forced break of four years, the electronics packaging community under the banner of the IEEE Electronics Packaging Society, in close collaboration with IMAPS Europe. The framework created for the participants, during the oral and poster sessions of the conference as well as the industrial sessions, numerous workshops dedicated to electronics packaging topics, including human resource education aspects, and the exhibition, will allow numerous exchanges of opinion between the professionals in our field, specialists from both parts of our entire community, the industrial environment, and the academic environment respectively. The large number of young participants, many undergraduates or PhD students, will allow them to get in touch with their future profession, to ask questions of the professionals, to find out answers regarding the trends of our world.

We have the chance to create a "first contact" at this R8 premium conference, one of the IEEE EPS flagship conferences: ECTC, EPTC, and ESTC, highly recommended to my industry fellows. We see this event as an opportunity to connect the well-established actors from the electronics packaging global community events with the local representative footprint for electronics industry. By our active involvement, we hope to give the next generations of hardware engineers the chance to apply the ESTC gained knowledge in the vast field of electronics research, development, and industrialization. There is an active push to link the professional environments with the preparation of the students, therefore industrial partners salute the IEEE Student Branch chapters that show a high interest in the event, through actively submitting papers.

Sibiu with Foggaras Mountains in background, left picture, and Downtown of Sibiu with the City Hall and the Catholic Church,—(Grosser Ring), right picture.

Opening ceremony, left picture, and key note from EPS President—Kitty Pearsal, right picture.

"Design Tools and Modeling" track, left picture, HIR Panel Discussion, middle picture, and poster evaluation session, right picture.

Around the corner of this year's conference location, there is a well stablished automotive industry. There is a strong need to link the local electronics ecosystem to the international actions aiming to secure the supply chain, thus ensuring the continuation of the innovation pace. We are challenged by our times, with pandemics and security issues, still I see encouraging and positive mindsets into the IEEE community, with a strong long-term living vision excellent presented in the Heterogeneous Integration Roadmap (HIR),

In the day before the event, took place the IEEE EPS&NTC Student Branch Chapters Summit. It is a meeting organized for students, having two important goals: to present them some of new trends in electronics packaging filed and to know each other and start collaboration between them. This is the first such summit and it took place in Sibiu, Romania, on 12th September 2022 jointly with the 9th Electronics System-Integration Technology Conference. The current edition brings together students from eight IEEE EPS&NTC Student Branch Chapters from Bulgaria, Hungary, and Romania, being an environment where the representatives of these chapters to know each other and excellent opportunity for them to find out the new trends in Electronics Packaging and nanotechnology, from lecturers that are deeply involved in these domains. The industry was involved in organizing of this event through R&D and manufacturing visits at Marquardt and especially Continental Automotive Systems Romania that merge their effort to sustain this summit and to sustain the universities in improvement process of the student's skills as well.

The event was sustained by tech speeches from Kitty PEARSALL, President IEEE Electronics Packaging Society, Beth KESER, INTEL, Director of Packaging and Systems, Klaus WOLTER TU Dresden, Institute of Electronics Packaging and Michael de MONCHY Applications Manager presenting "Die Attach and Preforms" from MacDermid Alpha Assembly Solutions.

The main event was well described in the event Brochure by the ESTC 2022 Program Chair and PROGRAM DIRECTOR 2022–2023 for IEEE Region 8, Tanja BRAUN from Fraunhofer IZM, Germany:

"After a long period of online events and social distancing, we are delighted that ESTC 2022 will give us the chance to meet you in person again and to share and promote new ideas from the realm of advanced packaging. oral and poster presentations

Welcome, Prof. Ovidiu Pop, Hu-Ro Student branch coordinator,upper picture, and Key Note speech from Kitty PEARSALL, President IEEE EPS,lower left picture, and Beth KESER, INTEL Package Engineering & President of IMAPS, lower right picture.

have been organized into technical sessions, covering all aspects of microelectronic packaging. With the introduction of two new sub-committees, one on RF, mm-wave and THz-Systems Packaging and the other one on Global Education for Electronics, we have broadened the traditional scope of ESTC to integrate novel technologies and acknowledged the importance of supporting young talents in electronics, a fact that is also brought home by the many students and PhD students who are participating in this year's ESTC Conference. Other highlights of the conference include high-level keynote presentations given by experts from industry and academia. There will be special workshops on Wednesday morning and ESTC 2022. Thursday afternoon, discussing today's and future challenges in the field of packaging technologies with regard to climate neutrality, intelligent reliability, heterogeneous integration and other pressing topics. At the concurrent industrial exhibition some 30 exhibitors from Europe, Asia and North America will be showcasing their equipment and services—make sure to drop by during the coffee breaks! My thanks go to the local organizers for their help and support and to the colleagues from the technical committee for reviewing the many papers and once again ensuring the highest academic standard of ESTC. Last not least, a warm thank you goes to our industry sponsors and exhibitors for their continued support of ESTC 2022. The ESTC program booklet has been designed as a navigator for your ESTC 2022 participation. It includes all the sessions, presentations, workshops, and evening events to help you make the most of your stay. We are confident that all ESTC participants will return home with new ideas and contacts and look forward to welcoming you in Sibiu to an inspiring and stimulating ESTC 2022!"

The happening was more than expected and as a summary, ESTC 2022 had 353 registered participants from 28 countries from Europe, Asia, North America. The 7 countries with the highest number of participants were: Romania (145), Germany (86), United States (10), France (9), Norway (7), Hungary (7), Austria (7). The IEEE EPS & NTC Summit was held as a joint event with the participation of 8 Student Branch Chapters from Bulgaria, Hungary, and Romania. The participants had the opportunity to visit Sibiu, the European Capital of Culture 2007, and, during the conference dinner, to taste many gastronomic refinements, to enjoy a great cultural program and to visit the beautiful summer residence of Baron Samuel von Brukenthal (a baroque palace built in 1762), located near Sibiu, in Avrig (Freck).

What did ESTC 2022 brings to us?

- Four professional development courses delivered by leading specialists: Why is now the right time to start digitalizing electronics manufacturing with an end-to-end holistic solution?—OREN MANOR, Siemens Digital Industries Software, Israel, Advances in Fan-Out Wafer Level Packaging (FOWLP)—BETH KESER, Ph.D., Intel, Fan-out Packaging and Chiplet Heterogeneous Integration—JOHN H LAU, Unimicron Technology Corporation, Additive Printed Flexible Hybrid Electronics—PRADEEP LALL, Auburn University, Alabama, USA.
- Four sponsored sessions covering hot topics in the automotive industry: Development of Electronic Braking Systems for

Closure ceremony chaired by Prof. Paul Svasta ESTC 2022 General Chair, left picture, and Conference dinner, right picture.

Exhibition area—snapshoots.

iRel workshop team, left picture, and IPCEI workshop team, right picture.

Harsh Environment, Qualification Laboratory—Vibrations in Automotive, From Innovation to Standardization: The journey towards robust manufacturing solutions, The path towards Autonomous Mobility and the technologies that takes us there.

- 7 workshops on Climate neutrality and sustainable electronics, iRel40—Intelligent Reliability along the Value Chain, Nanopackaging, IPCEI—A Session on Industrial Research on Assembly & Packaging in Europe, Heterogeneous Integration Roadmap (HIR) Workshop, University Level Education Activities in Electronics Packaging—Present and Future.
- Ten keynotes addressed the future of a wide variety of technologies and market segments.
- 126 presented papers:
  - 82 oral presentations in 21 parallel sessions
  - 34 poster presentations, including pitch video and e-poster in a virtual gallery on the website
- An exhibition with 33 exhibitors and 17 sponsors.
- A company visit to Continental Automotive Systems Sibiu.

The next **ESTC Conference and Exhibition**, the **10th edition** will be hosted in **Berlin Germany, September 2024**, Conference General Chair being Dr. Tanja Braun, Fraunhofer IZM.

On behalf of the Organizing Committee,

Prof. *Paul Svasta, ESTC 2022 General Chairman*
University Politehnica of Bucharest, and the Association for Promoting Electronics Technology, Romania

Cosmin Moisă, ESTC 2022 Technical Program Co-Chair
IEEE Hu&Ro, EPS&NTC, Joint Chapter Board, Industry Representative
IEEE Region 8 Action for Industry Subcommittee Volunteer,
Continental Automotive, Romania

Highlights of the 24th EPTC Conference

The 24th IEEE Electronics Packaging Technology Conference (EPTC2022) is an international event organized by the IEEE Singapore RS/EPS/EDS Chapter and co-sponsored by the IEEE Electronics Packaging Society (EPS). Since its inauguration in 1997, EPTC has been established as a highly reputed international electronics packaging conference and is the EPS flagship conference in the Asia-Pacific Region. It aims to cover the complete spectrum of electronics packaging technology. Topics include modules, components, materials, equipment technology, assembly, reliability, interconnect design, device and systems packaging, heterogeneous integration, wafer-level packaging, flexible electronics, LED, IoT, 5G, emerging technologies, 2.5D/3D integration technology, smart manufacturing, automation and AI. EPTC2022 featured keynotes, a panel, HIR Workshop, technical sessions, invited talks, PDCs, interactive sessions, packaging education workshop, an exhibition and networking activities.

The 24th Electronics Packaging Technology Conference (EPTC2022) went in-person this year. The conference in the last 2 years (2020 & 2021) were virtual due to COVID-19. The 24th EPTC was held from Dec 7 to Dec 9 at the Grand Copthorne Waterfront Hotel, Singapore. Great catch up with industry technologists and academicians. There were over 430 attendees from 20 countries. The conference had a total of 201 papers, with 137

oral and 36 interactive presentations. 28 papers were prerecorded for on-demand viewing by those unable to travel due to COVID-19 restrictions in their respective countries. The conference had 3 keynotes, a panel session, a Heterogeneous Integration Roadmap workshop, a Packaging Education Workshop, 6 invited presentations, 2 exhibitor presentations, 42 oral sessions and 2 interactive presentation sessions.

A plenary session at EPTC2022.

The conference kicked off with 5 half-day professional development courses: "Reliability Engineering Testing Methodology and Statistical Knowledge for Qualifications of Consumer and Automotive Electronic Components" by Dr Fen Chen, Cruise LLC (a GM company); "Photonic Technologies for Communication, Sensing, and Displays" by Dr Torsten Wipiejewski, Huawei Technologies; "Reliability of Heterogeneous Integration (HI) Systems - Reliability Needs of HI Stakeholders" by Prof SB Park; The State University of New York, Binghamton; "Fan-Out Packaging and Chiplet Heterogeneous Integration" by Dr John H Lau, Unimicron Technology; and "Advanced Packaging for MEMS and Sensors" by Dr Horst Theuss, Infineon Technologies.

Dr Chandra Rao, General Chair EPTC 2022 gave the welcome address, thanking all conference delegates, sharing the conference statistics and appreciating sponsors, exhibitors and conference partners for their support. In her Opening Speech, Dr Kitty Pearsall, the IEEE EPS President, presented an overview of the Society's mission and activities, and expressed her appreciation to the EPTC2022 organising committee for their great work.

Dr Kitty Pearsall, EPS President, giving her Opening Speech.

Following the opening ceremony were 3 keynotes delivered by prominent leaders from industry. Dr Ravi Mahajan, Intel Fellow, give the first keynote on "Challenges and Opportunities in Heterogeneous Integration". He spoke on the tremendous opportunities of Heterogeneous Integration in different application environments and focused on the projected evolution of advanced packaging architectures. He gave specific examples showing how product implementations can take advantage of these technologies to provide an unprecedented level of performance, and described the challenges and opportunities in developing robust advanced package architectures.

First keynote speaker, Dr Ravi Mahajan, Intel.

Dr Raj Pendse, Director of Si Packaging, Meta Reality Lab delivered the second keynote titled, "New Directions and Challenges in the Packaging of AR/VR Hardware". His presentation focused on the new trajectory for Si packaging technology set by the emergence of AR/VR hardware and advanced wearable computing. The next major step in that evolution will be wearable computing in the form of novel, hands-off and all-day wearable AR/VR devices like AR glasses. These devices will continue the remarkable journey of miniaturization and power/performance carved out by their predecessors. He discussed the complex array of packaging technologies that lie under the hood of such devices, spanning the three areas of Augmented Reality Processing (ARP), Display and Imaging (D&I) and Low-energy Wireless (LW) communication. Meta has demonstrated unique approaches that combine advanced packaging technologies like flip chip, fan-out wafer-level packaging and TSV, often within the same package. He discussed the challenges created by the need to spawn new ecosystems, such as heterogeneous integration and fabrication methods that often fall in the grey zone between Foundry and OSAT.

Dr Sundar Ramamurthy, VP & GM Advanced Packaging, Applied Materials delivered the third keynote titled "Materials

Second keynote speaker, Dr Raj Pendse, Meta.

Engineering Innovations to address Next-Gen Electronics Packaging Challenges". He declared that hybrid bonding needed new dielectrics and optimized copper grain morphology which enabled low-temperature processing. Tuning the CMP process for optimal bond surface profiles can improve the efficiency of the bonding process. Panel-level packaging offers the ability to reduce cost by moving to larger format but new challenges for handling large substrates need to be overcome. Speeding up yield-learning and addressing defect sources also requires increased inspection and monitoring for known-good-dies. The materials challenges and engineering innovations that were enabling the advances required for the next generation of electronics packaging was shared.

Third keynote speaker, Dr Sundar Ramamurthy, Applied Materials.

Following the keynotes was a panel session on "Chiplets as An Enabler for System Scaling" which was moderated by Prof CS Tan. The panel speakers were Dr Ravi Mahajan, Intel; Dr Raj Pendse, Meta Reality Labs; Dr Bernd Dielacher, EVG Group; and Dr Yik Yee Tan, Yole Group. The panel revisited the drivers behind chiplets technology, the manufacturing ecosystem, and use-cases. The Universal Chiplet Interconnect Express (UCIe) was also discussed. The panel ended with a critical examination of the supply chain and market outlook.


Panel on "Chiplets as An Enabler for System Scaling".

The Heterogeneous Integration Roadmap (HIR) workshop was held at the end of the conference with the theme "Heterogeneous Integration Paving the Way for Global Electronics Resurgence". Heterogeneous Integration through advanced packaging innovations is widely acknowledged as being increasingly important to drive performance, system availability, power efficiency, cost and time to market of microelectronics systems, from HPC and Data Centers, to 5G and beyond, mobile, autonomous automotive, IoT, medical and health markets. The HIR is a system and application driven roadmap inclusive of the full microelectronics technology ecosystem with the purpose to deliver the next extension of Moore's law for decades to come. Dr Ravi Mahajan gave an overview of HIR which was followed by presentations on Supply Chain by Dr Kitty Pearsall, EPS President; Thermal Management by Dr Gamal Refai-Ahmed, AMD; 2D – 3D Interconnects by Dr Ravi Mahajan, Intel; and Updates on Photonics by Prof. Amr Helmy, U of Toronto.

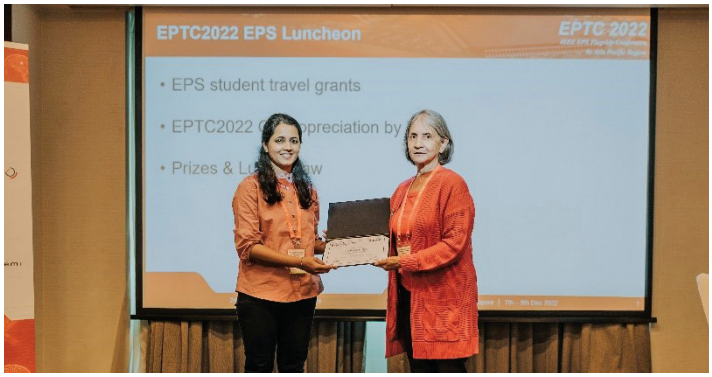
A Packaging Education Workshop was organized in conjunction with EPTC2022. The main objective of the workshop was to discover what some universities in Asia are doing in preparing their students to enter the electronics packaging industry. Prof K. N. Chiang, National Tsing Hua University, (Taiwan); Prof Wenhui Zhu, Central South University, (China); Prof Gu-Sung Kim, Kangnam University, (South Korea); Prof Anandaroop Bhattacharya, IIT Kharagpur, (India); and Prof Chuan Seng Tan, Nanyang Technological University, (Singapore), shared specialization programs on electronics packaging in their respective universities and countries.

Packaging Education Workshop at EPTC2022.

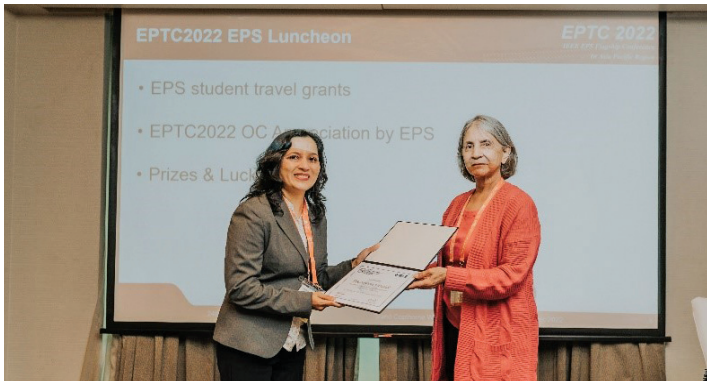

Prof Wenhui Zhu presenting on packaging education in China.

Two EPS-EPTC Student Travel Grants were awarded to two students. They were Ms. Ankitha Rao from Manipal Institute of Technology, India, and Ms. Takshashila Pathade from Dhirubhai Ambani Institute of Information and Communication Technology, India. The travel grants are awarded to encourage students in the electronics packaging field, especially female students and students from underrepresented countries, to become members

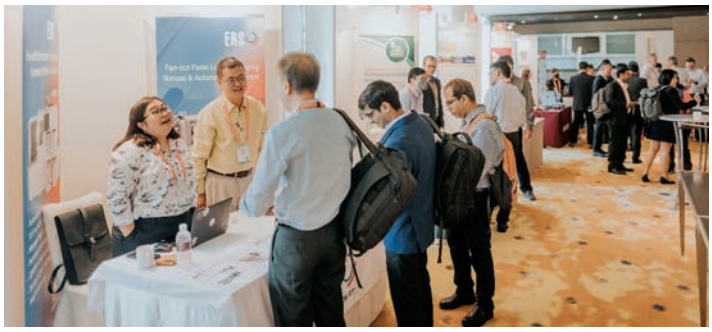
of EPS and actively participate in the flagship conferences of the society. Up to 6 grants will be offered for EPTC annually. Ms. Rao was especially grateful for the travel grant as without it, she would not have been able to present her paper at EPTC2022.



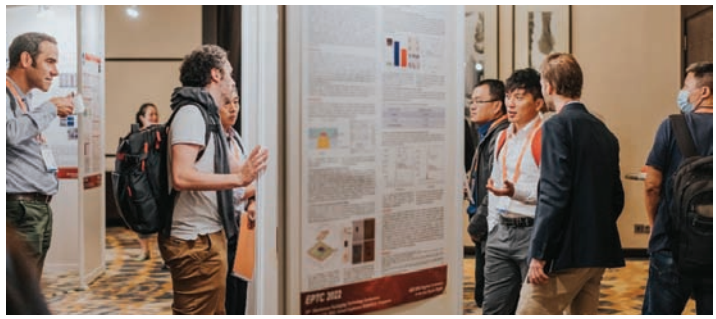
Graduate student Ms. Ankitha Rao receiving her Student Travel Grant Award.



Graduate student Ms. Takshashila Pathade receiving her Student Travel Grant Award.


Lively discussion at exhibition booths.


A well-attended technical session.


Interactive presentation session.


Time for networking during coffee break.


Great food served at the conference.

A highlight of the conference social program is the Banquet which was held this year on the scenic Mount Faber. Delegates were transported up the mount by cable cars and enjoyed the


Cable car ride up to the top of Mount Faber.

Conference banquet at Mount Faber Restaurant.

One of many light-hearted moments at the banquet.

spectacular scenery of the southern coastline. The delegates had a great networking session after a hiatus of more than 2 years due to the COVID-19 pandemic.

Another highlight of the conference was the lucky draw at the end of the conference. The top prize of an iPhone 14 was won by Dr Fen Chen.

One lucky winner!.

Winner of top prize of lucky draw, an iPhone 14, Dr Fen Chen.

The EPTC2022 Executive Committee would like to thank all our conference delegates, sponsors, exhibitors, partners and all other contributors for their participation. Industry partners have continued their strong support of the EPTC in 2022 which has enabled EPTC to be an excellent platform for packaging technologists from all over the world but especially from Asia, to share and exchange information and ideas on electronics packaging technologies. Special thanks to the Executive Committee for their strong commitment, dedication and support in making EPTC2022 a memorable event!

EPTC2022 Organizing Committee.

EPTC2023 will be the 25th Anniversary of EPTC and will be held in the Marina Bay Sands Convention Centre, Singapore, on Dec 5–8, 2023. The normal 3-day conference will be extended by a day to cater for an extra-special program of celebration. The fall meeting of the EPS Board of Governors will be held in conjunction with EPTC2023 and many of the BoG members are expected to play a role in the conference. The Call for Papers will be posted soon at https://www.eptc-ieee.net/.

(Written by Ranjan Rajoo and Andrew Tay)

Upcoming EPS Sponsored and Cosponsored Conferences

Dear Members and Patrons of the IEEE Electronics Packaging Society,
As always, the health and safety of our members and participants is our first priority. Please know that our thoughts are with those affected by the COVID-19 outbreak.

We will continue to closely monitor the developments related to this pandemic and work diligently with the IEEE and our conference organizing committees worldwide on our preparedness. Please reference the IEEE MCE Health and Safety page for the latest information.

Before traveling to any EPS sponsored conference, we recommend that you stay informed of any information your local health agencies and those at the conference location may make available and take reasonable precautions to protect yourself.

The following is the current status of the EPS sponsored conferences for the remainder of 2022 which are all scheduled as in-person events. However, please reference the EPS conference page weekly for the latest updates.

2023 Fourth International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM)
Miami, FL USA
Feb 1, 2023–Feb 3, 2023

2023 IEEE Design and Technology of Modern Electronic Systems (DTMES)
Addis Ababa, Ethiopia
Feb 6, 2023–Feb 8, 2023

2023 24th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)
Graz, Austria
Apr 16, 2023–Apr 19, 2023

2023 34th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)
Saratoga Springs, NY USA
May 1, 2023–May 4, 2023

2023 IEEE 27th Workshop on Signal and Power Integrity (SPI)
Aveiro, Portugal
May 7, 2023–May 10, 2023

2023 46th International Spring Seminar on Electronics Technology (ISSE)
Timisoara, Romania
Abstract Submission Date: Jan 16, 2023
May 10, 2023–May 14, 2023

2023 IEEE 73rd Electronic Components and Technology Conference (ECTC)
Orlando, FL USA
May 29, 2023–Jun 3, 2023

2023 22nd IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)
Orlando, FL USA
May 30, 2023–Jun 2, 2023

Top Conference Papers Based on Usage

2022 IEEE 72nd Electronic Components and Technology Conference (ECTC)

(May 31–June 3, 2022)

Organic Interposer CoWoS-R+ (plus) Technology
M.L. Lin; M.S. Liu; H.W. Chen; S.M. Chen; M.C. Yew; C.S. Chen; Shin-Puu Jeng

3D Packaging for Heterogeneous Integration
Rahul Agarwal; Patrick Cheng; Priyal Shah; Brett Wilkerson; Raja Swaminathan; John Wuu; Chandrasekhar Mandalapu

Wafer to Wafer Hybrid Bonding for DRAM Applications
Jinwon Park; Byungho Lee; Heesun Lee; Dail Lim; Jiho Kang; Changhyun Cho; Myunghee Na; Ilsup Jin

Development of face-to-face and face-to-back ultra-fine pitch Cu-Cu hybrid bonding
Yoshihisa Kagawa; Takumi Kamibayashi; Yuriko Yamano; Kenya Nishio; Akihisa Sakamoto; Taichi Yamada; Kan Shimizu; Tomoyuki Hirano; Hayato Iwamoto

The Influence of Cu Microstructure on Thermal Budget in Hybrid Bonding
Laura Mirkarimi; Cyprian Uzoh; Dominik Suwito; Bongsub Lee; Gill Fountain; Thomas Workman; Jeremy Theil; Guilian Gao; Bryan Buckalew; Justin Oberst; Thomas Ponnuswamy

2022 21st IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)

(May 31–June 3, 2022)

Package level thermal analysis of backside power delivery network (BS-PDN) configurations
Herman Oprins; Jose Luis Ramirez Bohorquez; Bjorn Vermeersch; Geert Van der Plas; Eric Beyne

From 2.5D to 3D Chiplet Systems: Investigation of Thermal Implications with HotSpot 7.0
Jun-Han Han; Xinfei Guo; Kevin Skadron; Mircea R. Stan

Hollow Micropillar Evaporator for Cooling Wide-Bandgap Silicon Carbide Power Converters
Vivek V. Manepalli; Kidus Guye; Erdong Song; Alex Dutton; Daniel Luberda; Quan Chau;Yousof Nayfeh; Troy Beechner; Sean H. Hoenig; Michael C. Ellis; Damena D. Agonafer

A Dynamic Co-Simulation Framework for the Analysis of Battery Electric Vehicle Thermal Management Systems
Tayler Shelly; Justin A. Weibel; Davide Ziviani; Eckhard A. Groll

Device-level Transient Cooling of β-Ga2O3 MOSFETs
Samuel H. Kim; James Spencer Lundh; Daniel Shoemaker; Bikramjit Chatterjee; Kelson D. Chabak; Andrew J. Green; Kyle Liddy; Samuel Graham; Sukwon Choi

2022 9th Electronic System-Integration Technology Conference (ESTC)

(September 13–16, 2022)

Effect of line structures on the self-propagating reaction of Al/Ni multilayer
Konrad Jaekel; Heike Bartsch; Jens Müller; Yesenia Haydee Sauni Camposano; Sebastian Matthes; Peter Schaaf

10 µm and 5 µm Die-to-Wafer Direct Hybrid Bonding
Emilie Bourjot; Alice Bond; Carine Ladner; Nicolas Bresson; Stéphane Moreau; Viorel Balan; Arnaud Cornélis; Renan Bouis; Catherine Euvrard; Noura Nadi; Loic Sanchez; Frank Fournel; Nicolas Raynaud; Pascal Metzger; Eric Ollier

Novel Cu-nanowire-based technology enabling fine pitch interconnects for 2.5D/3D Integration
Adil Shehzad; Ran Yin; Iuliana Panchenko; Maik **Müller;** Steffen Bickel; Olav Birlem; Sebastian Quednau; Jürgen M. Wolf

Design, Fabrication and Measurement of FOWLP-based Series-Fed Antennas for 6G D-Band MIMO Applications
Thi Huyen Le; Oliver Schwanitz; Ivan Ndip; Friedrich Mueller; Tanja Braun; Martin Schneider-Ramelow

PCB Embedding Technology for 5G mmWave Applications
Stefan Kosmider; Thomas Löher; Andreas Ostmann; Kavin Murugesan; Uwe Maaß; Martin Schneider-Ramelow; Le Thi Huyen; Michael Kaiser

2021 IEEE 23rd Electronics Packaging Technology Conference (EPTC)

(December 1–3, 2021)

High Reliability Solution of 2.5D Package Technologies
Hsin Jou Lin; Vito Lin; Joe Lin; Ying Ju Lu; David Wang; Yu Po Wang

Cu CMP Dishing in High Density Cu Pad for Fine Pitch Wafer-to-Wafer (W2W) Hybrid Bonding
HongMiao Ji; King-Jien Chui

Fan-Out Embedded Bridge Solution in HPC Application
Shuai-Lin Bradley Liu; Nicholas Kao; Teny Shih; Yu-Po Wang

Energy management method for energy storage system in PV-integrated EV charging station
Shanshan Shi; Yu Zhang; Luan Ni; Qixing Yang; Chen Fang; Haojing Wang; Yufei Wang; Shuntian Shi

Update on the CHIPS and Science Act

Jan Vardaman, Nancy Stoffel, Benson Chan

Abstract

The 2022 CHIPS and Science Act is the largest investment into the microelectronics industry made by the US government in history. The intent of this legislation is to strengthen the competitiveness of domestic manufacturers and suppliers for microelectronics assemblies. The sweeping vision from the signing brief stated that with this legislation, the US is "making historic investments that will poise U.S. workers, communities, and businesses to win the race for the 21st century. It will strengthen American manufacturing, supply chains, and national security. The Act provides money for investment in research and development, science and technology, and the workforce of the future to keep the United States the leader in the industries of tomorrow, including nanotechnology, clean energy, quantum computing, and artificial intelligence. The CHIPs and Science Act makes the smart investments so that American to compete in and win the future."[1]

What is the CHIPS and Science Act?

The CHIPS and Science Act seeks to do the following:

- Increase capacity in domestic manufacturing and emerging technologies
- Promote critical supply chain resilience
- Strengthen the national capacity for manufacturing innovation, and expands workforce development efforts
- Deliver important measurement and technology to semiconductor R&D needs

The U.S.Department of Commerce (DoC) will manage both the incentive and R&D programs and support industry at large. The incentives program is $39 billion and is focused on increasing domestic semiconductor and packaging capacity and capability. Direct funding and loans will be offered to support these goals. Additionally, there are 25% tax credits available for advanced manufacturing investments as well as loans designed to increase capacity. New advanced fabs have received the most attention, but legacy fabs and packaging will also be funded.

DoC has appointed a Special Advisor to help setup the CHIP Act program office and a team is in place to support DoC semiconductor initiatives. The DoC has actively solicited input from the electronics community. DoC and National Institute of Standards and Technology (NIST) have received over 200 unique responses to a CHIP Act RFI issues from the ecosystem. Workshops were held to define metrology needs for the next 5 to 10 years. NIST issued reports including the Strategic Opportunities for U.S. Semiconductor Manufacturing in August 2022.

Department of Commerce and NIST appointed leaders from industry, academia, and national labs to a newly established Industrial Advisory Committee. $52.7 Billion investment in infrastructure and R& D will be managed by the DoC. There is an additional $2 Billion investment in prototyping and lab to fab transition called the Microelectronics Commons that will be run by the Department of Defense (DoD).

The R&D part of the program has four components, and the funding breakout is shown in Table 1.

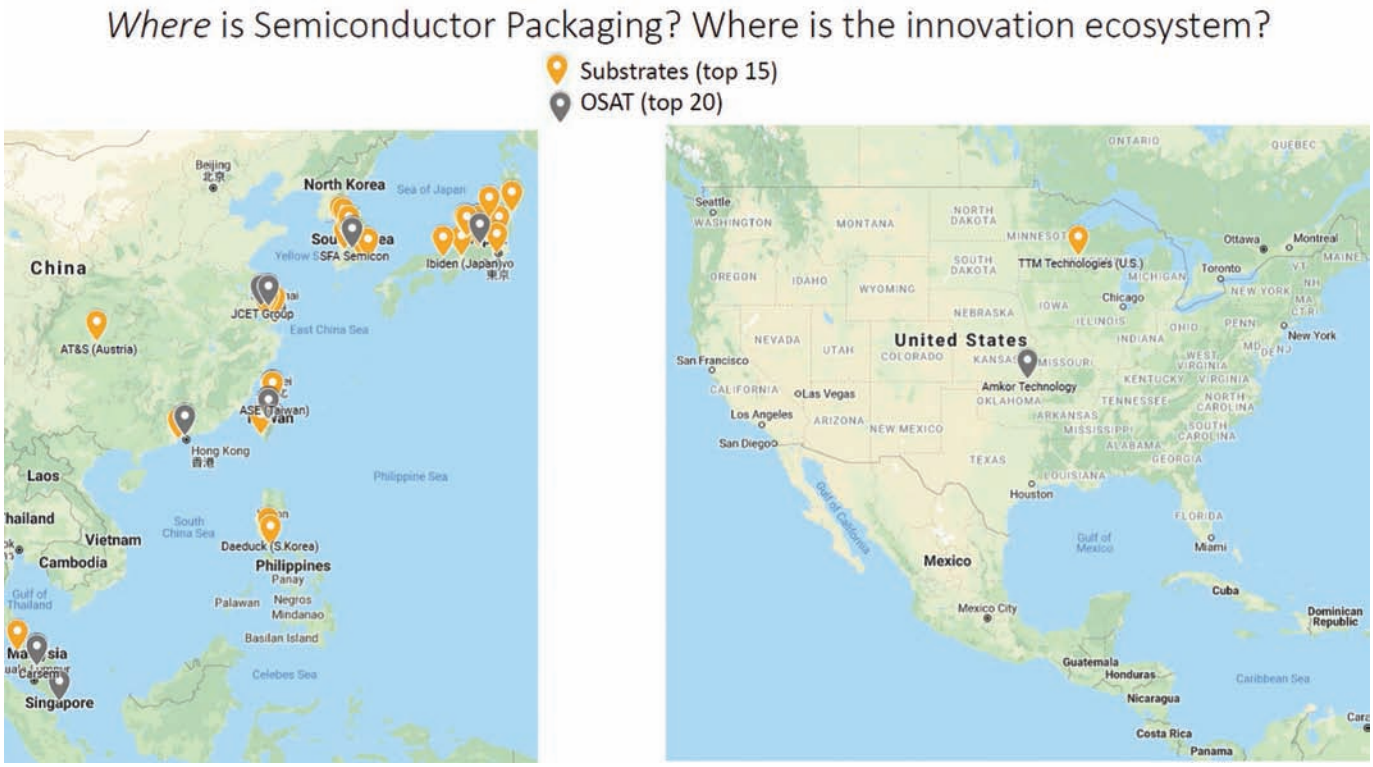


Figure 1. Source NIST.

Table 1: Appropriated Funds for CHIPS and Science Act ($ in Billions) Source: DoC

	FY 2022	FY 2023	FY 2024	FY 2025	FY 2026
Section 9902 Semiconductor Incentives					
Incentives Program	19	5	5	5	5
Section 9906					
National Semiconductor Technology Center	2				
Nat. Adv Packaging Manufacturing Program	2.5	2	1.3	1.1	1.6
Microelectronics Research at NIST	0.5				
Manufacturing USA Institutes					

The outlined programs will be run out of NIST leveraging the organizations' history in grant management and technology expertise. Figure 2 shows the relationship between the new investments managed by the Department of Commerce, and existing programs.

The National Semiconductor Technology Center (NSTC) will be the focal point of the R&D investments. Its mission will be to advance semiconductor technology throughout the semiconductor ecosystem, and seed new industries, based on the availability of advanced semiconductor devices. The NSTC will focus on fab level integrated circuit developments with $2 billion in the first year and continuing investments over the next 5 years.

NIST solicited input across the industry on the needs and structure of the proposed NSTC and they received over 250 responses on their questions on the scope of the NSTC. They have also hosted 36 workshops and solicited input through other advisory bodies. NIST will publish a whitepaper in the first quarter of 2023 that will summarize the results of the landscape analysis, governing structure, and financial models.

The NSTC program described in the 9906 legislation has the following focus areas:

- To conduct semiconductor advanced test, assembly, and packaging capability in the domestic ecosystem."
- Materials characterization, instrumentation and testing for next generation microelectronics.
- Virtualization and automaton of maintenance of semiconductor machinery.
- Metrology for security and supply chain verification.
- training programs and apprenticeships, in advanced microelectronics design, research, fabrication, and packaging capabilities,"

The CHIPS Act is not just about the chips but rather recognizes the critical role that packaging plays in the electronics-manufacturing ecosystem. Without parallel advances in substrate,

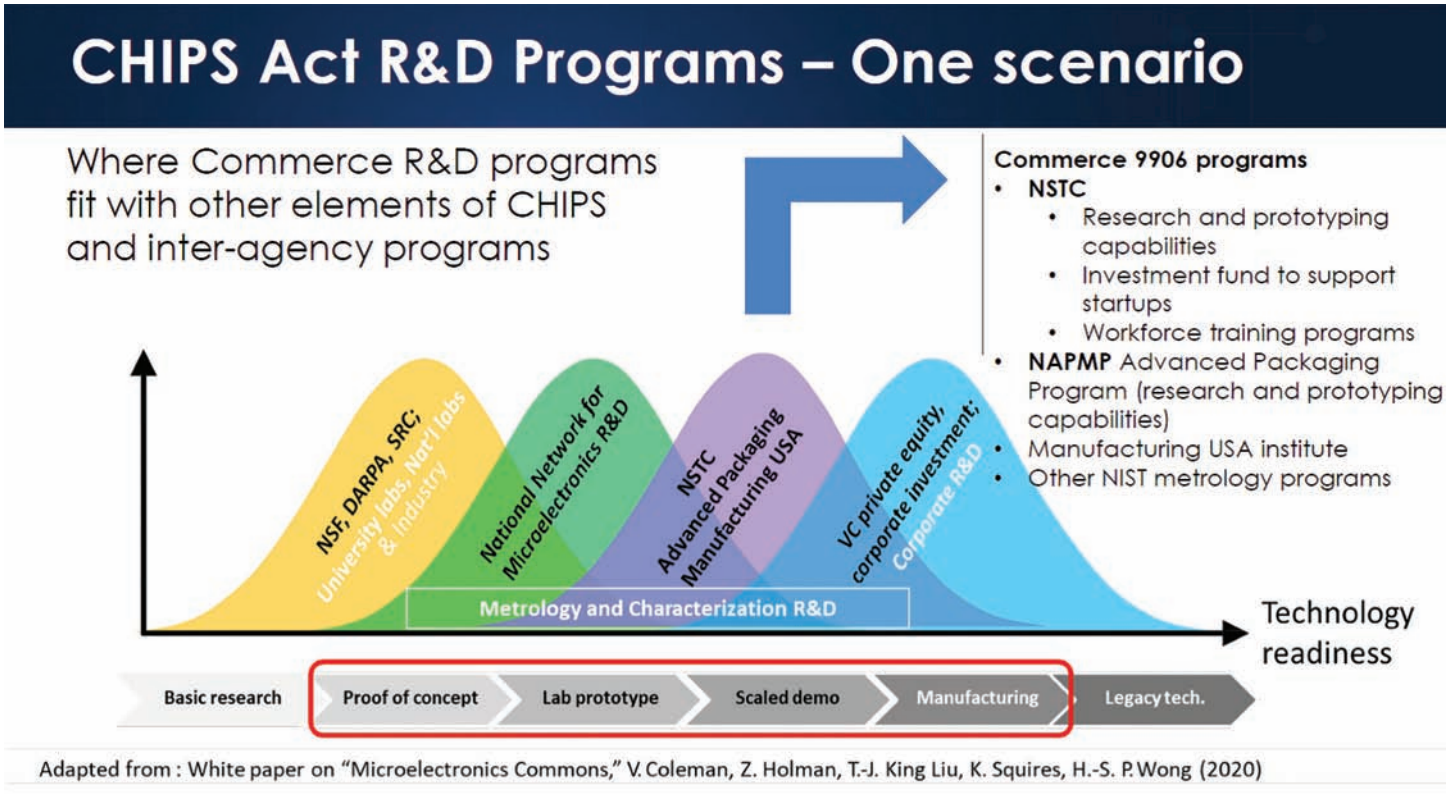


Figure 2. CHIPS and Science Act investments to support semiconductor and packaging development

test and assembly capabilities, the supply chain issues will not be solved. The National Advanced Packaging Manufacturing Program is the largest R&D program investment with a $2.5 billion budget. The focus is to strengthen semiconductor advanced test, assembly, and packaging capability in the domestic ecosystem.

Additional critical R & D investment designed to move developments through the transition from lab to fab, is the Microelectronics Commons. The $2 Billion investment in prototyping capabilities will be run by DoD.

There are also funds set aside for microelectronics Research at NIST which will include a focus on metrology needs for the industry. Additionally further investment into the Manufacturing USA Institutes will be funded at $0.5 billion in the first year with additional funding over the next four years. The intent is to utilize the strengths of the existing 16 manufacturing institutes. These institutes and their focus areas are shown in Figure 3. Additionally, the bill specifies that up to 3 new manufacturing institutes may be funded. The national manufacturing institutes (NMI) focus may include

- Research to support the virtualization and automation of maintenance of semiconductor machinery.
- Development of new advanced test, assembly, and packaging capabilities.
- "…Developing and deploying educational and skills training curricula needed to support the industry sector and ensure the U.S. can build and maintain a trusted and predictable talent pipeline,"

The current common institute features are that they are focused on identified target manufacturing approaches. These Department of Defense Manufacturing Innovation Institutes (MII) are public-private consortia, with strong participation from industry, academia, and government customers. The institutes require cost-match to federal investment. The current list of existing MII are: shown in Figure 3.

The next MII focus areas are under development and input will be sought through an RFI.

The Global share of the US in packaging manufacturing is only 3% (See Figure 4). However, the US has major strengths in packaging research both academic and industrial. With investment, these strengths can be converted into new domestic manufacturing capabilities focused on advanced packaging.

Advanced packaging is an enabler. Combining heterogeneous devices together in a package creates compact and capable systems critical to new applications, DOD, and industrial uses. Packaging incorporates communications capabilities such as 5G and 6G, Bluetooth, and RF, Video drivers, Low-cost combo of cutting-edge chips with legacy chips, Photonics, Compound semiconductor for extending batter life, GPS, stacked memory, and chiplets. Other novel concepts include flexible hybrid electronics. Moore's Law alone is not going to be the enabler of products. New approaches to cost and performance challenges involve shifting from monolithic

Figure 4. North Amerian electronics manufcturing capabilities (source: US DoD and IPC)

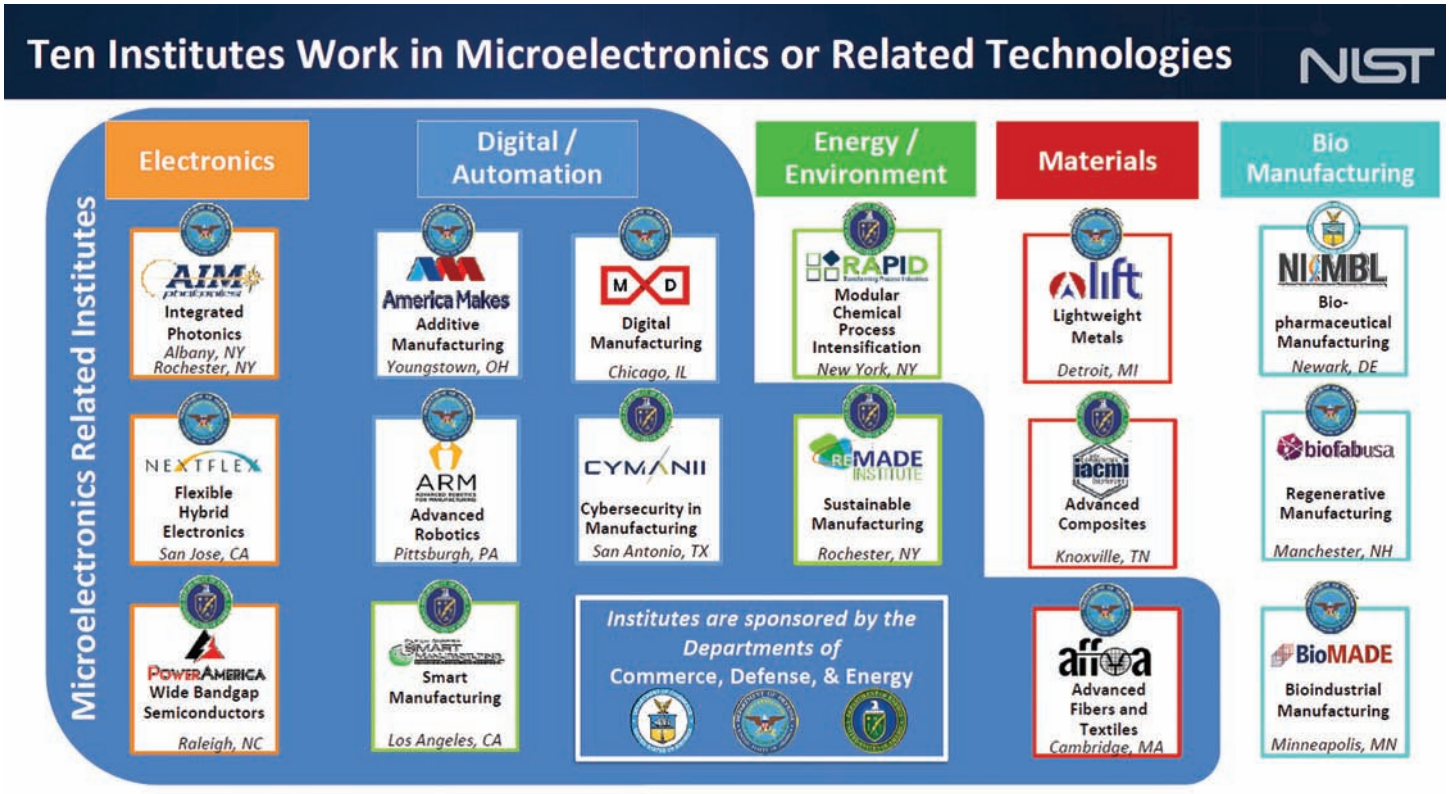


Figure 3. Manufacturing USA Institutes (Source: NIST)

chip design to modular concepts. The future includes 3D manufacturing methods and structures. The CHIPS investments will support the development lifecycle from proof of concept through commercialization as shown in Figure 2.

Workforce development is critical for all the CHIPS Act investments as the demand for skilled workers will increase substantially. "Whoever wins workforce, wins microelectronics. Period." The CHIPS Act has substantial goals to create a new and diversified workforce to meet the workforce needs that will arise with the growth of high-tech manufacturing. At this moment in time, the U.S. has unique opportunities to create a new workforce with the needed skillsets. Figure 5 outlines the needs and initial and emerging programs to address these needs.

Specific communities that may match the opportunity include returning service members transitioning to civilian life (200,000 annually), underserved rural and urban communities. Institutions that have demonstrated success with workforce training will be engaged. These institutions include minority serving institutions (HBCU, HIS, TCU, & others), Manufacturing USA proven programs. An additional resource that can meet the emerging technology skill gap are foreign national students. Half of engineering students are foreign nationals. Retraining of the current workforce will also be critical. Emerging models to increase the engineering and science graduates include national fellowships for graduate and undergraduates, new NSF programs, and stipend-based technical and professional education.

For more information go to:

1) https://Chips.gov
2) https://www.whitehouse.gov/briefing-room/statements-releases/2022/08/09/fact-sheet-chips-and-science-act-will-lower-costs-create-jobs-strengthen-supply-chains-and-counter-china/
3) https://www.mckinsey.com/industries/public-and-social-sector/our-insights/the-chips-and-science-act-heres-whats-in-it
4) https://nstxl.org/opportunity/microelectronics-me-commons/
5) https://www.manufacturingusa.com/news/manufacturing-usa-releases-2022-highlights-report

Acknowledgement

The authors would like to acknowledge Frank Gayle, Robert Rudnitsky and David Seiler for presenting their keynote titled "NIST, Semiconductors and the CHIPS and Science Act" at the 33rd Electronics Packaging Symposium held at Binghamton University, September 7, 2022.

Authors

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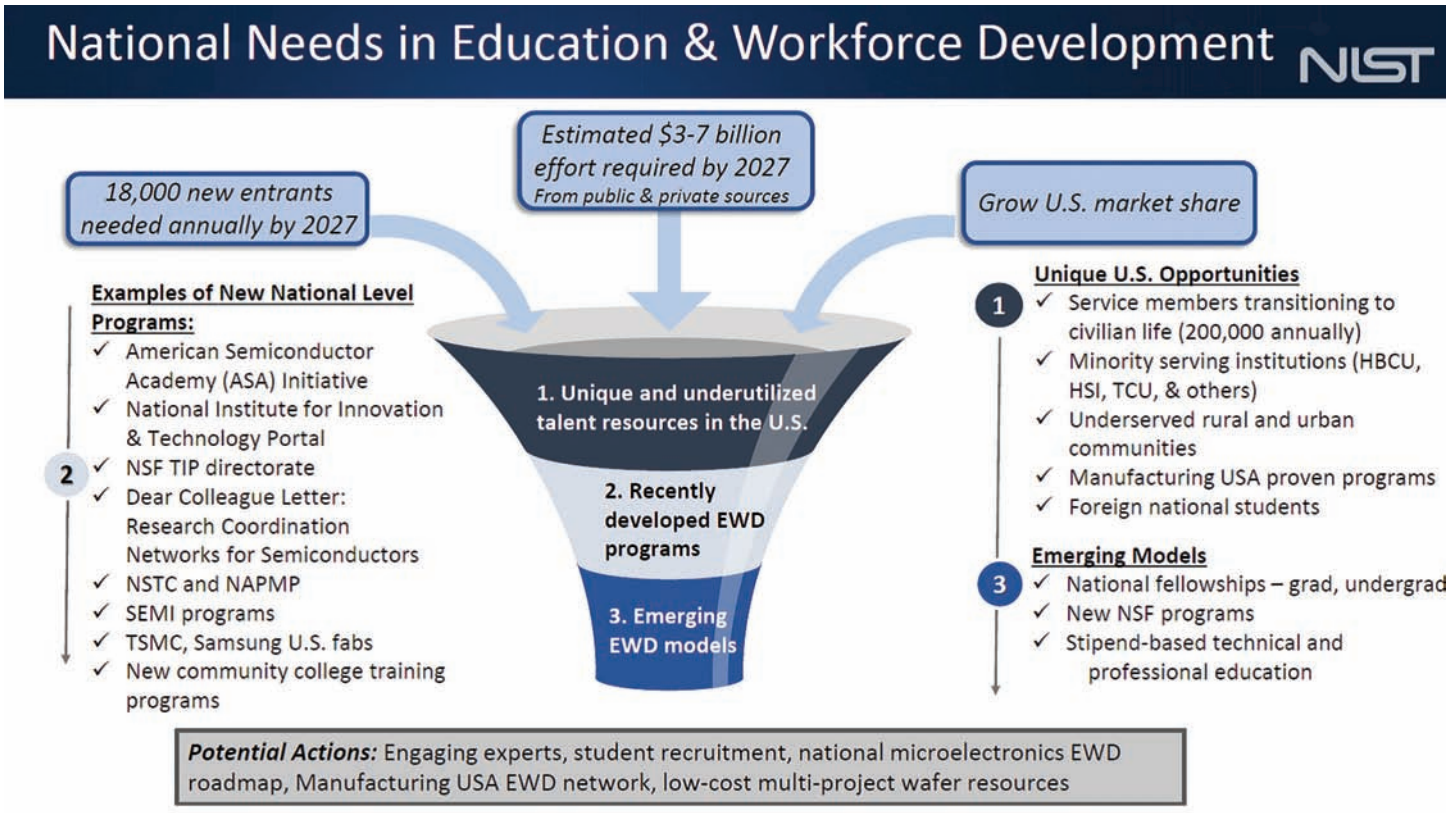

Figure 5. National Needs in Education and Workforce Development (source NIST: Fall 2022)

Nancy Stoffel Nancy holds a PhD in Materials Science from Cornell University. Her career has focused on materials, process development and reliability for electronics integration. Currently Nancy works for GE Research and specializes in design and manufacturing of printed electronic systems and electronics packaging. Nancy is active in the IEEE Electronics Packaging Society and is on the executive board of ECTC.

Benson Chan is the Associate Director for the Integrated Electronics Engineering Center at Binghamton University, a NY State Center for Advanced Technology with a mission to help companies to understand their use of electronics to improve their business by understanding the design, reliability and failures of their products. He holds 53 patents and numerous papers in electronics packaging. He is an iMAPS fellow and IEEE EPS TC Chair for Emerging Technologies and on the IEEE EPS Board of Governors.

Biodegradable and Nanocomposite Substrates: New Prospects for Sustainable Electronics Packaging

Csaba Farkas, Attila Géczy, Rebeka Kovács, Attila Bonyár, *IEEE Senior Member*

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Abstract

Biodegradables and nanomaterials are a promising path for the future of electronics in a greener mindset. Biodegradables and nanocomposites are already effectively used in prototypes and advanced application areas with demanding requirements, such as flexible and wearable electronics, implantable or biomedical applications, and traditional commercial electronics. The nano-enhanced biopolymer substrates (e.g., with improved gas and water barrier functionalities) sometimes also with integrated, nano-enabled functionalities (such as electromagnetic shielding or plasmonic activity) can be beneficial in many electronics packaging and nanopackaging applications as well.

1. Introduction

Electronics industry is facing significant problems with increasing production and, consequently, the problem of hazardous electronic waste [1]. The issue is additionally elevated by the global market-based attitude, which encourages consumers to discard outdated hardware. While most of the electronic equipment and modules are essentially non-degradable, proper recycling is also a crucial concern. In the modern time period of the technology, some rules were implemented to prevent the manufacture of devices with hazardous elements (an example: the "RoHS Directive", which was a key action in this matter more than a decade ago [2-3]).

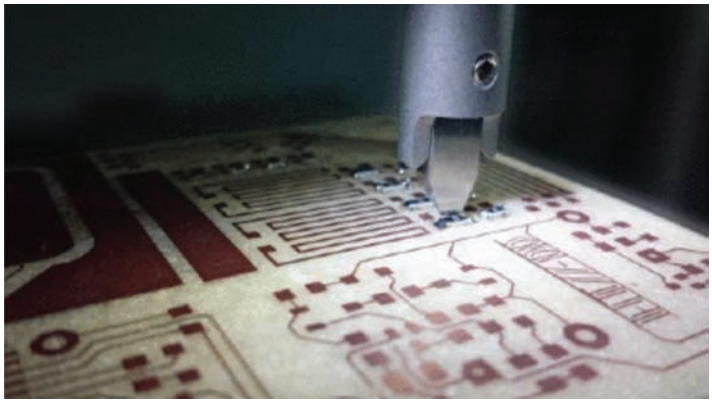

Figure 1. SMT component test on printed circuit board made of sustainable material [4]

Bio-based and modern biodegradable materials only surfaced recently in the field of printed electronics in advance research efforts. In this field, we must separate printed electronics on plastics and flexibles from conventional PCB technologies involving rigid, multilayered PCBs. These substrates can be a promising alternative in the economy-based pathfinding processes of the electronics industry, which is facing problems from the ever-emerging e-waste management requirements.

A possibility to decrease plastics in electronic products is to use materials where advanced end-of-life recycling and recapture can be used - in this vision, biodegradables form a potential future application [4] (Fig 1). Although biodegradable electronic circuit substrates have many favorable properties, modification of their mechanical, electrical, or thermal properties is often needed for advanced applications. By using nanomaterials as fillers, these physical properties can be controlled and improved to match the application-driven requirements. Moreover, new functionalities can also be enabled.

2. Biodegradables as Circuit Substrates

Biodegradables

Special types of polymers, known as bioplastics, become widely known with the development of amylomaize in the 1950s. Bioplastics can be biodegradable and compostable [5, 6] (in accordance with the DIN 12432 standard [7]), or they can be produced from renewable resources. There are various subclasses of bioplastics [5], including:

- Not bio-based, but compostable or biodegradable
- Biobased, yet non-biodegradable;
- biodegradable or compostable at the same time.

Some publications separate biodegradability and compostability of plastics [8], but the overall specification is not set globally yet. Nägele et al. highlighted early [9] that not only the ecological aspects of renewable bio-resources are important in this field; they pointed out the possible increase in costs, which is due to the further depletion of fossil resources. These factors urge the spread of developing novel materials and technologies in the production of electronic substrates. In terms of waste handling, printed circuit boards and printed circuit substrates are essential components of an electronic assembly. Still, the substituting of classical compositions

(such as flame-retardant epoxies with glass fiber reinforcement) is not solved generally in the field.

Despite the beneficial qualities of such substrates, they are rarely used in consumer devices yet. The current findings are well below the technological readiness level of mass production. It must be noted that the use of biodegradables as printed electronics substrates does not imply that these materials will break down during the course of their lifespan, but in specific composting processes or dissolution [10]. The key is that the procedure gets more straightforward and more environmentally beneficial as the item reaches the end of its useful life and becomes e-waste.

Materials and Processes Used to Produce Printed Electronics on Biodegradables

Yedrissov et al. [11] very recently proposed a new method for producing polylactic acid (PLA)-based PCBs to replace environmentally hazardous polymer binders with a biodegradable solution. The production and the recycling process were presented, the proposed material with the recycling method aims to save and reuse the most valuable components of the PCB. PLA was also used by other researchers for composition of such devices. Géczy et al. showed PLA and cellulose-acetate (CA) boards could be used for surface mounting. Recently a promising improvement was introduced by the same team, where flame-retarded PLA was reinforced with flame-retarded flax fibres, to form a biodegradable substrate [12].

Lincoln et al. [13] also tested flax-reinforced bioepoxies - the flammability, thermal resistance, mechanical performance, and electrical properties of prototype circuit boards. The bioepoxy-flax composites show promising results in terms of toxicity, biodegradability, energy consumption, GHG emissions, and economic costs compared to the petroleum-based, epoxyfiberglass composites. Veselý et al. [14] conducted measurements on 3D printed PLA test samples to evaluate mechanical and thermomechanical properties. Guna et al. [15] applied biocomposites to develop biodegradable PCBs, using banana stems and wheat gluten to extract natural cellulose fibers. After the achievement of flame retardancy, adequate dielectric requirements, and performance stability, the proposed agricultural waste and coproducts are offering a feasible solution to produce biodegradable PCBs.

Liu et al. [16] performed life cycle assessment study about the environmental impact of paper-based multilayer printed circuit boards. The paper examined the acidification potential, global warming potential, toxic potential, and ozone layer depletion potential. The environmental impact index is determined, which is found about two orders of magnitude lower than in the case of organic printed circuit boards. However, the examined solution is not suitable for high-density and high-performance integrated circuit applications.

Flexible Substrates and Devices

Next to the traditional PCB substrates, flexible and electronic device substrates are also investigated from this aspect. Daniele et al. [17] applied a citric acid-based elastomer, POMaC - Poly(octamethylene maleate (anhydride) citrate) - as PCB substrate and packaging. Single and multilayer layer POMaC-PCBs were produced and characterized. Swelling behaviour, degradation behaviour, tensile properties, and crosslinking conditions were tested. Held et al. [18] investigated the mechanical properties of biodegradable and photo-cross-linkable elastomer poly(glycerol sebacic) acrylate (PGSA) as a component of soft and stretchable electronics. The rubber-elasticity, biodegradability, and conductivity properties make the examined platforms ideal for agriculture, healthcare, packaging, and disposable electronic consumer products. Chandrasekaran et al. [19] used cellulose-laponite composite as substrate material for printed electronics. The authors examined the effects of laponite with various mass ratios. They found that the thermal and flame retardancy properties are increased by adding laponite into the cellulose, although it makes the substrate more brittle. Jung et al. [21] showed that key electrical components could be presented on flexible cellulose nanofibril paper. Their results had comparable performance with the standard components. Mattana et al. [22] employed polylactic acid (PLA) thin films as substrates for organic electronic devices. The authors reported that the examined substrates are applicable for disposable electronics after the mechanical and dielectric characterization. The study presents the fabrication of organic fieldeffect transistors (OFETs) and all-inkjet-printed organic electrochemical transistors (OECTs) on top of PLA.

Assembling

Regarding the assembly of components to biodegradable substrates, soldering is often applied. A low-temperature solder alloy based on bismuth usually is necessary because of the biopolymer low thermal resistance [11, 20, 23, 24]. As the study by Henning et al., 2019 [23] states, the solder joints exhibit a higher shear strength than those made by conductive epoxy-based adhesive. Nevertheless, the warping of the boards usually occurs due to high differences between the thermal expansion coefficients of the substrate, copper layer, and components. The mechanical properties of resulting joints are usually not as good as those made on FR4 substrates. Several soldering techniques were investigated in the study by [20], including hotiron, selective hot-gas, laser, and vapor phase soldering (VPS). They concluded that VPS is the most promising from the list, due to the uniform heating and applicability of a low-temperature heat-transfer medium.

Next to soldering, components mounting via electroconductive adhesives (ECA) can be a feasible alternative to joining. A benefit of this technique is the possibility of adhesives curing at room temperature. Thus, thermal treatment impacting the assembly can be avoided [25]. Guna et al. established a composite composed of banana fibers and wheat gluten. In both cases, the components for testing the functionality of the circuit were mounted using ECA. The testing did not reveal any defects in the circuit, even after several days of service.

Reliability and Quality Issues

Bozó et al. [26] highlighted that bioplastics could be employed during the manufacturing of microelectronics components and devices, but compared to the conventional polymers, the results show inferior thermal and mechanical properties. Most papers cite this as a general problem with biodegradables in electronic packaging. Silver, contained in the conductive adhesives, is prone to electrochemical migration. This reliability issue occurrence could also be affected by the type of substrate. The biodegradable substrates differ in surface structure from the traditional FR4 substrates and exhibit different wetting characteristics of liquids. This fact, combined with the lower accuracy of the conductive pattern shape, could lead to higher susceptibility to electrochemical migration [27]. Biopolymers can be used as packaging material thanks to their high crystallinity and hydrophobicity [28]. Cao and Ulrich [29] found that the mechanical flexibility of synthetic polymers can be adjusted in the case of

stretchable biodegradable electronics. In our recent comprehensive review paper on the topic [30], we summarized the material parameters for the most common substrates in Table 1: biodegrability or compostability, conductivity [Scm-1], UTS – ultimate tensile strength [MPa], and Tg – glass transition temperature [°C].

3. Nanocomposites

Biopolymer nanocomposites are materials composed of biopolymer matrices modified with nanoscale filler materials. While in bulk nanocomposites, these nanofillers are dispersed evenly in the polymer matrix, in the case of surface nanocomposites, the nanomaterials are usually layered on the surface of a polymer or segregated in a subsurface layer [31]. The role of nanomaterials is twofold, they can either improve the physical properties of the matrix material (nano-enhanced applications), or they can enable new properties and functionalities (nanoenabled applications). For both purposes, the substrate materials discussed in the previous section can be considered ideal biopolymer matrices for nanocomposite fabrication. The addition of different nanomaterials (metallic nanoparticles and wires, metal-oxides, carbon allotropes, etc.) usually does not impair the biodegradable/ biocompatible properties of the substrates. In contrast, the mechanical, electrical, optical, thermal, etc. properties could be influenced to a great extent. Considering printed circuit substrates, we will concentrate on the most relevant properties regarding this application. For readers interested in a wider application area of nanocomposites in electronics, several in-depth reviews can be recommended [28, 32–33]. For the material properties of common conductive nanocomposite materials based on biodegradable or biocompatible matrixes please see Table 1 in [30].

Electrical Properties

Although the primary purpose of using biodegradable substrates is E-waste management, many advanced applications require the modification of the electrical properties of the matrix materials, especially for flexible substrates, where matching the mechanical properties of the substrate and conducting layers is important (e.g., stretchable electronics, wearable or implantable biomedical applications, etc.) [34-35]. As illustrated in Fig. 2, a variety of nanofillers, mostly carbon allotropes and metallic nanomaterials can be used to create conductors from the generally insulating biopolymer materials or increase the conductivity of the few conductive/ semiconductive polymers (e.g., polyaniline (PANI), polypyrrole (PPy),Poly(3,4-ethylenedioxythiophene), (PEDOT)) as well [28]. In our comprehensive review [30], Table 2 presents a few examples of conductive nanocomposite materials based on the most frequently used biodegradable and biocompatible biopolymer matrices.

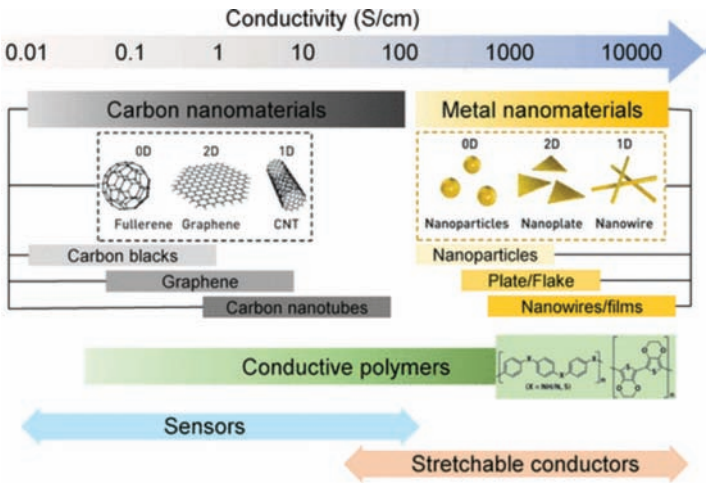

Figure 2. The conductivity of different nanomaterial fillers and nanocomposites with their potential application areas. Reprinted with permission from [35]. American Society of Chemistry 2019.

Mechanical Properties

A favorable property of many substrate materials is their flexibility, which can be advantageous both during processing/manufacture or during applications, such as in bendable, stretchable, or wearable electronics. Although the Young's modulus and tensile strength of a nanocomposite are primarily determined by the matrix, the nanofillers have an influence on it, and in most of the cases, care should be taken not to decrease the flexibility while, for example, creating a conducting nanocomposite [35]. Balancing the mechanical and electrical properties is also important for stiff printed circuit substrates. [36]

Thermal Properties

For high-power, flexible electronic applications, substrates that can effectively dissipate heat while maintaining their mechanical stability are required. Here the aim of doping is to increase the thermal conductivity of the substrate while maintaining its mechanical flexibility. Carbon-based nanofillers are especially promising for this purpose since they combine good thermal conductivity (from ~2000 $Wm^{-1}K^{-1}$ for graphene to ~100 $Wm^{-1}K^{-1}$ for bulk graphite [34]) with low density. By using graphite nanoplatelets, Burzynski et al. managed to increase the thermal conductivity of PDMS 9 × to 1.8 $Wm^{-1}K^{-1}$ at only 11 vol% filler content [37].

Other Properties

Considering electronics packaging applications, important factors can be to improve the gas and water barrier capabilities of the substrates. For this purpose, GO nanosheets were successfully used to decrease the oxygen and water vapor permeability of the polymer matrix [38]. Also, some special electronic devices need packaging with materials having electromagnetic shielding and antistatic functions. Conductive nanofillers, such as MWCNTs were successfully used to create an environment-friendly, biodegradable, low-weight PLLA/MWCNT nanocomposite foam for electromagnetic shielding applications [39]. Besides controlling the conductivity, metallic nanoparticles are often used to endow the biopolymer matrix with plasmonic or catalytic properties, which can be beneficial considering integrated sensor functions and applications [35].

4. Outlook

It was demonstrated through examples that with the help of nanomaterial fillers, the most important physical properties (electrical, mechanical, and thermal) of biodegradable matrices could be controlled and improved. These nanocomposites can enable novel functionalities and tackle the requirements of advanced application areas. The future shows promising application possibilities for such substrates. Still, while the presented demonstrators are mainly laboratory prototypes, the time is near when the technology readiness level will elevate from the general state of advanced research and prototyping. **This article is based on the authors'**

in-depth review of the topic, for further information and referencing please see [30].

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High Performance Graphene Enhanced Thermal Interface Technology for Electronics Cooling Applications

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Abstract

The rapid growth of information technology continues to increase power density and integration levels in electronics devices, leading to an increase in greater heat dissipation, lower performance, and shorter operating life. Thus, the development of new Thermal Interface Materials (TIM) with substantially high thermal conductivity is essential for various device cooling applications. This paper focuses on the development of a new high-performance thermally conductive graphene enhanced TIM (GT-TIM) via chemical cross-linking of vertically aligned graphene and silicone polymer. The effect of vertical alignment on the thermal performance of the new GT-TIM has been evaluated and further potential use in various application areas has been proposed. Advantageously, GT-TIM offers a very low thermal contact resistance at the same time very high elasticity, recovery degree and very high reliability as compared to the state-of-the-art TIM materials available in the market.

Introduction

There is an increasing demand for efficient thermal dissipation materials with high thermal conductivity, and high elasticity to be used in electronics cooling applications such as 5G wireless modules, high-power CPUs/GPUs, data servers, gaming modules, LEDs, and Opto-modules.[1–2] To handle the needs, the industry uses whatever the market can offer and takes higher repair costs, with lower/limited performance to survive and wait for better TIMs to be developed. This indicates that the electronics industry constantly seeks new TIM products to solve thermal management issues.

A variety of thermal interface materials (TIM) (adhesives, liquid metals, greases, pastes, gels, pads, and encapsulates) are available in the market, depending on their application and power requirements.[1] The composition of most TIMs comprises two parts: base

material and filler material. Base materials are silicones, polyurethanes, acrylics, and filler materials including metal powders (silver, aluminium, copper etc) and other non-metallic fillers (carbon black, graphite, graphene, aluminium oxide, silicon oxide etc), which directly affect the thermal conductivity of the final product.[3]

Over the past decade, graphene is considered as a promising material for industrial application in the fields of chemistry, materials science, and engineering.[4–5] Graphene enhanced products have received much attention lately and are promising materials for various industrial applications. Graphene enhanced TIM reported so far is made via traditional approaches using mixing and casting of graphene powder with a suitable polymer matrix. Because of the high thermal contact resistance derived from the weak coupling between the graphene skeleton and the polymer matrix, the random arrangement of graphene sheets and polymer resins seriously reduces the thermal conductivity of the graphene-composite-based TIMs.[6]

Some researchers have focused on improving the thermal conductivity using an aligned form of graphene.[6] However, to construct TIMs with excellent thermal conductivity, graphene sheets with high in-plane thermal conductivity need to be put together and assembled such that they are ordered in the vertical direction so that the intrinsic thermal properties of graphene can be fully extended and used. However, the arrangement and assembly strategies of graphene sheets are very complicated and often end with the poor performance of the final graphene-based TIM. So, careful molecular engineering of graphene layer alignment is required, which plays a decisive role in transmitting the thermal properties of the graphene microstructure to the macroscopic graphene assembled materials.

To our best knowledge, no research publications are available on the vertically aligned graphene and silicone-based TIM that offer as high thermal conductivity as GT-TIM. In this publication, a graphene assembled film and the silicone polymer matrix were chemically cross-linked to get GT-TIM and it was characterized via the ASTM 5470 method for the thermal performance. Reliability tests were also carried out to examine GT-TIM stability and thermal performance under different environmental conditions.

Experimental Methods

Preparation of Graphene Assembled Film and GT-TIM and Thermal Characterization

The GT-TIM was produced using multiple process steps. A well-dispersed Graphene Oxide (GO) suspension was made by shear mixing. The GO film (GOF) with a certain thickness was prepared by drying the GO suspension. Afterward, the GOFs were annealed to get GFs with micro-gasbag foam-like structures[7]. GT-TIM was produced via vertical alignment with GF, followed by immersion in a silicone polymer. After that, GF and silicone polymer mixture were cured between 100 and 120°C to complete the curing process.

The bulk through-plane thermal conductivity of GT-TIMs was measured by Laser Flash (LFA 447 instrument).[8] Contact thermal resistance and effective thermal conductivity of GTTIMs were measured using steady-state measurements according to ASTM D5470-17.[9] A thermal testing platform was built to show the superior thermal conductivity of the GTTIMs at the through-plane and in-plane directions.

Reliability Testing

A set of customized test rigs was designed and 1 mm thick, 3 × 3 cm^2 sized GT-TIM test samples were used. GT-TIM pad was compressed to 30% and further subjected to three different industry standard reliability tests i.e., thermal aging (at 120°C), temperature cycling (between –40°C and +125°C), and damp heat (at 85°C, 85% RH). The thermal contact resistance was measured sequentially during each test to monitor changes from the triplicate of test specimens. Detailed reliability characterization testing has been reported in a recent publication.[10]

Results and Discussion

Structure of GT-TIM

The operation and lifetime of a circuit board largely determine the type of TIM and application technique. The new graphene enhanced TIM contains vertically oriented graphene fillers and a silicone polymer matrix, via structural control technology, to combine these two materials effectively. GT-TIM can offer a through-plane thermal conductivity of up to 100 W/m.K.[11] Figure 1 shows an image of a GT-TIM, revealing the vertically oriented graphene creating a pathway to the other side of GT-TIM.

To apply the TIM, it should be sandwiched between the heating element and the heat sink to boost heat transfer efficiency.

GT-TIM offers reusability while maintaining the high thermal conductivity of vertically oriented graphene and is a proven technology in thermal burn-in and other industrial electronics cooling applications as compared to general-purpose grease.

Thermal Performance

As compared to thermal conductive adhesives, non-curing thermal grease materials, and other forms of low thermal conductive thermal pads and tapes, the graphene enhanced TIM (GT-TIM) can

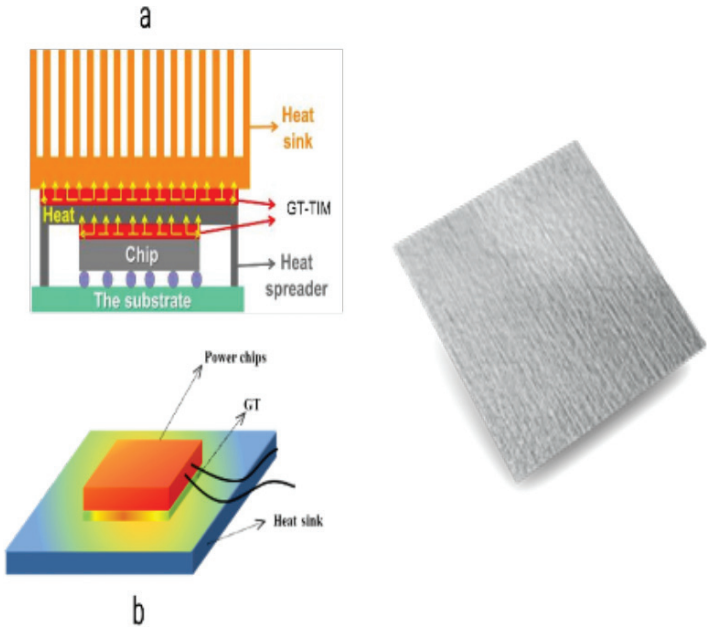

Figure 1. GT-TIM thermal interface materials for electronics and power module cooling.

offer up to 100 times better bulk thermal conductivity, 2–5 times better effective thermal conductivity and 2–5 times lower than effective thermal resistance compared to the current commercial products (Table 1).[3,11]

From Table 1, it is observed that GT-TIM shows almost comparable thermal performance to pure indium solder bonding. In addition, the GT-TIM has more advantages than indium solder bonding, including lightweight (density=0.4-0.6 g/cm^3), good maintainability, and ease of use. The resulting GT-TIM thus opens new opportunities for addressing large heat dissipation issues in form factor driven electronics and other high power-driven systems.

In addition, GT-TIM can also be re-used with ultra-longlasting performance as compared to thermal paste and other competitor products available in the market. Interestingly, GTTIM offers extremely low thermal contact resistance value compared to other non-metal-based TIM products available from the commercial market. Figure 2 shows GT-TIM effective thermal resistance vs applied pressure. GT-TIM offers very high flexibility, softness, extreme compressibility, reusability, and recovery compared to the competitor products from the market.[3]

Applications

GT-TIM is currently qualified in many potential cooling applications such as 5G, gaming, crypto mining and data server, CPU/GPU modules because of its long-lasting life compared to the commercial thermal paste. It also offers a very high compressibility, high recovery, and sustainable manufacturing processes because of high automation degree. Thus, the GT-TIM offers a very interesting energy efficient thermal management solution and saves energy up to 30% compared to commercial thermal paste.

A. 5G Wireless Module Cooling

5G wireless technology offers enhanced mobile broadband, ultra-reliable low-latency communication, and massive machine-type-communications, which enable the growth of artificial intelligence and the Internet of Things technologies. However, development and verification of an efficient ultra-high cooling materials and technology are still in an infancy stage.

Use of graphene assembled materials for ICT 5G wireless product cooling application is a great interest for telecom industry.

Figure 3 shows the percentage of the change in thermal resistance from pristine rigs to current conditioning time and total thermal interface resistance plotted against conditioning time for the damp heat specimens according to the telecom reliability testing requirements. The reliability tests of graphene-enhanced thermal pads have shown a very stable thermal performance over time, showing that GT-TIM is very stable in different environmental conditions.[10] It was also confirmed that thermal resistance levels did not worsen. GTTIM surpasses in terms of reusability under harsh temperature conditions and is expected to become the main

Table 1: Commercial TIMs and typical properties vs. GT-TIM measured with ASTM 5470 standard.

Type	Thermal conductivity (W/m.k)	BLT (um)	Thermal interface resistance (Km^2/W)	Pump-out effect	Stress absorption	Reusable
Thermal grease	0.4–4	20–150	10–200	Yes	Well	No
Thermal pad	0.8–3	200–1000	100–300	No	Well	Yes
Thermal gel	2–5	75–250	40–80	No	Medium	No
Thermally conductive adhesive	1–2	50–200	15–100	No	Medium	No
Solder	20–80	25–200	<5	No	Poorly	No
GT-TIM	50–100	150–300	5–10	No	Outstanding	Yes

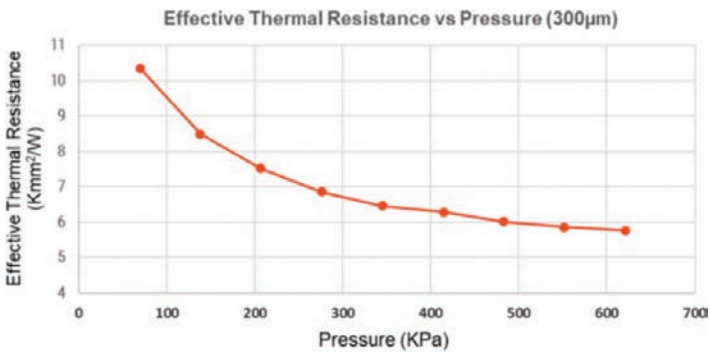

Figure 2. GT-TIM effective thermal resistance vs applied pressure.

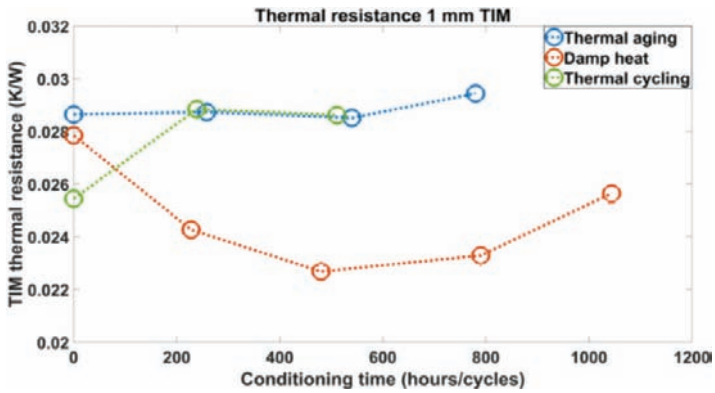

Figure 3. Reliability Characterization of GT-TIM.

component in 5G electronics device cooling and related power module cooling applications.

B. Thermal Burn-In/Test Equipment

Recently, the GT-TIM were successfully used in thermal burn-in and IC thermal testing equipment applications. Figure 4 shows an assessment of the thermal performance of GT-TIM in thermal burn-in testing with very reliable performance compared to the existing TIM used in the testing applications.

C. CPU, GPU, and Gaming Hardware Cooling

Power dissipation of central processing units (CPUs) and graphics processing units (GPUs) are often very high. The GT-TIM can dissipate heat from the modules efficiently compared to the thermal paste. Figure 5 shows that they are also highly effective in cooling of CPUs. It can offer over 10 degrees low operation temperature for gaming as compared to conventional TIM product.

Conclusions

In summary, a lightweight, compressible, and highly thermal conductive GT-TIM has been developed as a combined thermal interface material and heat-spreading material for both through-plane and in-plane thermal management applications. The high thermal conductivity and high compressibility effectively fill the voids between the heating device and the cooling device to achieve low thermal contact resistance and outperform commercial materials. The resulting GT-TIM thus opens new opportunities for addressing large heat dissipation issues in form-factor driven electronics and other high power-driven systems. GT-TIM can successfully be implemented in a 5G wireless technology cooling, thermal burn-in tester and IC thermal testing equipment, and GPU/CPU cooling as a replacement for thermal grease currently being used by many electronics manufactures. In conclusion, GT-TIM offers long-lasting cooling performance, cost-effectiveness, energy saving, easy use and is chemically stable for a long period as compared to thermal grease materials.

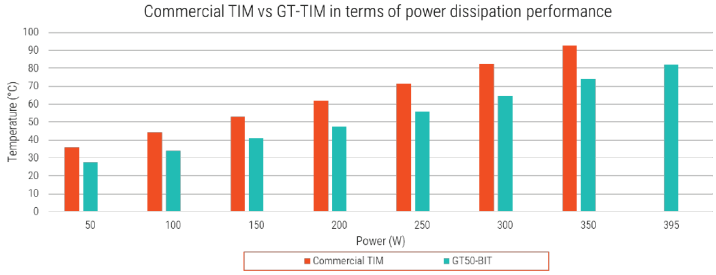

Figure 4. Assessment of Thermal performance in Thermal Burn-In Test (GT-50).

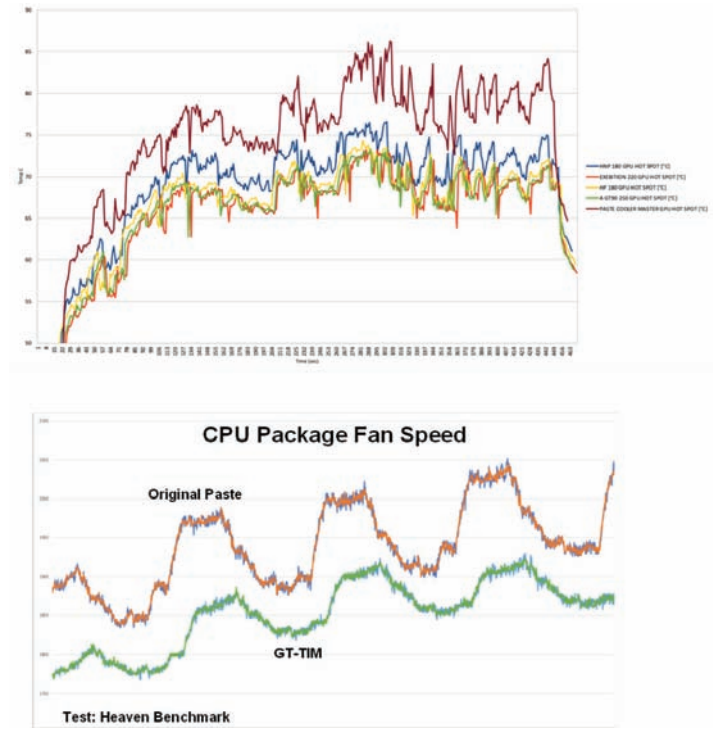

Figure 5. GT-TIM can offer more than 10°C lower operation temperature for gaming compared with commercial paste.

Acknowledgments

The authors acknowledge the funding provided by the Swedish National Board for Innovation via the SIO Grafen Program. In addition, J. Liu acknowledges the financial support from the Swedish National Science Foundation with the contract No: 621-2007-4660 and from the Production Area of Advance at Chalmers University of Technology.

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Production Testing of MEMS & Sensors

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Abstract

The number and variety of sensors in typical mobile, wearable and automotive applications has exploded in the recent past and continues to grow well into the future. It is mission critical in select customer applications to ensure each of these sensors are production tested prior to assembly into the customer platform. Production testing of sensors requires the handler to induce the accurate level of stimulus in the range of operation and test access with tester instruments to test against the datasheet specifications. This article describes the production test challenges for high volume manufacturing.

Keywords

Semiconductor, Outsourced Semiconductor Assembly & Test (OSAT), Multi-die Packages, Heterogeneous Integration (HI) [1], Test, Functional Test, Structural Test, System Level Test (SLT), Microelectromechanical Systems (MEMS), Production Test Flow.

I. Introduction

A broad range of Outsourced Semiconductor Assembly and Test (OSAT) suppliers deliver packaging and test services [2] for sensors and microelectromechanical systems (MEMS) devices for magnetometers, accelerometers, gyroscopes, microphones, pressure, inertial, optical and radio frequency (RF) applications. Each of these sensor types may have a specific range of operation. For instance, absolute pressure sensors, side crash detection sensors, tire pressure sensors and barometric pressure sensors can be different sensors designed for the specific range of operation.

Temperature, pressure and microphone sensor types are amongst the highest by production volumes, especially those that have an automotive and environmental usage rate. There are a variety of test challenges for these products in the high- volume manufacturing process. The objective of this article is to highlight a couple of important aspects that are being resolved by the test industry to reduce the overall production cycle times and hence the cost.

The RF sensors are a different category of product. RF sensors depend on radio detection and ranging (radar). In an automotive application, the transmitter sends an RF pulse, which when reflected back from a reflector and received at the receiver is used to compute the distance between two automobiles.

II. Multi-Die Package

For traditional customer applications, sensors are typically packaged separately. There are several benefits to the approach in the end application. The larger application platform can communicate with the sensor, via an application- specific integrated controller (ASIC) over a slow speed serial digital interface like I^2C, SPI, UART and/or others. There are two different functional block types within the package, one that includes an analog functional block and the other that includes a controller. Fig. 1 & 2 show the two different sensor package blocks.

More recent application architectures and designs require higher density integration and hence demanding multiple sensors [2, 3] getting integrated within a single package. Fig. 3 shows a block diagram on the left and a package model on the right. The referenced Heterogeneous Integration Roadmap, Chapter 17 does a good job of describing the challenges associated with multi-sensor product testing [6].

Depending on the sensor type and the end application, the sensor package may include a window to expose the sensor die or be over-molded or have a cavity or may require a combination of molded and cavity type. These are pictured in Fig. 4.

III. Key Test Challenges

One of the vital production test steps in the manufacturing process, is the Final Test step. Production testing of a sensor device under

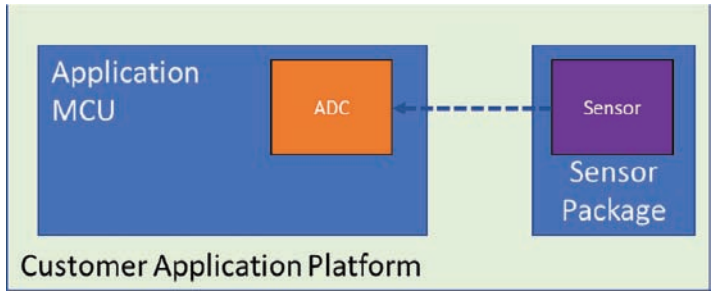

Figure 1. Sensor package, without the ADC controller block.

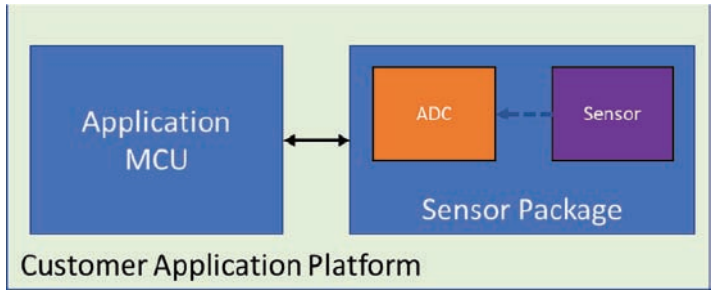

Figure 2. Sensor package, with the ADC controller block.

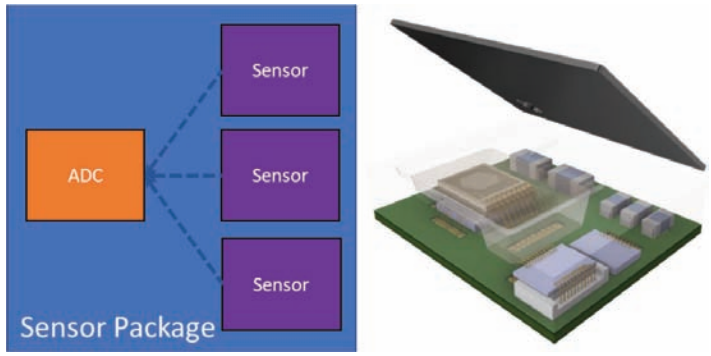

Figure 3. A multi-die sensor package may or may not include the controller.

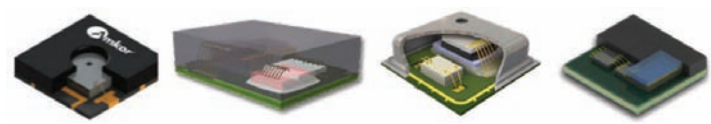

Figure 4. Example sensor packages (left to right): exposed die, overmolded, cavity and molded/cavity packages.

test (DUT) requires automated test equipment (ATE), a material handler and the test interface hardware. Fig. 5 shows the functional block depiction of the production test cell. The package handler includes a calibrated stimulus source. This source generates the stimulus that the DUT is subjected to. The ATE is electrically connected to the DUT via the test hardware and tests for all required datasheet attributes.

Product affordability and costing targets mandate multi-site testing of sensors. The magnitude of parallelism is limited by the maximum allowable parts that can be physically located on the test hardware, stimulus constraints and the number of parts the handler is able to present at the test sites.

The tester resource requirements to test most sensor types includes the appropriate count of channels on the power supply, digital and clock channels and analog test channels.

RF sensors have different requirements. RF sensor test requires RF instrumentation within the ATE. These radar sensors can include an antenna that may be integrated within the package. The continuous wave (CW) frequencies range from <10 GHz to <100 GHz with signal power <+10 dBm, depending on the end application requirements.

From a DUT setup standpoint, testing of RF sensors is challenging. The two-way RF signal path between the test head and the DUT is made up of conduction path medium that includes shielded cables and the lossy "over the air" medium. The production setup must be repeatable and reproducible and calibratable. Any deviations from acceptable limits can result in loss of yield.

While multi-sensor packages like the ones shown in Fig. 3, result in higher levels of integration, they can result in increased test times per insertion or increased count of test insertions to test each sensor, which again results in increased test time and hence increased cost. Examples of multi-sensor packages include pressure/temperature, microphone/temperature or humidity/temperature sensors.

The most popular and demanding market segment with the most stringent test requirements is the automotive market [4, 5]. The automotive industry, as of the writing of this article, is driving the most complex packaging and test services.

IV. Package Handling Challenges

Test capabilities for temperature sensors is by far relatively easily implemented in production test. Package handler manufacturers have stimulus sources integrated with package handling equipment. The number of choices of these stimulus sources is large and mostly customized by the handler supplier for each type of sensor. Sensors for microphone, magnetometer, accelerometer, pressure, relative humidity, gas detectors and others can require test signal isolation from the production environment. At the same time, product affordability warrants maximizing parallel testing. Fig. 8 shows an example of a 70 sensor placement topology being tested in parallel within a production material handler.

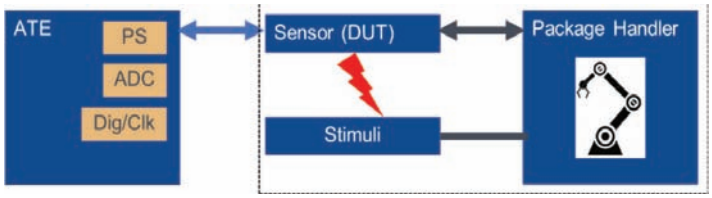

Figure 5. Functional blocks of the typical production sensor test setup.

Product-specific parallel site test hardware design, including DUT sockets, require careful design verification to ensure all sites are stimulated within the specified test limits.

Microphone testing can be sensitive to stray ambient (e.g., facility ventilation air ducts) sound sources. There are numerous stray sound sources within the production test environment that may impact the test result and production yield. In addition to isolation of stray sources of sounds, the manufacturing test cell can be sensitive to motor vibrations, floor footing vibrations, and changes in light sources, etc. Test equipment motors need to be paused for the duration of test, which may impact the overall production throughput.

Vacuum cups on the plungers to pick and place DUTs into test sites require careful design, to avoid damaging the unit. Mechanical

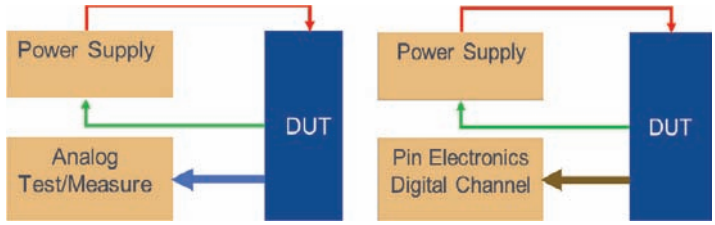

Figure 6. Power, analog and digital signal path connection. Analog connection integrity is maintained with differential signals. Digital connections are single-ended. In both cases, signal path calibration can be required.

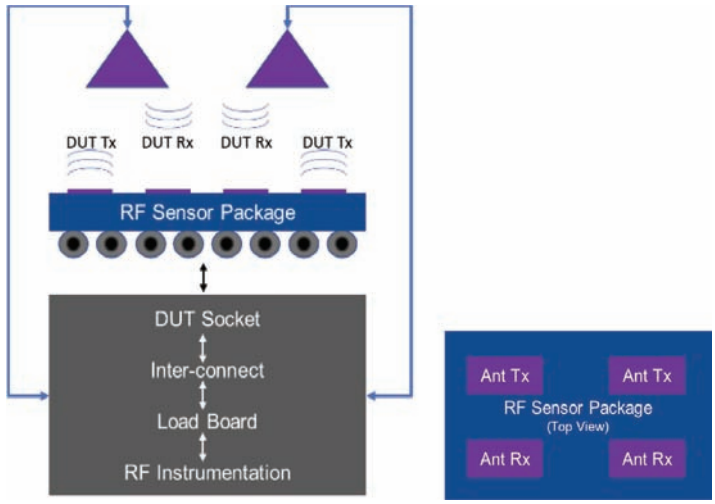

Figure 7. Shown on the left is the live "bug" view of the RF sensor production test setup. The right shows the top view of the block representation of the patch antenna placement on the top surface of the package.

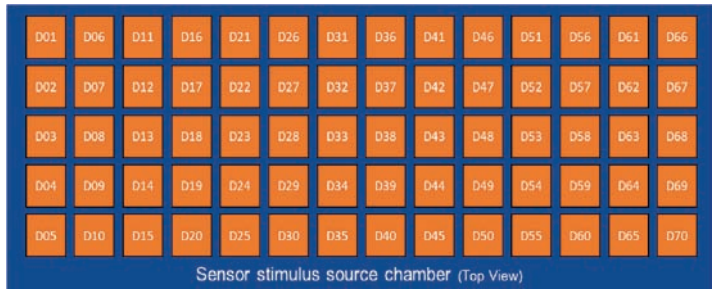

Figure 8. DUTs layed out in an insulated chamber within the production environment. The chamber includes a calibrated stimulus source that is not shown in this view.

handling of pick and place or bowl feeder handlers is designed to prevent dropping of device packages since dropped packages result in loss of manufacturing yield.

Production site facility requirements are stringent. Production yields are sensitive to variation in test facility temperature and relative humidity during the day and night. To alleviate some of the above stated challenges, handler vendors have encapsulated microphone test stimulus within an isolation chamber. The shield design isolates the DUTs from impacts for the duration of testing. The stimulus reference sound source and reference microphone require periodic calibration, depending on the production environment to ensure impairment free operation.

Pressure sensor testing, depending on the range of operation, can be sensitive to minor leaks within the test chamber of the handler. The handler pressure chamber is designed to maintain, pressure, temperature and relative humidity within the allowable specification limits. Cycling production parts through the chamber may result in condensation. This can result in additional settling times that slow down production throughput. Sensors depending on the architecture, design, and fabrication, require per unit trimming at a specific temperature and relative humidity to ensure accuracy to the product datasheet. The trimming process may or may not be completely automated and while trimming is necessary to perform, it takes time that reduces the production units per hour (UPH) metric.

Other MEMS and sensor devices have their own set of non-idealities within the handler and stimulus chamber. Multi-sensor products have continued to add complexities to the production test processes and systems. MEMS and sensor production test equipment may benefit from design for manufacturing (DFM) systemic and design improvements that will allow production sites to keep the overall manufacturing costs from increasing as the sensor product volumes grow in the future.

MEMS and sensor devices in all categories may require multiple test insertions to test the performance at the complete temperature range of operation. This varies by application. For example, the automotive range of operation can be quite wide.

The higher the site parallelism, the higher are the sources of errors that impact the overall production throughput. It takes time and effort to eliminate test equipment induced false failures and to optimize first pass yield. Re-tests of sensors can be required, to keep test equipment induced failures in-check. Methods to isolate true sensor architecture, design, fabrication and package assembly related failures are required to be accurately tagged to allow process improvements, generation over generation.

V. Test Manufacturing Metrics

There are a variety of key process indicators (KPI) that are tracked to ensure that test factory efficiencies are at the optimal levels and the out-going quality metrics for sensor production test are met. Typical factory throughput indicators include units per hour (UPH), units per month (UPM), test cell count, lot rejection rate (LRR), first pass yield (FPY), on-time delivery (OTD), customer returns, inspection failures and others.

Apart from sensor architecture, design, fabrication and packaging-related failure mechanisms (true failures), inefficiencies that result in less-than-optimal yield for sensor production testing primarily stem from consistent performance on all parallel sites within the test cell. The central reason for site failure can be the test hardware (load- board) related or inconsistent performance of the stimulus. It is important to track the aging of production test hardware to ensure that these failure mechanisms are minimized or eliminated with systemic root cause fixes.

VI. Summary

The number of sensors in recent applications is rapidly growing. Internet of Things (IoT), wearables, mobile and automotive applications are continuing to demand application-specific higher resolution, accuracy and range of operation for existing sensors. Complexities in production testing of MEMS and sensor devices continues to grow. New complexities are demanding streamlining and efficiency improvements to existing test equipment technologies, manufacturing processes and systems.

Acknowledgment

The author expresses his gratitude to Amkor's package design teams to allow sharing block level representations to surface production test complexities. The author also thanks Amkor's sensor mass production test site manager Mon Lopez for providing feedback and areas of improvements that allow consistent test factory throughput.

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