Welcome to 2024. It’s my pleasure to write to you as the incoming EPS President. I was fortunate to spend the last year as President-elect preparing for this role under Kitty Pearsall’s leadership, and look forward to her continued partnership and guidance in her role as Junior past president.

2024 promises to be an exciting year for the industry and for EPS. Our industry is never boring, but the last few years have brought us COVID-related challenges, overlapped with surprising demand in some sectors coupled with supply chain challenges, followed by strong demand across many sectors, with the market growing more than 25% between 2020 and 2022. Then in 2023, demand softened, with the market decreasing more than 10% relative to 2022. We appear to be on the upswing again, with November, 2023 seeing the first year on year growth since August, 2022. Forecasts for 2024 indicate a return to high growth. There will be high and increasing demand for skilled packaging professionals.

EPS was affected by, and responded to, these industry dynamics. For example, when COVID prevented travel and large gatherings, we pivoted to virtual conferences and workshops. We now offer live, hybrid and virtual events. As electronics have become pervasive in every type of product, and demand for qualified technologists exceed the supply, EPS has ramped its workforce development and education efforts. No matter the challenges of the day, EPS remains focused on our priorities:

• Providing high value to our members and their organizations through access to state-of-the-art training, education and literature resources, and leading professionals across the spectrum of electronic packaging. These resources include our Transactions, newsletters, webinars and podcasts, our set of Distinguished lecturers, and more than 40 EPS and joint chapters around the world.

• Offering the widest range and highest quality technical conferences and workshops that include updates on current and emerging packaging technologies and opportunities for direct engagement with peers and top industry suppliers. EPS holds events in every month and on every populated continent.

• Identifying future packaging technology requirements, defining the challenges they provide, and leading efforts to meet them. EPS initiated the Heterogeneous Integration Roadmap in 2016, and together with our partners at SEMI, ASME and the IEEE EDS and Photonics societies, we’ve created and maintain the technical document that is the basis for derivative roadmaps used by industry, governments and academia.

EPS is led by a team of dedicated and talented volunteer professionals. I feel fortunate to work with the 2024/2025 incoming and continuing Vice Presidents and Directors:

• Vice President, Technology: Dave McCann
• Vice President, Conferences: Tanja Braun
• Vice President, Publications: Ravi Mahajan
• Vice President, Finance: Jeff Suhling
• Vice President, Membership: Alan Huffman
• Vice President, Education: Eric Perfecto
• Program Director, Awards Programs: Patrick McCluskey
• Program Director, Chapter Programs: Toni Mattila
• Program Director, Industry Programs: William Chen
• Program Director, Student Programs: Mark Poliks
• Program Director, Regions 1 – 7 & 9: Annette Teng
• Program Director, Region 8 Programs: Steffen Kroehnert
• Program Director, Region 10 Programs: Andrew Tay

EPS also has a set of geographically dispersed Members at Large that fill key roles and guide much of the ongoing EPS effort. Welcome to the incoming and returning Member at Large team:

• Regions 1–6, 7, 9. Mukta Farooq, Patrick McCluskey, Mark D. Poliks, Annette Teng, Jin Yang, Luu Nguyen, Jose Schutt-Aine, Benson Chan, Wolfgang Sauter, Pradeep Lal

(continued on page 23)
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VP (Conferences): Tanja Braun, Tanja.Braun@izm.fraunhofer.de
VP (Publications): Ravi Mahajan, ravi.v.mahajan@intel.com
VP (Education): Eric Perfecto, eperfecto@gmail.com
VP (Finance): Jeff Suhling, jsuhling@auburn.edu
VP (Membership): Alan Huffman, alan.huffman@ieee.org
Senior Past President: Chris Bailey, christopher.j.bailey@asu.edu
Junior Past President: Kitty Pearsall, kitty.pearsall@gmail.com

Members At Large

2024 Term End: Regions 1-6, 7, 9—Benson Chan, Pradeep Lall, Wolfgang Sauter, Region 10—Kishio Yokouchi, Chuan Seng Tan, Chin Pin (CP) Hung

2025 Term End: Regions 1-6, 7, 9—Jose Schutt-Aine, Lau Nguyen, Region 8—Karlheinz Bock, Przemyslaw Gromala, Grace O’Malley, Region 10—Shaw Fong Wong

2026 Term End: Regions 1-6, 7, 9—Mark Poliks, Annette Teng, Patrick McCluskey, Jin Yang, Mukta Farooq, Region 10—Eiji Higurashi, Young Professional—Aakrati Jain

Publications

Transactions on Components, Packaging and Manufacturing Technology
Managing Editor: Ravi Mahajan
Co-Editor Special Topics: Koneru Ramakrishna
Co-Editor, Electrical Performance: Wendem Beyene
Co-Editor, Components: Characterization and Modeling: Yogendra Joshi
Co-Editor, Advanced Packaging Technologies: Hsien-Chie Cheng
Co-Editor, Electronics Manufacturing: Muhammad Bakir

Technical Committee Chairs

Materials & Processes: Yi Li
High Density Substrates & Boards: Takashi Hisada
Electrical Design, Modeling & Simulation: Dipanjan Gope
Thermal & Mechanical: Sreekant Narumanchi
Emerging Technology: Benson Chan
Nanotechnology: Attila Bonyar
Power & Energy: Douglas Hopkins
RF & Thz Technologies: Premjeet Chahal

Photonics—Communication, Sensing, Lighting:
Farnood Rezaie
3D/TSV:
Peter Ramm
Reliability:
Vanessa Smet
Test:
Abram Detofsky

Program Directors

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Student Programs: Mark Poliks, mpoliks@binghamton.edu
Industry Programs: William T. Chen, William.Chen@aseus.com
Region 1-7 & 9: Annette Teng, annetteteng@promex-ind.com
Region 8 Programs: Steffen Kroehnert, steffen.kroehnert@espat-consulting.com
Region 10 Programs: Andrew Tay, andrew_tay@ieee.org

Standing Committee Chairs

Fellows Evaluation: Jie Xue, jixue@cisco.com
Nominations: Kitty Pearsall, kitty.pearsall@gmail.com

Distinguished Lecturers

VP Education: Eric Perfecto, eperfecto@gmail.com
Lecturers: Ramachandra Achar, Ph.D., Mudasir Ahmed, Kemal Aygün, Ph.D., Muhannad Bakir, Ph.D., W. Dale Becker, Ph.D., Wendem Beyene, Ph.D., Karlheinz Bock, Ph.D., Bill Bottoms, Ph.D., Chris Bower, Ph.D., Tanja Braun, Ph.D., William T. Chen, Ph.D., Kuan Yew Cheong Ph.D., Xuejun Fan, Ph.D., Madhu Iyengar, Ph.D., Subu Iyer, Ph.D., Beth Keser, Ph.D., Pradeep Lall, Ph.D., John H. Lau, Ph.D., Ravi Mahajan, Ph.D., James E. Morris, Ph.D., Rajen Murugan, Ph.D., Eric D. Perfecto, Mark Poliks, Ph.D., Gamal Refai-Ahmed, Ph.D., Jose Schutt-Aine, Ph.D., John Shalf, Dongkai Shangguan, Ph.D., Rohit Sharma, Ph.D., Ephraim Suhir, Ph.D., Andrew Tay, Ph.D., Manos Tentzeris, Ph.D., Rao Tummala, Ph.D., E. Jan Vardaman, Paul Wesling.

Chapters and Student Branch Chapters

Refer to eps.ieee.org for EP Society Chapters and Student Branch Chapters list IEEE Electronics Packaging Society Newsletter is published semi-annually by the Electronics Packaging Society of the Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016-5997. US $1.00 per member per year is included in Society fee for each member of the Electronics Packaging Society. Printed in U.S.A. Periodicals postage paid at New York, NY, and at additional mailing offices. Postmaster: Send address changes to IEEE EPS Newsletter, IEEE 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved, copyright (c) 2024 by the EP Society of IEEE. Authors and Artists given full permission for further use of their contributions. For circulation information call IEEE Customer Service 800-701-4333, or FAX 908-981-9667.

EPS NEWS

Madhavan Swaminathan Receives the 2024 IEEE Rao R. Tummala Electronics Packaging Award

“For contributions to semiconductor packaging and system integration technologies that improve the performance, efficiency, and capabilities of electronic systems.”

Over his illustrious career, Madhavan Swaminathan has consistently taken a lead role in offering solutions for engineers to effectively create high-performing designs. His work has led to a fundamental understanding of power distribution networks (PDNs), design of package architectures that improve power efficiencies, and glass packaging for millimeter wave (mm wave) applications. These efforts laid the foundation for several commercially available modeling tools, along with delivering significant performance improvements for high-speed computing, wireless, and mixed signal electronic systems. Swaminathan literally wrote the book on modern PDNs, as the book he authored on the subject is now used by universities and industry worldwide.

An IEEE Fellow, Swaminathan is Department Head of Electrical Engineering, William E. Leonhard Endowed Chair, and Director of CHIMES (an SRC JUMP 2.0 Center), College of Engineering, Penn State University, Pennsylvania, USA.

2023—Guoqi (Kouchi) Zhang
“For scientific and technological leadership in “More than Moore” (MtM) packaging, co-designing, and reliability.”

2022—Douglas C. H. Yu
“For contributions to the development of advanced packaging technologies and their implementation in high-volume manufacturing.”

2021—Chin C. Lee
“For contributions to new silver alloys, new bonding methods, flip-chip interconnect, and education for electronics packaging.”

2020—Mitsumasa Koyanagi and Peter Ramm
“For pioneering contributions leading to the commercialization of 3D wafer and die level stacking packaging”

2019—Ephraim Suhir
“For seminal contributions to mechanical reliability engineering and modeling of electronic and photonic packages and systems.”

2018—William Chen
“For contributions to electronic packaging from research and development through industrialization, and for his leadership in strategic roadmapping.”

2017—Paul Ho and King-Ning Tu
“For contributions to the materials science of packaging and its impact on reliability, specifically in the science of electromigration.”

2016—Michael Pecht
“For visionary leadership in the development of physics-of-failure-based and prognostics based approaches to electronic packaging reliability.”

2015—Nasser Bozorg-Grayeli
“For contributions to the advancement of microelectronic packaging technology, manufacturing, and semiconductor ecosystems.”

2014—Avram Bar-Cohen
“For contributions to thermal design, modeling, and analysis, and for original research on heat transfer and liquid-phase cooling.”

2013—John Lau
“For contributions to the literature in advanced solder materials, manufacturing for highly reliable electronic products, and education in advanced packaging.”

2012—Mauro J Walker
“For advancing electronic manufacturing, technology and packaging worldwide through technical innovation and cooperative leadership in industry, government, academia, and professional organizations.”

2011—Rao R. Tummala
“For pioneering and innovative contributions to package integration research, cross-disciplinary education and globalization of electronic packaging.”

2010—Herbert Reichl
“For contributions to the integration of reliability in electronics systems, and leadership in research and education in electronics packaging.”

2009—George G. Harman
“For achievements in wire bonding technologies.”

2008—Karl Puttlitz Sr. and Paul A. Totta
“For pioneering achievements in flip chip interconnection technology and for semiconductor devices and packages.”

2007—Dimitry Grabbe
“For contributions to the fields of electrical/electronic connector technology, and development of multi-layer printed wiring boards.”

2006—C. P. Wong
“For contributions in advanced polymeric materials science and processes for highly reliable electronic packages.”

2005—Yutaka Tsukada
“For pioneering contributions in micro-via technology for printed circuit boards, and for extending the feasibility of the direct flip-chip attachment process.”
New Appointments for 2024

At the December 2023 EPS Board of Governors meeting, the following appointments were made for 2024.

PATRICK THOMPSON (M’87, SM’92) earned his BS, MS and PhD degrees in Chemical Engineering at the University of Missouri-Rolla. He has more than 25 years of experience in advanced packaging research, development and transfer to manufacturing, contributing to technologies ranging from flip chip fabrication and packaging, flip chip on board and chip scale packages, to multi-chip packaging, MEMS, optoelectronic packaging, and high-performance portable packaging. He has led teams at Bell Labs, AMI Semiconductors, and Motorola (now Freescale). Since 2001, he has been a Senior Member of the Technical Staff at Texas Instruments, where he currently leads fine pitch Cu pillar interconnect and TSV packaging technology development.

Pat is active in industry-consortia and industry-university partnerships, including mentoring SRC custom projects and PhD students.

Pat has five patents and over two dozen publications. He has presented packaging tutorials and given invited talks at leading packaging conferences. He is a member of the Electronic Components and Packaging Technology Conference technical program committee, where he has held multiple positions, including General Chair of the 2006 ECTC, and continues to serve as Financial Chair. He has served at both the local and Society level of EPS holding positions including Vice President of Finance, Member-at-Large of the Board of Governors, Administrative Vice President, and Vice President of Technology.

JEFFREY C. SUHLING (AF ’94, M ’01, SM ’17) Jeffrey C. Suhling received his Ph.D. degree in Engineering Mechanics in 1985 from the University of Wisconsin. He then joined the Department of Mechanical Engineering at Auburn University, where he currently holds the rank of Quina Distinguished Professor and Department Chair. From 2002–2008, he served as Center Director for the NSF Center for Advanced Vehicle Electronics. He was appointed Department Chair of the Department of Mechanical Engineering in 2008.

His research interests include solid mechanics, stress and strain analysis, material characterization, experimental mechanics, advanced and composite materials, finite element analysis and computational mechanics. He works primarily on applications of these fields to electronics packaging, including silicon sensors for stress and temperature measurement, and materials characterization and constitutive modeling of microelectronic solders and encapsulants. Dr. Suhling has authored or co-authored over 600 technical publications, and he has advised over 100 graduate students at Auburn University. He is a Fellow of ASME, and is a member of IEEE, SMTA, IMAPS, SEM, ASTM, and TAPPI.

In ASME, Dr. Suhling served as Chair of the Electrical and Electronic Packaging Division during 2002–2003, and was on the EPPD Executive Committee from 1998–2003. Dr. Suhling was the Technical Program Chair of the ASME InterPACK ’07 Conference, and General Chair of the ASME InterPACK ’09 Conference. He also served the InterPACK Conference Series as Finance Chair (2003), Track Chair for Modeling and Characterization (1999), Track Chair for Reliability (2005), and Honors and Awards Chair (2011). He was Associate Editor of the ASME Journal of Electronic Packaging from 2014–2019.

In IEEE, Dr. Suhling has been a member of the Electronics Packaging Society (formerly CPMT Society) for the past 30 years. He has served on the ECTC Program Committee (Applied Reliability) from 2003-present, and as Co-Chair of the ECTC Professional Development Course Committee from 2007-present. He was first elected to the IEEE Electronics Packaging Society Board of Governors in 2014, and has served as Member at large (2014–2016), Director of Membership Services (2016–2018), and Vice President, Education (2019–2023). Dr. Suhling has served in several roles in the ITherm Conference Series including Conference Program Vice Chair (2017), Conference Program Chair (2018), and Conference General Chair (2019). He is currently serving as Chair of the ITherm PDC Committee, and Co-Chair of the ITherm Best Paper Committee.

ERIC PERFECTO (M’95, SM’01, F’17) has extensive experience working in microelectronics. At IBM, Eric has led the development of multi-level Cu-polyimide advanced packages for high-end systems, followed by the introduction of Pb-free solder interconnects and 2.5D wafer finishing. As part of the IBM Microelectronics Division divestiture, Eric moved to GLOBALFOUNDRIES where he established a Si Photonics packaging development line. In 2019 he returned to IBM part time to establish a heterogeneous integration line in Albany. He holds a M.S. in Chemical Engineering from the University of Illinois and a M.S. in Operations Research from Union College.
An author of more than 80 technical papers and three book chapters, Eric received two Best Conference Paper Awards (2006 ESTC and 2008 ICEPT-HDP) and the 1994 Prize Paper Award from CPMT Trans. on Adv. Packaging. He holds 55 US patents and has been honored with two IBM Outstanding Technical Achievement Awards.

Eric served as the 57th ECTC General Chair, the 55th ECTC Program Chair and is the current ECTC Publicity Chair. For the last 12 years, Eric’s popular Flip Chip Fabrication and Interconnection course has been given at ECTC to great reviews. He is an EPS Distinguished Lecturer, an IEEE Fellow, and has achieved IMAPS and SPE senior membership.

Eric has represented the EPS members previously, elected 4 times to the BoG. For three years he served as the EPS Strategic Director of Global Chapters and Membership where he focused on enhancing the EPS membership value. Through his efforts, the CPMT Transactions are now part of the EPS membership. For eight years, Eric has chaired the EPS Awards Committee responsible for the EPS Mayor Awards, the Regional Awards, the PhD Fellowship, the ECTC Student Travel Awards and the ECTC Volunteer Award. He is the current chair of the Rao Tummala Electronics Packaging Award. At a local level, Eric is the membership Chair of the Mid-Hudson IEEE Section and founding member of the EPS Mid-Hudson EPS Chapter where he serves as membership chair.

DAVID MCCANN (M’89) is the VP of Technology for the Electronics Packaging Society. David was a member of the ECTC Executive Committee for 10 years and later participated on the ECTC Steering Committee for two years.

David is currently Sr. VP, Chief of Staff, Business Unit at Amkor Technology in Tempe, AZ. Prior to this role, he was at Rockley Photonics in Pasadena, CA for three years where he led packaging development for medical sensors and communications transceivers. Prior to Rockley Photonics, David was at GlobalFoundries for eight years where he was Vice President of Post Fab Development and Operations. He was responsible for GlobalFoundries internal bump and probe factories, packaging and test development for Global’s Foundry, ASIC, and RF businesses, for OSAT partnerships, supply chain qualifications and external bump-probe-assembly-test production. He led the Post Fab process and business integration between GlobalFoundries and IBM, and later was part of the team that transitioned the ASIC business to Marvell. He was based in Malta, New York.

Prior to GlobalFoundries, David was at Amkor Technology for 11 years leading flip chip technology development and the flip chip business unit. Amkor is a leading OSAT (Outsourced Assembly and Test) company, with factories across Asia. His technology and business focus was primarily on HPC, mobile, MEMS, and gaming packaging.

Prior to Amkor, David was at Biotronik GmbH, a pacemaker and implanted defibrillator supplier for 10 years, in product development, process development, and operations leadership roles.

RAVI MAHAJAN is an Intel Fellow and the Co-director of pathfinding and assembly and packaging technologies for 7-nanometer (7 nm) silicon and beyond in the Technology and Manufacturing Group at Intel Corporation. He is responsible for planning and carrying out multi-chip package pathfinding programs for the latest Intel process technologies. Ravi also represents Intel in academia through research advisory boards, conference leadership and participation in various student initiatives.

Ravi has led efforts to define and set strategic direction for package architecture, technologies and assembly processes at Intel since joining the company’s Assembly and Test Technology Development organization in 2000, spanning 90 nm, 65 nm, 45 nm, 32 nm, 22 nm and 7 nm silicon. Earlier in his Intel career, he spent five years as group manager for thermal mechanical tools and analysis. In that role, Mahajan oversaw a Thermal-Mechanical Lab chartered with delivering detailed thermal and mechanical characterization of Intel’s packaging solutions for current and future processors.

A prolific inventor and recognized expert in microelectronics packaging technologies, Mahajan holds more than 30 patents, including the original patent for a silicon bridge that became the foundation for Intel’s Embedded Multi-Die Interconnect Bridge technology. His early insights also led to high-performance, cost-effective cooling solutions for high-end microprocessors and the proliferation of photo-mechanics techniques used for thermo-mechanical stress model validation. Ravi has written several book chapters and more than 30 papers on topics related to his area of expertise.

Ravi joined Intel in 1992 after earning a bachelor’s degree from Bombay University, a master’s degree from the University of Houston, and a Ph.D. from Lehigh University, all in mechanical engineering. His contributions during his Intel career have earned him numerous industry honors, most recently the SRC’s 2015 Mahboob Khan Outstanding Industry Liaison Award, the 2016 THERMI award from SEMITHERM and the 2016 Allan Kraus Thermal Management Medal from the American Society of Mechanical Engineers. He has also been nominated as an IEEE EPS Distinguished Lecturer. He is one of the founding editors for the Intel Assembly and Test Technology Journal (IATTJ) and currently Co-Editor for Special Topics of IEEE T-CPMT. Additionally he has been long associated with ASME’s InterPACK conference and was Conference Co-Chair of the 2017 Conference. Ravi is a Fellow of two leading societies, ASME and IEEE. He was named an Intel Fellow in 2017.

ALAN HUFFMAN (M: 2005, SM: 2007) is currently the Business Unit Director for Heterogeneous Integration at SkyWater Technologies where he is responsible for business development, customer engagement. Prior, he was the Director of Engineering Micross Advanced Interconnect Technology in Research Triangle Park, NC. He received the B.S degree in physics from the University of North Carolina at Chapel Hill in 1994. From 1994 to 2005 he was a Member of the Technical Staff at MCNC Research & Development Institute working on development and implementation of wafer level packaging technologies, reliability and failure mode analysis of flip chip devices, and optoelectronic and MEMS packaging. In 2005, he joined RTI International and was a Senior
Alan is an IEEE Senior Member whose activities include, member of ECTC Interconnects technical sub-committee from 2005-2013, Chaired multiple ECTC technical sessions during this period, member of ECTC Executive Committee 2011-present, 2016–17 Jr. Past General Chair, 2015–16 General Chair, 2014–15 Vice General Chair, 2013–14 Program Chair, 2012–13 Asst. Program Chair, 2011–12 Web Administrator. Alan was appointed to the EPS Board of Governors in 2016 and has been a contributing member of the Board through various ad-hoc including Branding Change, Membership and Conference Functional Teams.

TANJA BRAUN studied mechanical engineering at Technical University of Berlin with a focus on polymers and micro systems and joined Fraunhofer IZM in 1999. In 2013 she received her Dr. degree from the Technical University of Berlin for the work focusing on humidity diffusion through particle-filled epoxy resins. Tanja Braun is head of the group Assembly & Encapsulation Technologies. Recent research is focused on fan-out wafer and panel level packaging technologies and Tanja Braun was leading the Fan-out Panel Level Packaging Consoritia at Fraunhofer IZM Berlin.

Results of her research concerning packaging for advanced packages have been presented at multiple international conferences. She also holds several patents in the field of advanced packaging.

In 2014, she received the Fraunhofer IZM research award and in 2021 the Exceptional Technical Achievement Award from IEEE Electronics Packaging Society (EPS) and the IMAPS Sidney J. Stein Award.

Tanja Braun is an active member of IEEE. She is member of the IEEE EPS Board of Governor (BOG) and was the IEEE EPS Region 8 Program Director. She is also a member of the IEEE EPS Technical Committee “Materials and Processes.”

Tanja Braun is also supporting several conferences. She was the Technical Chair of ESTC 2022 and will be the General of ESTC 2024. In addition she is also a technical committee member of ECTC, WLPS, EDTM and APC Semicon Europe.

TONI MATTILA (M’08) is a research scientist and docent at Aalto University in Helsinki, Finland where he leads a research team that focuses on the reliability of electronic devices. He received his Ph.D. degree in electrical engineering in 2005 and an M.Sc. degree in materials science and engineering in 1999 from the Helsinki University of Technology (HUT). Since 1996, he has been working with electronics production technologies and reliability of electronic devices both in industrial and academic settings. Before joining HUT in 1999 he worked in Tellabs and Nokia.

Toni’s research has focused on electronics production technologies, soldering in electronics, failure mechanisms of electronic assemblies, MEMS technologies, and the development of improved methods for reliability assessment and lifetime prediction. Within the framework of his research Toni has been working in close cooperation with the international electronics industry, research institutions and universities. His research has so far resulted in over fifty publications in scientific and technical journals and conferences. In addition, Toni has authored seven book chapters, held several professional tutorials during conferences and been a frequent speaker at conferences, seminars and technology fairs. He is also a frequent reviewer in several scientific journals, including CPMT Transactions.

Since 2008, Toni has been Chairman of the CPMT Finland Chapter. During this time he has, together with other board members, developed and revitalized local activities. More than 100 people attend seminars and events organized by the CPMT Finland chapter annually. He has also established firm connections between the CPMT chapters in Scandinavia. Toni is currently an elected member of the Board of Directors of the CPMT.

Toni also works actively in the IEEE Finland Section, where he has been a member of the executive committee since 2008 and served in various positions. Other IEEE activities include, for example, a membership of technical committees for all three Electronics System Integration Technology Conferences (ESTC). In the past he has also acted in several other positions of trust. For example, he has been the chairman of a housing association for ten years.

PATRICK McClusKEY (M: 1985, SM: 2015); (B.S. ('84) Lafayette College; M.S.('86) and Ph.D. ('91), Materials Science and Engineering, Lehigh University) is a Professor of Mechanical Engineering at the University of Maryland, College Park and the Mechanical Engineering Department’s Division Leader for Electronic Products and Systems. He has over 25 years of research experience in the areas of thermal management, reliability, and packaging of electronic systems for use in extreme temperature environments and power applications. Dr. McCluskey has published three books and over 125 peer-reviewed technical articles with over 2000 citations, including over 40 articles in IEEE journals and major EPS conferences, such as ECTC and iThERM. He has also served as technical program or general chair of IEEE conferences on high temperature electronics and integrated power electronic packaging, as well as being the organizer of the President’s panel session on Power Module Integration at ECTC 2016, and panel sessions at iThERM and ITEC. Dr. McCluskey has provided a short course on integrated thermal packaging of power electronics at ECTC and iThERM since 2013, along with short courses at IWIPP and 3D-PEIM. He is an associate editor of the IEEE Transactions on Components, Packaging, and Manufacturing Technology, and of Microelectronics Reliability. He is a senior member of IEEE and the chair of the EPS Technical Committee on Energy and Power Electronics. He has also served as IEEE EPS representative to the Future Car Workshop. He is a fellow of IMAPS and a member of ASME and TMS/AIME.
MARK POLIKS (M: 2004) is Empire Innovation Professor of Engineering, Professor of Systems Science and Industrial Engineering, Professor of Materials Science and Engineering and Director of the Center for Advanced Microelectronics Manufacturing (CAMM) at the State University of New York at Binghamton. In 2006 he established the first research center (CAMM), to explore the application of roll-to-roll processing methods to flexible electronics and displays, with equipment funding from the United States Display Consortium (USDC) and the Army Research Lab. His research is in the areas of industry relevant topics that include: high performance electronics packaging, flexible hybrid electronics, medical and industrial sensors, materials, processing, aerosol jet printing, roll-to-roll manufacturing, in-line quality control and reliability.

He has received more than $20M in research funding from Federal, New York State and corporate sources and more than $30M in equipment funding from federal and state sources. He is the recipient of the SUNY Chancellor’s Award for Excellence in Research. He leads the New York State Node of the DoD NextFlex Manufacturing USA and was named a 2017 NextFlex Fellow. He has authored more than one hundred technical papers and holds forty-six US patents. Previously, he held senior technical management positions at IBM Microelectronics and Endicott Interconnect. Poliks is a member of technical councils for the FlexTech Alliance, NBMC and NextFlex, and on the NextFlex Governing Council. He is an active member of the IEEE Electronics Packaging Society Electronic Component and Technology Conference and served and the 69th ECTC General Chair. Poliks received dual undergraduate degrees, with honors, in chemistry and mathematics from the University of Massachusetts and a Ph.D. from the University of Connecticut in materials science and engineering. He was a McDonnell-Douglas post-doctoral fellow working on solid-state magnetic resonance at Washington University, St. Louis before starting his career at IBM.

WILLIAM T. CHEN (M’92, SM’03, F’06) received his engineering education at University of London (B.Sc), Brown University (M.Sc) and Cornell University (Ph.D). He joined IBM Corporation at Endicott New York in 1963.

At IBM, he worked in a broad range of IBM microelectronics packaging products. He received IBM Division President Award for his leadership and innovation in Predictive Modelling on IBM products. He was elected to the IBM Academy of Technology for his contributions to IBM Products and Packaging Technologies. He retired from IBM in 1997. He joined the Institute of Materials Research and Engineering (IMRE) in Singapore, to initiate research in micro-electronic packaging materials and processes. He was appointed to the position Director of the Institute (IMRE) steering the growth in people, funding and research facilities and research direction for IMRE to become the leading materials science and engineering research center in the ASEAN region. In 2001 he joined ASE Group, where he holds the position of ASE Fellow and Senior Technical Advisor. In this assignment he has responsibilities for guidance to technology strategic directions for ASE Group.

He is Senior Past President of the IEEE/CPMT Society. He is the Co-Chair of the ITRS Assembly and Packaging Roadmap Technical Working Group. He is chair of the Semicon West Packaging Committee. He has been elected to be a member of the iNEMI Board. He is a member of the Technology Committee of GSA.

He has been elected to Fellow of IEEE and Fellow of ASME. He has served as an Associate Editor of ASME Journal of Electronic Packaging, and IEEE/CPMT Transactions.

ANNETTE TENG (SM: 2001) is the Chief Technology Officer at Promex Industries, a manufacturer of electronic and medical components in Silicon Valley, since 2014. She has spent most of her career in electronic component packaging and manufacturing in both corporate and academic environments. Born in Borneo (Malaysia), she left at 16 to attend Sweet Briar College in Virginia. After Graduating from University of Virginia with a Ph.D. in Materials Science, she moved to Silicon Valley and started her career in the IC world at Signetics. She has worked in components packaging and assembly at Philips Semiconductor, Linear Technology Corp. and Corwil Technology. Prior to joining Promex, she was Package Assembly Manager at Silanna in Australia for 3 years. She also worked at Hong Kong University of Science and Technology and helped launch their electronics packaging programs from 1997 to 2000. She has published at ECTC and Meptec in the area of dicing, die attach films and package delamination. She has been active in IEEE-EPS Chapter activities in Silicon Valley since 2000 and is currently the Chair of the IEEE-EPS Santa Clara Chapter.

STEFFEN KROEHNERT is a well-known component of the Packaging Community for more than 10 years. He is President & Founder of ESPAT-Consulting based in Dresden, Germany. Steffen is providing a wide range of consulting services around Semiconductor Packaging, Assembly, Interconnect Technologies and Test, mainly for customers in Europe. Utilizing his large network in industry, institutes and academic, he also supports small- and medium-sized companies as well as innovative Start-ups to find the right packaging solutions for their products and setup the supply chain from prototypes to small series and High-Volume Manufacturing (HVM).

Until June 2019, he worked for 22 years in different R&D, engineering and management positions at large IDMs and OSATs in Germany and Portugal, namely Siemens Semiconductors Regensburg (1997–1999), Infineon Technologies Regensburg and Dresden (1999–2006) and Qimonda Dresden and Porto (2006–2009), where Steffen was instrumental in developing FBGA packaging technology for DRAM products.
As Director of Technology, he helped setting up and making visible the company NANIUM Porto and Dresden (2009–2017), the largest OSAT in Europe, where Steffen has been heading R&D during introduction of System-in-Package (SiP) and technology transfer and scaling from 200 mm to 300 mm reconstituted wafer format of the leading Fan-Out Wafer Level Packaging Technology embedded Ball Grid Array (eWLB) from Infineon Technologies. After acquisition of NANIUM by Amkor Technology served as Senior Director Technology Development in Porto and Dresden (2017–2019) working with the European Business Development team. Steffen founded and chaired the European SEMI integrated Packaging, Assembly and Test—Technology Community (EiPATC) inside SEMI Europe from 2016–2020, serving now as co-chair.

His excellence in developing and innovating electronics packaging for semiconductor devices has resulted in authoring and co-authoring of 23 patent filings and many technical papers in the field of Packaging Technology. He co-edited the book “Advances in Embedded and Fan-Out Wafer Level Packaging Technologies.” Since 2011, Steffen is co-chair of the Advanced Packaging Conference (APC) committee at SEMICON Europe, which is built of 22 packaging experts from European industry, institutes and academic. Steffen is active member of several technical and conference committees at IEEE EPS, IMAPS, SMTA and SEMI. He holds a M.Sc. degree in Electrical Engineering and Microsystems Technologies from the Technical University of Chemnitz, Germany.

ANDREW TAY (M1991, SM2019, F2023) is currently a Visiting Scientist at the Singapore Hybrid-Integrated Next-Generation μ-Electronics Centre (SHINE), National University of Singapore (NUS). Prior to this he was a Senior Research Fellow at the Singapore University of Technology and Design and Professor in the Department of Mechanical Engineering, NUS. He obtained his B.E. (Hons I and University Medal) and PhD in Mechanical Engineering from the University of New South Wales, Australia. His research interests include thermo-mechanical reliability, thermal management of electronics and EV battery systems, reliability of solar photovoltaic modules and fracture mechanics. To date he has published more than 250 technical papers, four book chapters, seven keynote presentations, 11 invited presentations and three panel discussions.

Dr. Tay was the General Chair of the 1st Electronics Packaging Technology Conference (EPTC) in 1997. In 2006 he was appointed the inaugural Chairman of the EPTC Board and is currently serving as its Chairman. He has been in the Executive Committee of the IEEE Singapore RS/EPS/EDS Chapter since 2000 and was its Chairman from 2010–2011 and 2018–2019. He has been involved in the international advisory boards and program committees of many electronics packaging conferences including DTIP, ECTC, EMAE, EPTC, EuroSimE, HDP, ICEPT, IEMT, IMPACT, InterPack,ITHERM and THERMINIC.

He was an Associate Editor of the ASME Journal of Electronic Packaging, an editorial board member of several journals including Microelectronics Journal and Finite Elements in Analysis and Design, and a guest editor of special issues of Microelectronics Reliability Journal, and Journal of Electronics Packaging. He is currently Co-Editor-in-Chief, Encyclopedia of Packaging Materials, Processes, and Mechanics.

He was a member of the EPS Education Committee from 1998 to 2007, and the coordinator of the Singapore Economic Development Board’s Specialized Manpower Program in Electronics Packaging and Wafer Fabrication in NUS. He has been awarded competitive research grants exceeding $14 Million for electronics packaging projects.

He was awarded the 2019 IEEE EPS David Feldman Outstanding Contribution Award, the 2012 IEEE EPS Exceptional Technical Achievement Award, the 2012 IEEE EPS Regional Contributions Award, the 2004 ASME Electronics & Photonics Packaging Division Engineering Mechanics Award, the 2000 IEEE Third Millennium Medal and the 2000 Special Presidential Recognition Award.

Newly Elected Members of the Electronics Packaging Society Board of Governors

In 2023, EPS members elected new Members-at-Large to the EPS Board of Governors for the three-year term of 1 January 2024 through 31 December 2026:

REGIONS 1-6, 7 & 9

DR. MUKTA FAROOQ (M’10; SM’12; F’16) is an IBM Distinguished Research Scientist, IBM Lifetime Master Inventor with 232 granted US Patents, and a member of the IBM Academy of Technology. She is an IEEE Fellow, and a Distinguished Alumna of IIT Bombay. She is currently the Heterogeneous Integration Technology Leader at IBM Research, working on 2 nm CMOS 3D TSV integration and fine pitch die-stacking for AI Computing.

Her expertise includes semiconductor materials and structures, Heterogeneous Integration, 3-Dimensional (3D) Integration, flip-chip and die stacking technology, lead-free alloys, C4, Cu hybrid bonding, micropillar, ball/column grid arrays, chip package interaction, CMOS FET BEOL (Back End of Line) processing, packaging technology, and intellectual property development. She was awarded an Outstanding Technical Achievement Award for her pioneering and sustained contributions to IBM’s 3D Technology.

She has several patents designated as high value because of their use in semiconductor manufacturing. Her patents and intellectual property contributions are in multiple areas of semiconductors and microelectronics packaging: (1) Lead-free alloys and structures for C4, Ball Grid and Column Grid Arrays (2) Crackstop and chip package interaction improvement structures and processes (3) High BEOL TSV integration and evaluation (4) TSV proximity effect mitigation structures (5) Wafer level bonding structures to enable
tight die-die coupling (6) Bond and assembly (7) Capillary underfills (8) Heterogeneous Integration structures including surface bridges, die-stacking, wafer level processing (9) Architectures enabling AI compute. Key portions of this IP and know-how have been used in IBM mainframes and in several products such as the Hybrid Memory Cube [© Micron Technology] logic controller. Some of this IP is planned to be deployed in future generations of IBM AI Units.

Mukta has contributed technology papers to major conferences [such as ECTC 2022, IRPS 2015, IEDM 2011], given invited talks/papers [iMAPS, IRPS, others], and taught short courses at key technical conferences [3D Integration courses at IEDM, EDTM, SEMICON West, and the SOI-3D-Sub Vt conference].

Mukta is the Founding Member and current Chair of the EPS Mid-Hudson Valley Chapter that has membership along the Hudson Valley area, from Albany to Yorktown Heights, New York. She has organized with other volunteers several lectures and mini symposia in advanced packaging technology. She is also on the EPS Fellows Evaluation Committee [2023 and 2024]. She is an IEEE EDS Distinguished Lecturer and an invited lecturer to Women in EDS. Mukta has previously served 2 terms [3 years each] as an elected Member at Large of the Electron Device Society Board of Governors and has actively supported EDS for the last 15 years, including as Chair of the EDS Mid Hudson Valley Chapter. Mukta was awarded the 2022 IEEE EPS award for sustained lifetime contributions to electronic packaging. In 2021, she received the IEEE Region 1 Technological Innovation Award. She is active in mentoring professionals in engineering & technology.

Mukta holds a Ph.D. in Materials Science & Engineering from Rensselaer Polytechnic Institute, an M.S. in Materials Science from Northwestern University, and a B.Tech [Technology] in Metallurgical Engineering from the Indian Institute of Technology, Bombay.

STATEMENT OF INTEREST

Since the slowing down of logic scaling and the reticle size restrictions created by the use of EUV high numerical aperture, it has become widely accepted that Chiplet Technology and Heterogeneous Integration are a mandate for future high-performance computing. As the Heterogeneous Integration Technical Leader at IBM Research, I have been working with my colleagues on development and hardware build using advanced packaging technologies, to enable AI architectures.

To this end, I founded the EPS Mid Hudson Valley Chapter in 2020 along with my colleagues, both to learn from EPS lecturers, and to enable our teams to engage with others from industry and academia. I am always encouraging colleagues, especially the newer ones to join IEEE EPS, and become a part of this community, for their education and continued growth. Along with other chapter officers, we have arranged EPS Distinguished Lectures and mini symposia, which have been well-received.

I have previously served 2 terms [3 years each] as an elected Member at Large of the Electron Device Society Board of Governor. This experience has been very valuable in terms of understanding how BoG members can help the society flourish in activities to benefit its constituents.

I believe that interactions among peers who work in similar fields can lead to progress and innovations. I also believe that we need to be proactive in training and teaching the next generation of packaging engineers to excel and develop unique solutions for advanced packaging technology. Unlike Si Fabrication courses, Electronic Packaging technology is not taught at most universities, so engineers have to learn on the job.

EPS can play a vital role in this education, by creating training modules for short courses and special topics. I would like to serve on the EPS BoG to further this mission and provide any help and expertise that I can. I would also like to increase membership in EPS, by spreading the word about the benefits of the society to college grads and professionals, and enabling discounted or free first year EPS memberships. I believe that the next few years will see a tremendous increase in the interest in packaging technology. As an EPS BoG member, I would be able to help drive the above missions, and bring in newer professionals into volunteer roles to create a self-sustaining and vital society for the benefit of its members.

DR. PATRICK MCCLUSKEY (St M’85; M’91; SM’15) Ph.D., Materials Science and Engineering, Lehigh University) is a Professor of Mechanical Engineering at the University of Maryland, College Park, and the Mechanical Engineering Department’s Director of Undergraduate Studies. He has over 25 years of research experience in the areas of thermal management, reliability, and packaging of electronic systems for use in extreme temperature environments and power applications. Dr. McCluskey has published three books and over 200 peer-reviewed technical articles with over 4000 citations, including over 40 articles in IEEE journals and major EPS conferences, such as ECTC/iTHERM. He has also served as Technical Program Chair and General Chair of multiple IEEE international conferences on high temperature electronics and integrated power electronic packaging. Dr. McCluskey has provided a short course on integrated thermal packaging of power electronics at ECTC and iTHERM since 2013, along with short courses on integrated power electronics at IWIPF, WIPDA, and 3D-PEIM. He has also worked to build collaborations with other IEEE societies that are complementary to EPS, including PELS and the Reliability Society. He is an associate editor of the IEEE Transactions on Components, Packaging, and Manufacturing Technology and a member of the Thermal/Mechanical Simulation and Characterization committee for ECTC. He has been a member of IEEE ESP since 1995; a senior member since 2015; and is currently a member of the EPS Board of Governors and their Awards Chair. He is a fellow and member of the Board of Directors of IMAPS and a member of ASME.

STATEMENT OF INTEREST

My first goal should I be re-elected to the Board of Governors will be to continue to improve the Awards process. Since becoming the awards director, a new service award has been created and an award for excellence in thermal packaging is being developed with iTHERM. The student travel grant program for ECTC has also been expanded from 10 awards to 15 awards for ECTC, with an additional 6 awards each for EPTC and ESTC, all while ensuring greater representation from female and other historically under-represented student groups.

In addition to my efforts as awards director, I would also like to continue to champion an expansion of the IEEE Electronic Packaging Society’s efforts in the area of integrated power packaging and
bring those efforts closely into alignment with the Heterogeneous Integration Roadmap. The distribution and conversion of power is a critical element in these heterogeneously integrated units, requiring packaging developments in the areas of additive manufacturing, embedded technologies, thermal isolation and management, passive components, high temperature operating capability, materials with improved thermal and/or electrical conductivity, thin insulating layers with higher breakdown strength, and routing and distribution theory. I have championed these efforts as past Technical Chair for Energy and Power Electronics, as a co-author of the Power Electronics chapter of the Heterogeneous Integration Roadmap, as the past Technical Program Chair of the IEEE Workshop on Integrated Power Packaging (IWIPP) and as the co-founder and past General chair of the IEEE International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM). In these roles, I have created integrated teams from IEEE EPS, IEEE PELS, and PSMA to make these efforts successful.

As a member of the Board of Governors, I have also participated in the Education and Membership committees to expand outreach to students and produce educational content, and I am interested in continuing and expanding my roles on those committees.

MARK D. POLIKS (M’04) is a SUNY Distinguished Professor and Empire Innovation Professor in Systems Science and Industrial Engineering and Materials Science and Engineering, and the Director of the Center for Advanced Microelectronics Manufacturing (CAMM) at the State University of New York at Binghamton. In 2006 he established the first research center (CAMM), to explore the application of roll-to-roll processing methods to flexible electronics and displays, with equipment funding from the United States Display Consortium (USDC) and the Army Research Lab. His research is in the areas of industry relevant topics that include high performance electronics packaging, flexible and additive hybrid electronics, medical and industrial sensors, RF, high temperature and power electronics, thin-die handling and placement, materials, processing, aerosol jet printing, roll-to-roll manufacturing, in-line quality control and reliability. He has received more than $50 M in research funding from federal, New York State and corporate sources and more than $30 M in equipment funding from federal and state sources. He is the recipient of the SUNY Chancellor’s Award for Excellence in Research. His lab is a New York State Center of Advanced Technology and home to the SUNY Chancellor’s Award for Excellence in Research. His lab is a New York State Center of Advanced Technology and home to the New York State Node of NextFlex Manufacturing USA. He was named a 2017 NextFlex Fellow. He has authored more than 138 technical papers and holds forty-nine US patents. Previously he held senior technical management positions at IBM Microelectronics and Endicott Interconnect. Poliks is a member of technical councils for the FlexTech Alliance, NBMC and NextFlex, and the NextFlex Governing Council. He is an active member of the IEEE Electronics Packaging Society Electronic Component and Technology Conference and served as the 69th ECTC General Chair. He has served as a member-at-large of the Electronics Packaging Society Board of Governors since 2020 taking the responsibilities as Director of Student Programs for the last two years. He is an EPS Distinguished Lecturer. Poliks received dual undergraduate degrees, with honors, in chemistry and mathematics from the University of Massachusetts and a Ph.D. from the University of Connecticut in materials science and engineering. He was a McDonnell-Douglas post-doctoral fellow working on solid-state magnetic resonance at Washington University, St. Louis before starting his career at IBM.

STATEMENT OF INTEREST

I have been an active member of IEEE and the Electronics Packaging Society (EPS) for twenty years. I have served the IEEE EPS ECTC community as a subcommittee member and subcommittee chair (for both materials and processing and interactive presentations), an executive committee member including 2019 ECTC General Chair and as past general chairs. My career has been nearly exclusively dedicated to advancement of materials, processing, fabrication, and performance of electronics packaging technologies. I have worked the first half of my career in industry (at the IBM Corporation and Endicott Interconnect) while part-time as a research professor and the second half as a full professor and tenured faculty member at the State University of New York, Binghamton. During this time the importance of electronics packaging has continued to rise and is currently one of the primary means to achieve continued improvements in systems integration and performance. The IEEE Electronics Packaging Society has a unique opportunity to grow in membership, importance, and relevance within the larger IEEE community. EPS growth is essential to help to foster dialogue and collaboration within the industry on the advancement of packaging and interconnect technologies. I seek to continue and advance my active role in IEEE EPS and its BOG to help grow the outreach of EPS through new membership, continued development of student chapters, heterogeneous integration roadmap working groups, conferences, peer-reviewed publications, and electronic packaging education worldwide.

ANNETTE TENG (AM’97; M’97; SM’01) is Director of Package Integration at AIM Photonics TAP Facility. She was previously the Chief Technology Officer at Promex Industries. She has spent most of her career in electronic component packaging and manufacturing in both corporate and academic environments. Born in Bornean Malaysia, she left at 16 to attend Sweet Briar College in Virginia. After Graduating from University of Virginia with a Ph.D. in Materials Science, she moved to Silicon Valley to join Signetics. She has worked in components packaging and assembly at Philips Semiconductor, Linear Technology Corp. and Integra. She was Package Assembly Manager at Silanna in Australia. She also worked at Hong Kong University of Science and Technology and helped launch their electronics packaging programs from 1997 to 2000. She has published at ECTC and Meptec in the area of dicing, die attach films and package delamination. She has been active in EPS Chapter activities in Silicon Valley since 2000 and was the Chair for multiple years. Currently, she is the EPS Program Director of Region 1-7 & 9.

STATEMENT OF INTEREST

I have been active at the grass-root level of EPS chapter development and growth since helping form the CPMT chapter at the
opportunities for all who are interested in electronic packaging. Our community through dissemination of knowledge and provide activities and I am committed to ensure that EPS stays relevant to Clara Valley Chapter to hold technical meetings bimonthly, annual conference celebrating its 40th year in 2024. A recent outreach where I help initiate was in DTMES in Ethiopia. I help lead Santa Valley in 2000, I have been an officer of the local Santa Clara Valley chapter which at the time was the host for IEMT. Following trends where manufacturing moved from US to Asia, IEMT was moved to Malaysia which has now become the premier packaging conference celebrating its 40th year in 2024. A recent outreach where I help initiate was in DTMES in Ethiopia. I help lead Santa Clara Valley Chapter to hold technical meetings bimonthly, annual conferences (HIR and REPP), activities with students and company visits. I enjoy grooming new engineers in packaging and EPS activities and I am committed to ensure that EPS stays relevant to our community through dissemination of knowledge and provide opportunities for all who are interested in electronic packaging.

DR. JIN YANG (M’09; SM’17) is a Senior Principal Packaging Engineer with Advanced Packaging Group, Samsung Semiconductor and his current role is to oversee advanced packaging architecture (2.5D/3D) and chiplet heterogeneous integration R&D. His responsibilities expand to drive packaging technology innovation to bridge gaps between increasing computing demands and memory wall and power wall. Dr. Yang has over 15 years of experiences in microelectronic packaging and his interests include electronic and photonics packaging, wafer BEOL, process, and silicon-to-package-to-system electronics cooling. Prior to his role in Samsung, he worked as architect for Assembly & Test Technology Development, and Datacenter & AI Groups with Intel Corporation for over 13 years expanding his experiences from wafer BEOL, wafer and die sort, IC packaging (flip chip, fan out, and 2.5D/3D IC packaging), to electronics cooling with focus on disruptive packaging technology innovation for meeting next-gen and beyond CPU/AI chip needs. He also worked as a Senior Principal Engineer with NXP Semiconductor driving packaging innovation for automotive chips. Dr. Yang holds over 25 US patents and has published over 30 peer-reviewed journal and conference papers in areas of electronic packaging and microelectronics cooling. Jin Yang obtained PhD degree from Georgia Institute of Technology in the area of electronic packaging and received his master’s and bachelor’s degrees from Texas A&M University and Tsinghua University respectively.

Dr. Yang is an elected IEEE Senior Member and serves as a Member-at-Large in IEEE EPS Board of Governors (BoG) for 2021–2023 term. He has made contributions to BoG Conference and Technology Groups during his 1st term in EPS BoG. He has attended BoG meetings in person and virtually during the pandemic, regularly attended conference and technology group meetings and cast voting to BoG proposals. He has served in IEEE ECTC Assembly and Manufacturing Technology (AMT) committee for over 13 years in a row since 2010 and served as Assistant Chair and Chair in 2019 and 2020 respectively. He served as the session chair for ECTC multiple times, including ECTC’2023. During the last seven years, he served as Track Chair for IEEE ITERM since 2016. He has also been actively engaged in volunteering activities to IEEE EPS Silicon Valley Chapter since he recently moved to Silicon Valley. Dr. Yang has also served as liaison in Semiconductor Research Corporation (SRC) Programs on behalf of Intel and Samsung for over 6 years, lately JUMP 2.0 Program which is launched in 2023. He has helped strengthen collaboration between the industry and research institutions and promoted R&D in area of electronic packaging with researchers and graduate students worldwide.

Outside IEEE, Dr. Yang has a long history of continued service to ASME community in the area of electronic and photonics packaging and has taken a leadership role in ASME Electronic and Photonic Packaging Division (EPPD). He has been elected to ASME EPPD Executive Committee (2022–2026 term) to lead and drive agenda for ASME EPPD and flagship conference InterPACK. He served as General Chair of InterPACK in 2020 and successfully organized online meeting by overcoming numerous challenges in unprecedented pandemic. Prior to that, he served as Program Co-Chair for InterPACK in 2019. Meanwhile, he has served as track chair for InterPACK in the last six years. He is Associate Editor for ASME Journal of Electronic Packaging (JEP) since 2019 and has started his 2nd term through 2025. He is also Associate Editor for ASME Open Journal of Engineering. He received the AE of the Year Award from JEP.

STATEMENT OF INTEREST
If I have an honor to be selected into IEEE EPS Board of Governors, I would like to continue my service and contribution to Technology and Conferences Groups within BoG, especially tasks I pick up in my 1st term to strengthen collaboration between the industry and academics/national labs through technology collaboration and conference organization. In the area of microelectronics packaging, it has become more and more crucial to tie with the industry for promoting novel technology development and commercialization. I have established strong connections with many faculties and researchers from universities and National Labs through IEEE BoG, SRC and joint R&D programs between Intel/Samsung and research institutions and have made contributions to these programs and research proposals for fulfilling technology roadmap pipelines in the areas of chiplet based heterogeneous integration and microelectronics cooling. Meanwhile, I have rich experiences in promoting technology from concept/pathfinding to development and then to deployment for HVM. One big program I contributed to has been in full HVM production through over several years of pathfinding and development with big investment. One program I led went into HVM production and it helps save over tens of millions of dollars per year. I would like to serve as a bridge between the industry and academics/national labs to further strengthen technology collaboration to tackle great challenges for advanced packaging through the platform of IEEE EPS BoG. I also plan to further strengthen interaction between IEEE EPS BoG and IEEE EPS Silicon Valley Chapter (SVC). IEEE EPS SVC is very active based in the heart of Silicon Valley and there are more opportunities for BoG to support this local chapter to grow stronger by promoting connections of professionals and experts from all over the world with this local chapter and attract more local members/volunteers into this local chapter from many high-tech semiconductor companies in Silicon Valley.
Przemyslaw Gromala is a senior simulation expert at Robert Bosch GmbH, Automotive Electronics in Reutlingen, Germany. He currently leads an international simulation team and an FEM validation and verification laboratory, focusing on the implementation of simulation design of electronic control modules and multi-chip power systems for hybrid drives. His technical expertise includes materials characterization and modeling, multi-domain and multi-scale simulation including fracture mechanics, V&V techniques, and prognostics and health management of safety-relevant electronic control systems. Established an extensive international network within Robert Bosch GmbH (AE and other business units) and between top universities (TU Delft, TU Chemnitz, University of Maryland, Auburn University, IISC Bangalore) and R&D institutes (FhG ENAS, IMEC, RE.SE) in Europe and worldwide (USA, China, India). He established direct contacts between Bosch and semiconductor industry leaders: e.g., Intel, Xilinx, Infineon, On-Semi.

Before joining Bosch, Mr. Gromala worked at Delphi (now Aptiv), at the European Development Center in Krakow, Poland, and at the Infineon R&D Center in Dresden, Germany.

He holds a PhD in mechanical engineering from the Cracow University of Technology.

Przemyslaw Gromala is an active member of IEEE EPS conference committees:
- ECTC (TMSC co-chair 2017/18, TMSC chair 2018/19 and 19/20),
- EuroSimE (since 2016, various roles),
- REPP symposium—committee member and European liaison (2020 and 2021)
- iTherm (Mechanics and Reliability co-chair 2019 and 2020, Mechanics and Reliability track chair 2021 and 2022, Panel co-chair 2021 and 2022)
- ASME: InterPACK (Automotive tract co-chair 2017, Automotive track chair 2018, 19, technical program co-chair 2020, technical program chair 2021, General conference chair 2022)
- He is a chair of the IEEE EPS TWG Reliability since 2022, before he was a co-chair for 2 years.

Przemyslaw Gromala contributes to the IEEE EPS community by presenting his work at many conferences and professional development courses (EuroSimE, ECTC/iTherm). He has served/organized panels at many of these events (IEEE iTherm, ECTC, EuroSimE), on a variety of topics including materials characterization, numerical modeling, and prognostics and health management of electronics used in harsh environments.

He actively contributes to the IEEE EPS Heterogenous Integration Roadmap in three chapters:
- Automotive
- Simulation and Co-Design
- Reliability (as of 2021)

In addition to his IEEE activities, he is a member of the EPoSS (Chair of the EPoSS ID 2019 document, Quality, Reliability and Safety chapter) and ECS (Chair of the ECS SRIA 2020 chapter, Quality, Reliability, Security and Cyber Security chapter) committees—defining R&D and innovation needs as well as policy requirements related to the integration of smart systems and integrated micro- and nanosystems in Europe.

Przemyslaw Gromala is the author and co-author of more than 50 papers in journals and conferences and two book chapters.

STATEMENT OF INTEREST
To whom it may concern,

My contribution to EPS community:
There are four major topics that I would like to bring as my contribution to the IEEE EPS society:
1) My main area of expertise is numerical simulation of electronic control systems with an emphasis on materials characterization and modeling of epoxy-based thermostet materials. I would like to take a closer look at two specific simulation topics that I believe need further development:
a) The first one is the implementation of the compact digital twin concept. In the case of thermal domain, there are that allow implementing digital twin for electronic control modules. Model order reduction is one technique that allows efficient modeling. However, for the thermomechanical domain, especially when nonlinear effects dominate, currently only machine learning based models can be used. Further collaboration between academia and industry is needed. This is what I would like to strengthen through IEEE EPS society.
b) Among the possible solutions, I would like to contribute to the development of a new standard that allows the exchange of information using compact models (with a focus on the thermo-mechanical domain) throughout the supply chain, while still maintaining intellectual property. Having such a compact model would accelerate the development process of electronic device modules and systems.

2) The second important aspect that I would like to contribute is the prognostics and health management (PHM) of electronic components and electronic control systems. PHM for electronics is already available at the academic level but has not yet been industrialized. Unplanned downtime is a major concern for customers. PHM will be a tool to enable predictive maintenance to ensure availability. PHM will also provide a better understanding of the stresses experienced by electronic components and systems.

3) I would like to create a link between quality and reliability. Here, one technique that has great potential is artificial intelligence and machine learning. Model-based engineering can be one of the prominent methodologies that will benefit from this. This will have a significant effect of reducing development costs.
4) Finally, I would like to be an active representative of IEEE EPS in Europe. To be an “ambassador” of the IEEE EPS conferences, I am more than happy to answer any questions you might have. Should you have any additional questions, please don’t hesitate to contact me: przemyslawjakub.gromala@de.bosch.com. I will be more than happy to answer any questions you might have.

Thank you for considering my candidacy.

Best regards,
Przemyslaw Gromala

REGION 10

EIJI HIGURASHI (M’10; SM’17) received the M.E. and Ph.D. degrees from Tohoku University, Sendai, Japan, in 1991 and 1999, respectively. From 1991 to 2003, he was with Nippon Telegraph and Telephone Corporation (NTT), Japan. From 2003 to 2017, he was an Associate Professor with The University of Tokyo, Japan. From 2017 to 2022, he was a team leader or a group leader with The National Institute of Advanced Industrial Science and Technology (AIST). Since 2022, he has been a Professor in the Department of Electronic Engineering, School of Engineering, Tohoku University.

He is a Senior Member of the Institute of Electrical and Electronics Engineers (IEEE), the Institute of Electrical Engineers of Japan (IEEE), and the Institute of Electronics, Information, and Communication Engineers (IEICE). He is a member of the Japan Institute of Electronics Packaging (JIEP), the Japan Society for Precision Engineering (JSPE), the Japan Society of Applied Physics (JSAP). He is an active member of the IEEE EPS Japan Chapter and served as the Secretary from 2013 to 2014, the Vice Chair from 2019 to 2020, and the Chair from 2021 to 2022. He has served as the General Chair of the International Conference on Electronics Packaging (ICEP) from 2020 to 2021. He served as the Editor-in-Chief of Editorial Committee of the Journal of The Japan Institute of Electronics Packaging and has served as an Editor-in-Chief of Editorial Committee of the Transactions of The Japan Institute of Electronics Packaging.

He has authored or co-authored more than 300 journal and conference papers. He was a recipient of the Igarashi Award from the Sensors and Micromachine Subsociety of the Institute of Electrical Engineers of Japan in 2002, the Okawa Publications Prize from the Okawa Foundation for Information and Telecommunications in 2003, the Ichimura Academic Award from the New Technology Development Foundation in 2008, the International Conference on Electronics Packaging Best Paper Award in 2013 and 2016, 18th International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers 2015) Outstanding Paper Award in 2015.

STATEMENT OF INTEREST

Dr. Eiji Higurashi has been engaged in R&D of low temperature bonding technologies and their application to sensors, optical Microsystems, and electronic devices.

He proposed various low-temperature bonding methods, especially room-temperature bonding methods using surface activation. He has developed low-temperature bonding process (from room temperature to 150 °C) of optical chips (e.g., laser diodes) based on Au-Au surface-activated bonding instead of conventional AuSn bonding (bonding temperature: 300 °C). Passive alignment technology based on the low temperature bonding was also developed. The passive alignment and mounting of lithium niobate (LiNbO3) chips, with a large mismatch in the coefficient of thermal expansion with most semiconductors, were demonstrated for hybrid-integrated optical modulators on Si substrate. This technology enables us to integrate various optical chips precisely in three-dimensions and has opened up many new possibilities in constructing small, reliable, and highly functional optical microsystems. Furthermore, low-temperature bonding is essentially energy saving process because long high-temperature annealing is not necessary. One of his outstanding achievements is development of compact and thin optical microsensors (micro-encoders) with 3-D structure (2.8 mm × 2.8 mm × 1 mm thick). The design and fabrication process allows wafer-level chip-size packaging. The small size, together with the small degree of inertia, makes it easier for the microencoders to be incorporated into small, high-speed actuators for precision instruments.

YOUNG PROFESSIONAL

DR. AAKRATI JAIN (M’21) is a Hardware Engineer at IBM Research’s AI Hardware Center in Albany, NY. Her work has a strong focus on advanced packaging for Heterogeneous Integration in high-computational applications like AI and Machine Learning.

Dr. Jain holds a B. Tech. degree in Mechanical Engineering (2013) from Indian Institute of Technology Kharagpur, India, and a direct Ph.D. in Mechanical Engineering (2019) with a specialization in heat transfer and electronics cooling from Purdue University in West Lafayette, Indiana.

Since joining IBM Research in January 2020, Dr. Jain has been actively involved in various aspects of packaging, particularly in heat transfer, cooling, and thermal characterization of electronic packages for high-bandwidth applications. Her research endeavors revolve around understanding the factors influencing the thermal performance of electronic packages, aiming to enhance their efficiency and reliability.

In addition to her role as a Hardware Engineer, Dr. Jain holds the position of Lead of Operations for IBM’s Chiplet Packaging Lab. She is responsible for enabling bond and assembly processes, and expertised lies in laser-based wafer separation techniques. Dr. Jain also serves as the technical lead in IBM’s joint development endeavors with their dicing technical partner. In this role, she spearheads the definition and strategic direction of wafer separation processes for IBM Research’s advanced packaging initiatives.

Throughout her career, Dr. Jain has actively contributed to the field of electronics cooling and packaging. Her research has been published in renowned journals and presented at international conferences such as IJHMT, IEEE ECTC, and ITherm. She has authored more than 15 peer-reviewed articles and filed multiple technical patents, showcasing her innovative thinking and contributions to the industry.
Outside of her research, Dr. Jain actively participates in professional organizations and community initiatives. She currently serves as the Secretary for IEEE EPS’s newly-formed Mid-Hudson Valley (MHV) chapter. Under her leadership, the chapter has successfully organized two well-attended Mini-Colloquiums, featuring industry experts who shared insights on relevant topics in electronics packaging. Under her tenure, the chapter also organized a lecture series and a virtual seminar. Additionally, she serves as an industry liaison for the Semiconductors Research Center (SRC), where she mentors students and selects research projects in the packaging domain, with a specific focus on materials and technologies for thermal management and cooling of advanced packages.

**STATEMENT OF INTEREST**

In this position, I am committed to contributing my skills and expertise to advance the field of electronics semiconductor and packaging. Through my membership in EPS, I aim to undertake the following key initiatives:

1) **Educating Undergraduate and High-School Students:** One of my primary objectives is to inspire and educate young minds about the exciting possibilities in electronics semiconductor and packaging. I plan to organize workshops, seminars, and interactive sessions to introduce students to the fascinating world of packaging technology. By sharing real-world applications and success stories, I aspire to kindle their curiosity and encourage them to consider pursuing careers in this dynamic industry. I firmly believe that nurturing young talent is essential for the continued growth and innovation in our field.

2) **Establishing Career Development and Mentorship Programs:** As a young professional, I understand the significance of guidance and support in the early stages of one’s career. To empower and assist fellow young professionals entering the electronics packaging industry, I intend to establish comprehensive career development and mentorship programs. These initiatives will provide invaluable resources, insights, and networking opportunities to help them navigate the industry landscape with confidence. By fostering a culture of learning and growth, we can collectively propel the next generation of professionals to excel in their careers.

3) **Increasing Young Professional Membership in the NY Capital Region:** I plan to collaborate with existing industry leaders, academic institutions, and relevant organizations in the NY Capital Region to promote the benefits of EPS membership. By organizing engaging events and showcasing the advantages of being part of this vibrant professional community, we can attract more young talent to join our ranks. A larger and more diverse Young Professional membership will enhance the exchange of ideas, spark innovation, and foster a sense of camaraderie among emerging professionals in the region.

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**Congratulations to New IEEE EPS Senior Members**

The members listed below were elevated to the grade of Senior Member between June and November 2023. The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields for a total of 10 years and have demonstrated 5 years of significant performance. For additional information or to apply online: [https://www.ieee.org/membership/senior/](https://www.ieee.org/membership/senior/)

Dereje Agonafer—Fort Worth Section
Thanuja Balasundaram—Madras Section
Sunil Baliga—Phoenix Section
Ramesh Kumar Bhandari—Nagoya Section
Chih Chen—Taipei Section
Soon Aik Chew—Malaysia Section
Selvakumar Chidambaram—Madras Section
Abram Detofsky—Oregon Section
Balakrishnan Ethiraj—Madras Section
Robert Garcia—Puerto Rico & Caribbean Section

Jeffrey Gotro—Orange County Section
Ulrike Grossner—Switzerland Section
Leenendra Chowdary Gunnam—Vizag Bay Section
Jon Haldorson—Oregon Section
Avanija J—Ananthapuramu Subsection
Prashanth Jnanendra—Bangalore Section
Soshy Joshi—Madras Section
Christine Kallmayer—Germany Section
Youngwoo Kim—Gwangju Section
Ka San Jimmy Lam—Hong Kong Section
Yongwon Lee—Atlanta Section
K. Reddy Madhavi—Ananthapuramu Subsection
Shahriar Mirabbasi—Vancouver Section
T Venkatakrishna Moorthy—Vizag Bay Section
Subha P—Madras Section
Jordan Roberts—Alabama Section
Vidya S—Madras Section
Beatrice Tamakloe—Phoenix Section
Matthew Torgerson—Phoenix Section
Prashanth Turla—Lehigh Valley Section
Tamilarasan Uthirapathy—Madras Section
Tiwei Wei—Central Indiana Section
Kirsten Weide-Zaage—Germany Section
David Williams—Northeast Michigan Section
Congratulations to the 2024 Newly Elevated IEEE EPS Fellows

Listed below are the IEEE Fellows who are members of the EPS. See a list of all EPS members who are IEEE Fellows in the IEEE Fellows Directory. The grade of Fellow recognizes unusual distinction in the profession and shall be conferred by the Board of Directors upon a person with an extraordinary record of accomplishments in any of the IEEE fields of interest. (Bylaw I-104:11) Nominees shall:

• have accomplishments that have contributed importantly to the advancement or application of engineering, science and technology, bringing the realization of significant value to society;
• hold Senior Member or Life Senior Member grade at the time the nomination is submitted;
• have been a member in good standing in any grade for a period of five years or more preceding 1 January of the year of elevation.

The year of elevation to the grade of Fellow is the year following approval by the Board of Directors conferring the grade of Fellow.

Members elevated to the Fellow grade may use the title immediately following approval by the Board of Directors. The IEEE Fellows, an elite global group with international recognition, are called upon for guidance and leadership as the world of electrical and electronic technology continues to evolve.

Wendemagegnehu Beyene for contributions to modeling and simulation techniques for high-speed links.

Premjeet Chahal for contributions to additive manufacturing and materials characterization.

Seungbae Park for contributions to design of reliable electronic packaging.

MEMBERSHIP NEWS

Society Member Digital Library—Renew Your Membership

The Society Member Digital Library (MDL) allows members to view and download a wide selection of journals and conference proceedings at no additional charge. EPS Members have access to the full archive of EPS sponsored Transactions, journals and conference proceedings via Xplore. This includes current and prior editions of more than 15 Transactions and journals and 35 conferences, including the ECTC, EPTC, ESTC and more.

Sign into Xplore to access the Digital Library. The MDL is available to members who join EPS or renew membership for 2024.

EPS Student Chapter Promotion Programs

To promote the formation and continuation of EPS student chapters, EPS has recently initiated a couple of promotion programs. The Student Chapter Promotion Program (SCPP) is aimed at the formation of new student chapters while the Student Chapter Continuation Program (SCCP) is aimed at helping existing student chapters to remain viable.

Student Chapter Promotion Program (SCPP)

Under the SCPP, six students from any university which has an IEEE student branch who are willing to serve as executive committee (excom) members in a new student branch chapter (SBC) will be given complimentary IEEE+EPS student memberships.

Additionally, faculty members who are willing to serve as Advisors to new SBCs will also be given complimentary IEEE+EPS eMemberships where available, otherwise regular memberships will be provided. The Advisor’s duties include advising the excom on student chapter activities, endorsing financial statements where necessary, ensuring that annual election/appointment of new student excom members are held before end December, and that required reports are submitted by the student excom in a timely manner every year.

Student Chapter Continuation Program (SCCP)

Another program, the Student Chapter Continuation Program (SCCP) has also been initiated to facilitate the continuation of existing EPS student chapters. Similar complimentary IEEE+EPS memberships will be given to six students in a university with an existing EPS SBC who are willing to serve as executive committee (excom) members in the student chapter, and to a faculty who agrees to serve as the Advisor to the student chapter.

To qualify for subsidy under the SCCP, the excom and Advisor must ensure that their SBC remains viable for the year. This
includes the organization of at least two technical activities per calendar year, formation of new excom for the following year, and timely submission of required activity and financial reports for the year.

An evaluation on the performance of subsidized student excom members and Advisors will be conducted in December each year based on reports submitted. Non-performing students and Advisors will not be subsidized for another year. While Advisors may be subsidized every year, student excom members may normally be subsidized for up to 2 years, in order to encourage a healthy succession of student leaders in the chapter. However, if the Advisor can report some extenuating circumstances, the subsidy for an excom student can be extended for up to 4 years, subject to the approval of the Student Program Director.

**Annual Subsidy for Student Chapters**

To support the organisation of technical activities by SBCs, existing SBCs may apply for subsidies of up to US$1000 per annum from EPS. For new SBCs in their first year, the subsidy can be up to US$1500.

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**PUBLICATIONS NEWS**

**Become a Reviewer for the IEEE Transactions on Components, Packaging and Manufacturing Technology (T-CPMT)**

T-CPMT provides the latest information in electronics packaging. Contribute to the research in the electronics packaging field by becoming an IEEE peer reviewer. Peer reviewers fulfill a vital role in the publishing process by giving detailed and professional commentary.

Rigorous peer-review of all papers that appear in the Transactions on Components, Packaging and Manufacturing Technology (T-CPMT) is required by the IEEE. Papers are selected for publication only on the basis of merit and appropriateness. As a reviewer, you play a key role in ensuring the quality, consistency, and impact of T-CPMT in the community. For T-CPMT, we normally require all reviewers to complete the review in two weeks from the date when you agreed with the Associate Editor.

We are inviting you to become a reviewer and to maintain the high standard for the journal. If you are interested in becoming a reviewer, please submit your interest online using the QR code below. It is especially important to indicate your areas of expertise with several keywords. These keywords will be accessed by Associate Editors searching for reviewers in the database, based on the keywords of the submissions received.

Although all reviewers remain anonymous during the review process, all reviewers are named and acknowledged annually in the December issue.

EPS Executive Office: Denise Manning d.manning@ieee.org
EPS VP Publications: Ravi Mahajan ravi.v.mahajan@intel.com

**Reviewer Form**

![QR code](QR code)
Electronics Packaging Society Section within IEEE Access

The Electronics Packaging Section within IEEE Access will draw on the expert technical community to continue IEEE’s commitment to publishing the most highly-cited content. The Journal peer-review process targets a publication period of 6 weeks for most accepted papers. This journal is fully open and compliant with funder mandates, including Plan S.

This is an exciting opportunity for your research to benefit from the high visibility of IEEE Access. Your work will also be exposed to 5 million unique monthly users of the IEEE Xplore® Digital Library.

Scope
The IEEE Electronics Packaging Society section in IEEE Access covers the scientific, engineering, and production aspects of materials, components, modules, hybrids and micro-electronic systems for all electronic applications, which includes technology, selection, modeling/simulation, characterization, assembly, interconnection, packaging, handling, thermal management, reliability, testing/control of the above as applied in design and manufacturing. Examples include optoelectronics and bioelectronic systems packaging, and adaptation for operation in severe/harsh environments. Emphasis is on research, analysis, development, application and manufacturing technology that advance state-of-the-art within this scope.

Get Published in the New Electronics Packaging Society Section of IEEE Access
Go to: https://mc.manuscriptcentral.com/ieee-access
Select the Electronics Packaging Society (EPS) Section from the pull-down menu of “Manuscript type” in the first page of the submission process.

Author Information and Instructions
EPS is committed to supporting authors and researchers with IEEE Author Tools including the IEEE Publication Recommender, IEEE Graphics Analyzer, LaTeX Analyzer and more. Discover the tools available at the IEEE Author Center—https://ieeauthorcenier.ieee.org/ieee-author-tools/.

The EPS is regarded as a trusted and unbiased source of technical information for dialog and collaboration to advance technology within the computing community. EPS is led by researchers and technology professionals who are at the center of respected electronics packaging communities where readers and authors already come together.

The articles in this journal are peer reviewed in accordance with the requirements set forth in the IEEE Publication Services and Products Board Operations. Each published article is reviewed by a minimum of two independent reviewers using a single-blind peer review process, where the identities of the reviewers are not known to the authors, but the reviewers know the identities of the authors. Articles will be screened for plagiarism before acceptance.

Article Processing Charge (APC): US$1,995
IEEE Members receive a 5% discount.
IEEE Society Members receive a 15% discount.
These discounts cannot be combined.

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Wendem Beyene, Meta, USA
Muhammad Bakir, Georgia Institute of Technology, USA
Koneru Ramakrishna, Cirrus Logic, Inc., USA
Hsien-Chie Cheng, Feng Chia University, Taiwan
Yogendra Joshi, Georgia Institute of Technology, USA

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Recent Advances and Trends in Advanced Packaging
John H. Lau
Publication Year: 2022, Page(s):228–252

Universal Chiplet Interconnect Express (UCIe): An Open Industry Standard for Innovations With Chiplets at Package Level
Debendra Das Sharma; Gerald Pasdast; Zhiguo Qian; Kemal Aygun
Publication Year: 2022, Page(s):1423–1431

Recent Advances and Trends in Cu–Cu Hybrid Bonding
John H. Lau
Publication Year: 2023, Page(s):399–425

Thermomechanical Challenges of 2.5-D Packaging: A Review of Warpage and Interconnect Reliability
Hakjun Kim; JaeYoung Hwang; Sarah Eunkyung Kim; Young-Chang Joo; Hyejin Jang
Publication Year: 2023, Page(s):1624–1641

CPU Overclocking: A Performance Assessment of Air, Cold Plates, and Two-Phase Immersion Cooling
Bharath Ramakrishnan; Husam Alissa; Ioannis Manousakis; Robert Lankston; Ricardo Bianchini; Washington Kim; Rich Baca; Pulkit A. Misra; Inigo Goiri; Majid Jalili; Ashish Raniwala; Brijesh Warrier; Mark Monroe; Christian Belady; Mark Shaw; Marcus Fontoura
Publication Year: 2021, Page(s):1703–1715
EDUCATION/CAREER NEWS

EPS Distinguished Lecturer Program

EPS Distinguished Lecturers are selected from among EPS Fellows, Award winners, and Society leaders, who are members of the technical community and experts in their field. They are available to present lectures and/or courses at EPS events–Chapters, Conferences, Workshops or Symposia, as well as IEEE Student Chapter events.

The EPS Distinguished Lecturer Program (DLP) aims at serving communities interested in the scientific, engineering, and production aspects of materials, component parts, modules, hybrids and micro-electronic systems for all electronic applications.

The Program strives to support EPS Chapters worldwide by helping them to invite leading researchers in their respective fields and IEEE Student Chapters to encourage students to pursue EPS related fields and to join the EPS society. The DLP talk is a major event in the life of the inviting Chapter.

EPS Distinguished Lecturers

**Ramachandra Achar (7/1/2020–6/30/2024)**
Department of Electronics, Carleton University
Ottawa, Ontario, CANADA
Topics: CAD tools and methodologies for interconnects, packages, and systems with an emphasis on signal, power and EMI integrity

**Mudasir Ahmad (1/2022–12/2025)**
Google
CA, USA
Topics: Internet of Things (IoT), Advanced Packaging, 2.5D, Heterogeneous Silicon Photonics, Advanced Reliability (Thermomechanical, Mechanical Shock), Numerical Modeling, Advanced Thermal Solutions, Stochastic Analysis, Bayesian Inference, Machine Learning, Artificial Intelligence

**Kemal Aygün, Ph.D. (7/1/2020–6/30/2024)**
Intel Corporation
Chandler, AZ USA
Topics: Package/socket/board/interconnect technologies, electrical simulation methodology and lab metrologies

**Muhammad Bakir, Ph.D. (1/2022–12/2025)**
School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, GA USA
Topics: Emerging interconnection architectures and technologies; heterogeneous system design and integration

**W. Dale Becker, Ph.D. (7/1/2020–6/30/2024)**
Retired
Hyde Park, NY USA
Topics: Electronic Package design and integration, system design, electrical modeling tools

**Wendem Beyene, Ph.D. (7/1/2020–6/30/2024)**
Meta
San Jose, CA
Topics: Electrical modeling and simulation techniques for analysis of interconnects, packages, and systems. Machine learning techniques

**Karlheinz Bock, Ph.D. (7/2020–7/2024)**
Technische Universität Dresden
Dresden, Germany
Topics: Multifunctionality & heterosystemintegration & additive manufacturing (IoT, Industry 4.0, tactile internet), packaging for mechanical, digital and power co-integration (automotive, machines, robots...), 2.5D and 3D electro-optical-RF interposer and board (high performance), heterointegration for flexible, bio, organic and large area electronics (open form factor)

Third Millennium Test Solutions
Santa Clara, CA USA
Topics: Heterogeneous Integration, Semiconductor test technology, Emerging research materials, Packaging of electronic components and systems, the global network and its future requirements, the internet of things and Smart manufacturing

**Chris Bower, Ph.D. (6/2021–6/2025)**
X-Celeprint Inc.
North Carolina, USA
Topics: novel assembly methods, elastomer stamp micro-transfer-printing, heterogeneous integration, three-dimensional integration, manufacturing of micro-assembled displays and other large-format electronics.

**Tanja Braun, Ph.D. (7/2023–6/2027)**
Fraunhofer IZM
Berlin, Germany
Topics: Advanced Packaging, Heterogeneous Integration, Chiplet, Fan-out Wafer and Panel Level Packaging.

**William T. Chen, Ph.D. (1/2024–12/2027)**
ASE (U.S.) INC
Santa Clara, CA USA
Topics: Semiconductor and Electronics Industry Trends and Roadmap

**Kuan Yew Cheong, Ph.D. (1/2024–12/2027)**
Universiti Sains Malaysia
Pulau Pinang, Malaysia
Topics: Materials and Physical Failure Analysis

**Xuejun Fan, Ph.D. (1/2024–12/2027)**
Lamar University
Beaumont, TX USA
Topics: Design, modeling and reliability in micro-/nano- electronic packaging and microsystems
Madhu Iyengar, Ph.D. (7/1/2020–6/30/2024)
Google
Mountain View, CA, USA
**Topics:** Thermal component and system design for packages, servers, and data centers.

University of California, Los Angeles
Los Angeles, CA USA
**Topics:** Heterogeneous Integration; Flexible hybrid electronics; 3D interposer, and wafer scale integration and stacking.

Beth Keser, Ph.D. (1/2024–12/2027)
Intel
San Diego, CA USA
**Topics:** Fan-Out Wafer Level Packaging and Wafer Level Packaging structures; processes, materials, tools, design rules and roadmaps; photoimageable liquid polymer films

Pradeep Lall, Ph.D. (1/2024–12/2027)
Auburn University
Auburn, AL USA
**Topics:** Semiconductor Packaging, Modeling and Simulation, Reliability in Harsh Environments, Shock/Drop/Vibration, Cu Wirebonding, Flexible Hybrid Electronics, Additive Manufacturing, Prognostics and Health Management, LEDs, Micro CT Measurements

John H. Lau, Ph.D. (1/2024–12/2027)
Unimicron Technology Corporation
Palo Alto, CA USA
**Topics:** Electronics and Photonics 2D and 3D packaging and manufacturing

Ravi Mahajan, Ph.D. (7/2020–7/2024)
Intel Corporation
Arizona, USA
**Topics:** Advanced Packaging Architectures, Assembly Processes and Thermal Management

James E. Morris, Ph.D. (1/2024–12/2027)
Department of Electrical and Computer Engineering
Portland State University
Portland, Oregon USA
**Topics:** Electrically conductive adhesives; Electronics packaging; Nanotechnologies

Rajen Muguran, Ph.D. (7/2022–7/2026)
Texas Instruments
Dallas, TX, USA
**Topics:** Multiphysics and System Co-Design modeling for complex analog and mixed-signal packaging, mmWave/THz signal integrity, power electronics packaging, and System-Level EMI/EMC modeling, analysis, and characterization.

Eric D. Perfecto, (1/2024–12/2027)
IBM Research
Poughkeepsie, NY USA
**Topics:** Fine pitch interconnect, chip to chip and chip to laminate connection, UBM and solder selection, chip package interaction and 2.5D fabrication

Mark Poliks, Ph.D. (1/2024–12/2027)
Binghamton University (SUNY)
Binghamton, NY USA
**Topics:** Materials and Processes, Advanced Manufacturing, Flexible Hybrid Electronics, High Speed and Additive

Gamal Refai-Ahmed, Ph.D. (7/1/2022–6/30/2026)
Xilinx
San Jose, CA USA
**Topics:** Thermo-mechanical Semiconductor and Electronics Industry Roadmap and directions, Advanced holistic Thermo-mechanical solution, assembly and reliability of Heterogeneous Packaging and Silicon Photonics, Future thermo-mechanical technology, architecture for component and system

Jose Schutt-Aine, Ph.D. (1/2024–12/2027)
University of Illinois
Champaign, IL, USA
**Topics:** High-Frequency Measurements, Mixed-Signal Design, High-Performance Computing, electromagnetic Modeling, Signal Integrity, CAD Tools for Interconnects and Packages, Machine Learning for High-Speed System Modeling

John Shalf, (1/2024–12/2026)
Lawrence Berkeley National Laboratory
Berkeley, CA USA
**Topics:** HPC System Integration, System Integration, Photonics and Packaging

Dongkai Shangguan, Ph.D. (7/1/2023–6/30/2027)
Thermal Engineering Associates, Inc.
San Jose, CA USA
**Topics:** Heterogeneous Integration and SiP; Electronics Packaging and Miniaturization; Materials; Thermal management; Reliability; Electronics manufacturing technology; Flexible hybrid electronics

Rohit Sharma, Ph.D. (1/2023–1/2027)
Indian Institute of Technology Ropar
Punjab, India
**Topics:** Design of High-speed Graphene-based and 2D materials-based nanoelectronics; Electrical-Thermal co-design of electronic packages and microsystems; Application of Machine Learning in design and analysis of interconnects; Heterogeneous integration.

Ephraim Suhir, Ph.D. (1/2024–12/2027)
Los Altos, CA 94024 USA
**Topics:** Accelerated life testing; Probabilistic physical design for reliability; Bonded assemblies; Thermal stress; Predictive modeling; Fiber optics structures: design for reliability; Dynamic response to shocks and vibrations

(continued on page 22)
EPS Certificate Program

The IEEE Electronics Packaging Society Certificate Program provides a pathway for early and mid to late-career professionals to highlight their accomplishments.

Criteria for all Certificates: Must be an IEEE Electronics Packaging Society Member.

There are three Certificates you may apply for, which are noted below.

EPS Achievement Certificate

The first level EPS Achievement Certificate is aimed at early-career professionals working in the field of electronics packaging. It is especially intended to encourage the career development of young professionals including advanced graduate students.

Criteria: Current EPS Member

To receive your certificate, 15 professional development hours (PDHs) must be completed. This can be obtained from a combination of the following:

1) IEEE EPS Webinar (1 PDH)—must complete PDH evaluation.
2) Professional Development Courses—must complete survey and CEU credit form. Previous ECTC PDCs from the last 10 years can be used towards this if the CEU application was completed at the time of the course. PDCs from ESTC and EPTC 2018 and forward can be used.
   - Electronic Components and Technology Conference (USA) = 4 PDHs
   - Electronic Systems-Integration Technology Conference (Europe) = 3 PDHs
   - Electronic Packaging Technology Conference (Asia) = 4 PDHs
3) Author of IEEE T-CPMT and/or EPS conference paper(s) (5 PDHs)—paper must be published in IEEE Xplore within the last 5 years.
4) Reviewer for IEEE T-CPMT (3 Reviews = 5 PDH) within the last 5 years.

Once you have completed any combination of the above and received 15 PDHs, please complete the certificate form to request your Electronics Packaging Society Certificate of Achievement.

EPS Distinguished Achievement Certificate for Technical Leadership and Expertise

Criteria: Must be a current EPS member

There are five high-level focus areas for this new certificate. These areas include:

1) Being a recognized authority of technical expertise in electronics packaging.

Examples include being an advanced member of the technical staff at a company (e.g. Fellow, Senior Technical Staff, Distinguished Engineer, etc.), making technical contributions
as a Member or Fellow of professional associations/societies related to electronics packaging (e.g., IEEE, IMAPs, SMTA, ASME, etc.), and being an invited speaker at companies, technical conferences, and EPS Chapter meetings.

2) Being a subject matter expert (SME) in electronics packaging at conferences, keynotes, webinars, blogs, etc.

   Methods to demonstrate participation as a SME include abstracts accepted and papers presented at conferences, giving keynote lectures at conferences or professional society meetings, presenting webinars for EPS and other IEEE Societies, and serving on technical panels at conferences and other venues.

3) Demonstrating sustained technical contributions to the electronics packaging industry.

   Examples of sustained technical contributions include publishing well-cited technical papers at conferences and in journals, book chapters, and patents; serving as an editor of a journal or reference book; and being a leader or participant in industry blogs, focus groups, technical roadmaps, newsletters, and forums.

4) Documenting advanced technical recognitions in electronics packaging.

   Methods to document technical recognitions include receiving technical awards from a company, institute, professional society, or academic institution; being the acknowledged inventor of a seminal technology or process important to industry; serving as the point person for global high-level task force activity; and being elected to be a Member of an organization such as the US National Academy of Engineering, Royal Academy of Engineering, Chinese Academy of Engineering, IBM Academy of Technology, etc.

5) Provide at least one endorsement letter.

   Nominations for the Distinguished Achievement Certificates will be accepted two times per year: Jan 1–June 30 and Aug 30–Oct 31.

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**EPS Distinguished Achievement Certificate for Professional Engagement and Service**

Criteria: Must be a current EPS member

There are four high-level areas of focus for this new certificate. These areas include:

1) Demonstrating leadership in the electronics packaging field.

   Leadership and broad impact activities in electronics packaging can be documented from outstanding accomplishments during industry employment or for notable volunteer contributions to the profession and society.

2) Illustrating broad impact/influence in the electronics packaging field.

   Examples of significant professional service include serving as an officer in a technical society at the international, national, or local chapter level; participating in packaging related technical committees, councils, or affinity groups; contributing to technology roadmaps such as the Heterogeneous Integration Roadmap (HIR); and receiving a professional society or industry award based on service contributions.

3) Providing extensive service and “give back” to the profession and/or industry; and

   Documentation of “give-back” to one’s technical community can be accomplished via demonstrations of coaching and mentoring of co-workers, young professionals, and students.

4) Provide at least one endorsement letter.

   Nominations for the Distinguished Achievement Certificates will be accepted two times per year: Jan 1–June 30 and Aug 30–Oct 31.

More details on the Certificate Program are available on the EPS website at https://eps.ieee.org/education/eps-certificate-program.html. The EPS Certificate Program is sponsored by the IEEE EPS VP Education and is offered only to EPS members. For questions, please contact Eric Perfecto (eperfecto@gmail.com).
Education/Career News  (Continued from page 19)

Andrew Tay, Ph.D. (1/2023–12/2026)
SHINE Center, National University of Singapore
Singapore
Topics: Thermomechanical reliability of microelectronics packages; Thermal and failure analysis of microelectronic devices; Thermal management of electronic and EV battery systems; Solder joint reliability; Delamination and fracture; Moisture effects; Modelling and simulation.

Manos Tentzeris, Ph.D. (7/2023–6/2027)
Georgia Institute of Technology
Atlanta, GA USA
Topics: RF/mmW/3D/electronics industry/nanotechnology/materials/packaging/3D printing/energy harvesting-zero power

Rao Tummala, Ph.D. (1/2024–12/2027)
Microsystems Packaging Research Center (PRC)
Georgia Institute of Technology
Atlanta, GA USA
Topics: Electronics Packaging

E. Jan Vardaman (1/2024–12/2027)
TechSearch International, Inc.
Austin, TX USA
Topics: International developments in semiconductor packaging, manufacturing and assembly; SiP; Business and technology Trends; drivers in advanced packaging; Flip chip and wafer level packaging

Paul Wesling (1/2024–12/2027)
Saratoga, CA USA
Topics: Origins of Silicon Valley and the Electronics Packaging Society; the IEEE/SEMI/ASME Heterogeneous Integration Roadmap and how to use it (as editor for the 2019 Roadmap).

EPS Achievement Certificate

Congratulations to these EPS Members on receiving the IEEE Certificate of Distinguished Achievement from the IEEE Electronics Packaging Society and completing the required number of professional development hours.

Lance Liu, Micron Memory Technology
Henry Antony Martin, Chip Integration Technology Center (CITC) and Delft University of Technology (TUD)
Patrick Thompson, Texas Instruments
Sasi Kumar Tippabhotla, Institute of Microelectronics, A*Star Research Entities

Congratulations to the EPS Members on receiving the IEEE Certificate of Distinguished Achievement from the IEEE Electronics Packaging Society for having made exemplary contributions to the areas of Technical Leadership and Expertise in the field of Electronics Packaging.

Mukta Farooq, IBM
John Lau, Unimicron Technology Corporation
Rajen Murugan, Texas Instruments
E. Jan Vardaman, TechSearch International, Inc.

EPS Resource Center

The IEEE EPS Resource Centers contains valuable, technical content from reputable experts to enhance research or industry work, implement trainings, or earn CEU/PDH credits—all of which are universally available on demand.

IEEE EPS Resource Centers benefits include:
• Access to valuable technical community content
• Access to content 24 hours a day, 7 days a week through an easy-to-use global portal

Available at no cost for EPS members
Opportunities to earn CEUs and PDHs
Top webinars:
• 6G Opportunities and Packaging Challenges
• Chiplet Design and Heterogeneous Integration Packing
• Roadmap Based on Holistic Understanding of Thermo-Mechanical Challenges
• Advanced Packaging for Wide Bandgap Semiconductor Power Modules
• Recent Advances and Trends in Advanced Packaging

https://resourcecenter.eps.ieee.org/

JANUARY 2024 / IEEE ELECTRONICS PACKAGING SOCIETY NEWSLETTER
**Upcoming EPS Photonics TC Webinar**

**Title of presentation:** Advanced Packaging for Integrated Photonics: From Research to Manufacturing.

**Date:** March 7, 2024

**Time:** 1:00 PM EST

**Speaker:** Dr. Pradric Morrissey, Tyndall National Institute

**Moderator:** Farnood Rezaie, CISCO

**Register Here**

**Abstract:** In the realm of cutting-edge research, advanced packaging serves as a pivotal enabler, facilitating the integration of diverse technology platforms such as photonics, electronics, micro-electromechanical systems, and fluidics. This interdisciplinary approach unlocks a multitude of exciting applications spanning telecommunications, quantum technologies, medical devices, and sensing. In this context, packaging processes play a transformative role, empowering researchers to take device concepts from the laboratory to fully functional systems. This transition not only expands technological possibilities but also fosters collaborative ventures with industrial partners. This talk offers an overview of photonics packaging technologies and provides insights into ongoing initiatives aimed at translating advanced photonics technologies from research to manufacturing.

**Biography:** Dr. Padraic Morrissey has over 8 years of experience as the Senior Programme Manager for the Photonics Packaging and Systems Integration Group at the Tyndall National Institute. His expertise lies in managing both industry and academic research projects, with a strong and broad understanding of photonics, focusing on design, characterization, advanced packaging, and testing. Dr. Morrissey serves as the Technology Manager for the EU-funded PIXAPP Pilot Line, coordinating all technical activities while supporting its growth and sustainability. In his current position as Programme Manager, Dr. Morrissey continues to contribute to the growth of PIXAPP while being responsible for the National Photonics Manufacturing Pilot Line. He oversees all industrial activities, collaborates with academic research partners, and leads initiatives to enhance technical capabilities.

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**President’s Column (Continued from page 1)**

- Region 8. Karlheinz Bock, Przemyslaw Gromala, Grace O’Malley
- Region 10. Eiji Higurashi, Shaw Fong Wong, Chuan-Seng Tan, Chih-Pin (C.P.) Hung, Kishio Yokouchi
- Young Professional. Aakrati Jain
  - My thanks to the leaders who completed their terms in 2023:
  - Vice President, Conferences: Sam Karikalan. Sam led us with great success through the challenges of holding conferences during COVID.
  - MaL: Yoichi Taira and Yan Liu. Yan will be continuing as our Women in Engineering representative.

I encourage each of you to: 1. Take advantage of the many resources available to you from EPS and 2. Become involved in EPS leadership at the local and/or Society level. Based on my experience, you will receive a rich return on your investment of time and effort.

Pat Thomsson
IEEE EPS President 2024–2025
The 25th Electronics Packaging Technology Conference (EPTC2023) Report

The 25th Electronics Packaging Technology Conference (EPTC2023) was held from 5th to 8th December, 2023 at the Grand Copthorne Waterfront Hotel, Singapore. 2023 marked the 25th anniversary of EPTC and the usual 3-day event was extended to a 4-day event to celebrate the occasion. It opened with a spectacular laser show during which the EPTC 25th Anniversary logo was unveiled with spinning LED lights. The show highlighted the significance of electronics packaging in our everyday lives from devices such as lasers and LEDs.

Following the show, the attendees were warmly welcomed by the General Chair, Prof. Andrew Tay, who incidentally was also the General Chair of the inaugural EPTC held in Singapore on 8–10 October, 1997.

EPS President, Dr. Kitty Pearsall, then gave her opening address updating the audience on the current activities of the Electronics Packaging Society.

A captivated audience
The inaugural EPTC conference in 1997 had only 55 abstracts and 110 participants but this has grown to 195 abstracts and 440 participants in 2018, and 290 abstracts and 566 participants in 2023. In 2023, the abstracts were received from 23 countries making it a truly international conference. What is also of great significance is the percentage of abstracts submitted from various countries as illustrated in the figure below which shows that there is very wide contribution from Asian countries as well as good contributions from Europe and USA.

Fast forward to 2023, the first day featured 4 keynotes by prominent technology leaders as listed below:

1) Topic: Advanced System Integration Technology Trend
   Speaker: Dr. Douglas Yu, Vice President of TSMC R&D and TSMC Distinguished Fellow

2) Topic: Advanced Packages Enriching Heterogeneous Integration
   Speaker: Dr. Chih Pin Hung, Vice President, Corporate R&D, ASE Group.

3) Topic: Will Advanced Packaging Save Moore’s Law?
   Speaker: Dr. Yang Pan Corporate Vice President, Lam Research.

4) Topic: 2.5D/3D Heterogeneous Integration for Silicon Photonics Engines
   Speaker: Dr. Radha Nagarajan, Senior Vice President and Chief Technology Officer of Marvell’s Optical and Copper Connectivity Group
It also featured two panel sessions on current hot-button topics:

1) **Topic: Chiplet Integration**
   Moderator: Dr. Jiantao Zheng, Huawei
   Panellists:
   - Dr. Ravi Mahajan, Intel Fellow and Director of Pathfinding for Assembly and Packaging Technologies, Intel;
   - Dr. Arvind Sundarrajan, MD/Head of Applied Packaging Development Center, Applied Materials;
   - Dr. Surya Bhattacharya, Director of SiP, IME, A-Star;
   - Dr. C.P. Hung, Vice President, Corporate R&D, ASE Group.

2) **Topic: Artificial Intelligence for Package Design and Manufacturing**
   Moderator: Dr. Sam Karikalan, Broadcom, Inc. and EPS VP of Conferences.
   Panellists:
   - Mr. Samuel Goh, Senior Director, Kulicke & Soffa;
   - Ms. Grace O’Malley, VP Technical and Project Operations, iNEMI;
   - Mr. Vincent DiCaprio, VP, Applied Materials;
   - Prof. Kuo Ning Chiang, Professor, National Tsing Hua University

The keynotes and panel sessions were all very well received with many questions and lively discussions after the presentations.

The second day opened with 5 Professional Development Courses (PDCs) in the morning:

1) Fan-Out, Chiplet, and Heterogeneous Integration Packaging by Dr. John H Lau
2) Flip Chip Interconnect by Mr. Eric Perfecto
3) Co-Packaged Si Photonics: Opportunities and Challenges by Prof. Amr S. Helmy
4) Design-on-Simulation Technology for Advanced Packaging Reliability Life Prediction by Prof K. N. Chiang
5) Automotive Electronics Reliability—Challenges and Opportunities by Prof. Pradeep Lall

This was followed by the EPS Luncheon where certificates of appreciation were given out to the members of the Organizing Committee. As well, EPS Student Travel Grants were given out to the following 5 students:

1) Xiaodong Wu; Xiamen University, China
2) Yuqi Zhou; Huazhong University of Science and Technology, China
3) Jiao Li; Northwestern Polytechnical University, China
4) Gaurav Khurana; Technische Universitaet Dresden, Germany
5) Ping Wu; Central South University, China

The EPS Student Travel Grants were given out to promote student participation in EPS flagship conferences, especially those students who have financial difficulties attending conferences.
Following the EPS Luncheon, Dr. Mo Shakouri, CEO of Micronanj, gave a Technology Talk on “Challenges in the Analysis and Testing of Advanced Packaging Systems”.

For the rest of the conference period, there were 12 Invited Talks, 168 Oral Presentations, and 44 Interactive Presentations. The 12 Invited Talks were:

- Modeling and Characterization of Single Grain Solder Micro Bumps in Advanced Packaging—Jeffrey C. Suhling, Auburn University, USA
- New Innovation of Heterogeneous Integration in AI and ML Era—Jin Yang, Samsung, South Korea
- Forward-Looking Roadmap View to Enable Heterogeneous Integration in the next 10 years—Gamal Refai-Ahmed, AMD, USA
- Development of Novel Polymer Materials for Advanced Packaging—Takenori Fujiwara, Toray, Japan
- Fluxless Bonding for Higher Density & Bandwidth Packaging—Steve Ng, KnS.
- Wafer to Wafer and Die to Wafer Hybrid Bonding for Advanced Interconnects—V. Dragoi, EVG, Austria.
- Die-to-Wafer Hybrid bonding to address next-gen Electronics Packaging Challenges—Gaurav Mehta, Applied Materials, Singapore.
- Signal and Power Integrity of CoWoS-R in Chiplet Integration Applications—Chuei-Tang Wang, TSMC, Taiwan.
- The Era of Generative AI and Advanced Packaging—Chak Wing Kei, Tommy, ASMPT, Hong Kong
- AI and Failure Mechanics based Life prediction for electronic systems—Pradeep Lall, Auburn University, USA
- Fan-out wafer level packaging solutions for mmWave applications—Tanja Braun, Fraunhofer IZM, Germany
- 3D Integrated Package for High Performance Computing Applications—Yu-Po Wang, SPIL, Taiwan
- Die-to-Wafer (D2W) Hybrid Bonding for Advanced Heterogeneous Integration—Jonathan Abdilla, Besi
- A highly relevant HIR Workshop was also convened where updates by experts from the HIR working groups on 2D-3D & interconnect, Mobile, Modelling & Simulation, Co-Design, Supply Chain, Integrated Power Electronics, SIP & Module, and Test were presented.

The conference was well-supported by 21 Sponsors, 22 Exhibitors, and 6 Conference Partners:

Great multi-ethnic food was provided for the international participants.
There was a meeting of Chairs of EPS Chapters in Region 10 where chapter activities were shared. A Young Professionals networking event was also held in which many EPS Board of Governors participated.

The exhibition booths were well visited by participants. Plenty of interaction at interactive presentations.

The highly anticipated final session of the conference was the lucky draw where many prizes including an iPhone and two iPads, were given out.

First time lucky, student Viktor Dudash from TU Dresden, Germany, won the top lucky draw prize, an iPhone.

Overall, the 25th Anniversary of EPTC was a huge success with many new conference records set. The post-conference survey has revealed that a large majority of the attendees were very satisfied with the technical program, organization, venue, networking sessions, exhibition, and food. The Organizing Committee would like to express its deepest appreciation to keynote speakers, panel speakers, HIR Workshop convenors, authors, sponsors, exhibitors, partners and participants for their contributions and support. They look forward to your participation at EPTC2024 which will be held on 3–6 December, 2024 in Singapore. Keep updated by visiting the EPTC website https://www.eptc-ieee.net/.

Written by Andrew Tay,
General Chair EPTC2023.
ICSJ2023 Report

The 12th IEEE CPMT Symposium Japan 2023 (ICSJ2023) was held on 15–17 November 2023 at Ritsumeikan University Suzaku Campus, Kyoto, Japan. ICSJ is recognized as the international symposium for leading-edge packaging technologies. The symposium started as “The VLSI Packaging Workshop in Japan” in 1992 and was held every two years. To cover the wide area of electronics packaging, the committee refurbished the workshop, and started the new symposium-IEEE CPMT Symposium Japan in 2010.

ICSJ2023 was sponsored by IEEE EPS and was incorporated with IEEE EPS Japan Chapter and IEEE Photonics Society UK & Ireland chapter. The General Chair, Taiji Sakai, from FICT LIMITED, set this year’s theme, “Advanced Packaging for Chiplet Era”. In the three-day program, we had 4 plenary speakers, 2 EPS special speakers, 2 specials speakers, 4 IEEE EPS Technical Committee 6 session speakers, 10 invited speakers and 47 technical presentations. Technical sessions were as follows; Advanced Package I, II, III, Co-packaged Optics, Photonics Package, VICSEL-Based Optical interconnections, Integrated Photonics, Polymer Waveguide Technology, Process and Materials I, II, III, Bioelectronics, Automotives I, II, Millimeter Wave application, High-Speed Electrical Interconnect and Power Electronics. After the technical presentations, the presenters held additional 15-minute discussions called “Interview with the Authors”. In the same manner as the poster session, presentation slides were put on the board, and more detail discussion could be done individually. We also had a unique poster session called “Early Career Researcher’s session (ECR session). The ECR sessions presenters are young researchers within 2 years’ experience in their professions and all students have the opportunity to present their work.

General Chair; Taiji Sakai

Opening Remarks

The Venue

Early Career Researcher’s session
including Ph.D. It was held on the 2nd evening, and the attendees discussed with the presenters directly while having finger snacks and drinks. There were 276 attendees who came to discuss technical interests for improving their development. I hope ICSJ brought many researchers together, supported them in creating friendships and helped create new development for the world.

During the symposium, EPS Japan BoG meet with EPS US headquarters BoG officers. Kitty Pearsall (Kitty-san), EPS president and Jeffrey C. Suhling (Jeff-san), EPS Vice President, Finance kindly joined the meeting. We introduced ourselves, discussed the future of Electronics Packaging and exchanged opinions.

ICSJ2023 Conference Relations Chair
Shiny Takyu

IEEE EPS: 8th of Dec, 2023, Young Professional (YP) Meeting with EPS BOG and Leaders at EPTC Conference, Singapore
(Compiled by Yan Liu & Shaw Fong Wong)

The IEEE EPS Young Professional (YP) Meetup session proved to be a dynamic forum where emerging leaders and professionals in the field of electrical and electronics engineering converged to share insights, collaborate, and foster connections. This event, in conjunction with EPTC conference in Singapore provided a platform for young professionals to engage in meaningful discussions related to their possible career development with the EPS BoG and respective leaders. Attendees had the opportunity to participate in interactive sessions and networking activities, enabling them to exchange ideas and build a supportive community. The meetup not only showcased the vibrant talent within the IEEE EPS community but also emphasized the importance of continuous learning and collaboration in shaping the future of the EPS landscape. Overall, the event served as an inspiring and enriching experience for young professionals looking to navigate and excel in their careers within the IEEE EPS network. Special thanks to all the EPS BoG and the leaders who joined the session. Also not forgetting Yan Liu on preparing the beautiful flash cards for the YPs to collect, which was indeed one of the highlights of the event too!

Opening by Shaw Fong Wong to remind the YPs to collect the special printed flash cards during the meet up event.

Group photo of all the YPs, EPS BoG and also the industry/ academia leaders.
EDAPS 2023 Report

Sugar Beach Resort, Republic of Mauritius, December 12-14th, 2023

From December 12-14th, 2023, the exotic island of Mauritius, located in the Indian Ocean, hosted its first-ever IEEE EPS EDAPS (Electrical Design of Advanced Packaging and Systems) conference. EDAPS, an international flagship electronics packaging society’s (EPS) event, has consistently served as a platform for disseminating the latest research in the multiphysics design of semiconductor chips, packages, and systems. The 2023 EDAPS 3-day conference theme was “Semiconductor Packaging: The Next Frontier”. The conference was well received as it offered an excellent opportunity to highlight the latest advances in the field from leading worldwide experts, showcased the current state-of-the-art research from local investigators, and provided a chance for the local engineering undergraduate and graduate students to interact and network with professionals and expose them to the myriad of career opportunities in this area. The conference comprised 38 accepted technical paper presentations (out of 59 submitted), 10 student poster sessions focusing on local university research, and 4 keynote speeches.

EDAPS is traditionally held in Asia and rotated amongst several countries, including India, Japan, South Korea, China, Taiwan, and Singapore. The 2023 EDAPS theme, “The Next Frontier,” was aptly chosen as it was the first time EDAPS was hosted outside Asia, other than Hawaii (held once there). Mauritius is in the IEEE Region 8 (Europe, Middle East, and Africa) and offers ample opportunities for EPS to promote packaging in Africa.

EDAPS 2023 was very successful. We would like to take this opportunity to thank the EPS and MGA supporting teams, the organizing committee members, the paper review committee members, our presenters (papers and posters), our keynote speakers, our generous sponsors, and the fantastic support of the IEEE Mauritius Section members, and the faculty members and students of the University of Mauritius.

We look forward to seeing you at EDAPS 2024 (Goa, India).

EDAPS 2023 Organizing Committee

Picture of the attendees on 2nd Day

Professor Madhavan Swaminathan delivering his keynote presentation

IEEE-EPS EDAPS 2023

Welcome to the 2023 IEEE EPS (Electronics Packaging Society) Conference on Electrical Design of Advanced Packaging and Systems (EDAPS)

Sugar Beach Resort, Wolmar, Flic-en-Flac, Republic of Mauritius, Dec. 12-14th, 2023

Website: edaps.org | Contact: admin@edaps.org
IEMT 2024 Call for Papers

IEEE IEMT 2024 invites you to submit your work to the 40th IEMT 2024 that will be held in G Hotel, Penang, Malaysia. It is an international event organized by the IEEE-EPS, Malaysia Chapter, with co-sponsorship from IEEE Electronic Packaging Society (EPS). IEMT 2024 welcomes papers covering electronics packaging technology in diverse semiconductor market. This segment includes telecommunication, data center, automotive, EV, healthcare, aerospace, defense and others.

For more information, kindly visit Call for Paper - IEMT 2024.

Upcoming Conferences

In pursuit of its mission to promote close cooperation and exchange of technical information among its members and others, the EPS sponsors and supports a number of global and regional conferences, workshops and other technical meetings within its field of interest.

All of these events provide valuable opportunities for presenting, learning about, and discussing the latest technical advances as well as networking with colleagues. Many produce publications that are available through IEEE Xplore.

NEW: To highlight the best/outstanding papers selected from each of the EPS flagship conferences (ECTC, ESTC and EPTC), travel funding will be provided to attend another EPS flagship conference. One author will be invited to present their best/outstanding paper (up to US$2,125 for intercontinental travel and up to US$1,375 for intracontinental travel). Only one trip per paper will be allowed (one co-author can be included; preference for original presenter) and can only be taken within 12 months of award.

2024 Pan Pacific Strategic Electronics Symposium (Pan Pacific)
Kohala Coast, HI USA
Jan 29, 2024–Feb 1, 2024

2024 40th Semiconductor Thermal Measurement, Modeling & Management Symposium (SEMI-THERM)
San Jose, CA USA
Mar 25, 2024–Mar 29, 2024

2024 25th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)
Catania, Italy
Apr 7, 2024–Apr 10, 2024

2024 IEEE 28th Workshop on Signal and Power Integrity (SPI)
Lisbon, Portugal
May 12, 2024–May 15, 2024

2024 35th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)
Albany, NY USA
May 13, 2024–May 16, 2024

2024 23rd IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITHERM)
Aurora, CO USA
May 28, 2024–May 31, 2024

2024 IEEE 74th Electronic Components and Technology Conference (ECTC)
Denver, CO USA
May 28, 2024–May 31, 2024

2024 IMAPS Nordic Conference on Microelectronics Packaging (NordPac)
Tampere, Finland
Abstract Submission Date: Jan 31, 2024
Jun 11, 2024–Jun 13, 2024

2024 IEEE International Conference on Microwaves, Communications, Antennas, Biomedical Engineering and Electronic Systems (COMCAS)
Tel Aviv, Israel
Jul 9, 2024–Jul 11, 2024

2024 IEEE 10th Electronics System-Integration Technology Conference (ESTC)
Berlin, Germany
Sep 11, 2024–Sep 13, 2024

2024 IEEE 69th Holm Conference on Electrical Contacts (HOLM)
Annapolis, MD USA
Oct 6, 2024–Oct 10, 2024
Top Conference Papers Based on Usage

2023 IEEE 72nd Electronic Components and Technology Conference (ECTC) (May 30–June 2, 2023)

CoWoS Architecture Evolution for Next Generation HPC on 2.5D System in Package
Yu-Chen Hu; Yu-Min Liang; Hsieh-Pin Hu; Chia-Yen Tan; Chih-Ta Shen; Chien-Hsun Lee; S. Y. Hou

Advanced Packaging Design Platform for Chiplets and Heterogeneous Integration
Lihong Cao; Chen-Chao Wang; Chih-Yi Huang; Hung-Chun Kou

Supercarrier Redistribution Layers to Realize Ultra Large 2.5D Wafer Scale Packaging by CoWoS
S. Y. Hou; Chien Hsun Lee; Tsung-Ding Wang; Hao Cheng Hou; Hsieh-Pin Hu

Integrated Optical Interconnect Systems (iOIS) for Silicon Photonics Applications in HPC
Harry Hsia; S. P. Tai; C. S. Liu; C. W. Tseng; S.W. Lu; Yutung Wu; C. C. Chang; Jason Wu; K. C. Yee; C. Y. Wu; C. H. Tung; Douglas C.H. Yu

Thermal Improvement of HBM with Joint Thermal Resistance Reduction for Scaling 12 Stacks and Beyond
Taehwan Kim; Jonggyu Lee; Youngdeuk Kim; Hwanjoo Park; Heejung Hwang; Haegoon Kim; Dong Wook Kim


Topology Optimized Fin Designs for Base Plate Direct-Cooled Multi-Chip Power Modules
Aniket Ajay Lad; Eric Roman; Yue Zhao; William P. King; Nenad Miljkovic

Capillary-activated scalable microporous copper microchannels for two-phase thermal management of semiconductor materials
Sujan Dewanjee; Gaurav S. Singhal; Jiaqi Li; Danny Lohan; Shailesh N. Joshi; Paul V. Braun; Nenad Miljkovic

Liquid jet impingement cooling of high-performance interposer packages: a hybrid CFD – FEM modeling study
H. Oprins; Tiwei Wei; Vladimir Cherman; E. Beyne

A Novel Scalable Modular Immersion Cooling System Architecture for Sustainable Data Center
Carrie Chen; Jiahong Wu; Jun Zhang; Ying-Shan Lo; Allen Liang; Checa Hung; Nishi Ahuja; Qing Qiao

A Simulation Study On SSD PCB Warpage During Reflow: From Understanding To Improvement
Quang Nguyen; Christopher Glancey; Kal Wilson; Mark Tverdy

2022 9th Electronic System-Integration Technology Conference (ESTC) (September 13–16, 2022)

Thi Huyen Le; Oliver Schwanzit; Ivan Ndig; Friedrich Mueller; Tanja Braun; Martin Schneider-Ramelow

10 µm and 5 µm Die-to-Wafer Direct Hybrid Bonding
Emilie Bourjot; Alice Bond; Carine Ladner; Nicolas Bresson; Stéphane Moreau; Viorel Balan; Arnaud Cornéliois; Renan Bouis; Catherine Euvrard; Noura Nadi; Loic Sanchez; Frank Fourmel; Nicolas Raynaud; Pascal Metzger; Eric Ollier

Low Height Wire bond Looping Technology using Wedge Bonding for the MMIC Package
Ah-Young Park; Jae Hak Lee; Seungman Kim; Sumin Kang; Seongheum Han; Seong-Il Kim; Jun-Yeob Song

Novel Cu-nanowire-based technology enabling fine pitch interconnects for 2.5D/3D Integration
Adil Shehzad; Ran Yin; Juliana Panchenko; Maik Müller; Steffen Bickel; Olav Birlem; Sebastian Quednau; Jürgen M. Wolf

Impact of Through Glass Vias Filling on the Performance of Passive Thermal Cooling in Photonic Packages
Parnika Gupta; Padraic E. Morrissey; Peter O’Brien; Kevin Kröhner; Markus Wöhrmann; Michael Schiffer; Christian Kelb; Norbert Ambrosius; Martin Schneider-Ramelow

2022 IEEE 24th Electronics Packaging Technology Conference (EPTC) (December 7–9, 2022)

Demonstration of 50 nm Overlay Accuracy for Wafer-to-Wafer Bonding and Further Improvement Study
Hajime Mitsuishi; Hiroshi Mori; Hidehiro Maeda; Mikio Ushijima; Masanori Aramata; Minoru Fukuda; Masashi Okada; Masahiro Kanbayashi; Toshimasa Shimoda; Isao Sugaya

Reduction of Aluminum Fluoride Formation during Fluorinated Plasma Etching of Dielectric Passivation Layer over Aluminum Pad
Darshini Senthilkumar; Kalyn Lim Tien Shee; B.S.S. Chandra Rao

700nm pitch Cu/SiCN wafer-to-wafer hybrid bonding
Soon-Aik Chew; Serena Iacovo; Ferenc Fordor; Sven Dewilde; Katia Devriendt; Joeri De Vos; Andy Müller; Gerald Beyer; Eric Beyne

Reliability of lead-free solders for die attach in automotive power modules
Bettina Ottinger; Joshua Holverscheid; Sebastian König; Edgar Jerichow; Sebastian Lunz; Mario Sprenger; Lars Müller; Christian Goth; Jörg Franke

Cu CMP Dishing Control for Fine Pitch Wafer-to-Wafer (W2W) Hybrid Bonding
Hong Miao Ji; Gim Guan Chen; K.-J. Chui
Abstract—The rapid emergence of a multitude of machine learning (ML) models with trillions of parameters has highlighted the need for high performance compute systems leveraging Artificial Intelligence (AI) accelerators with disaggregated memory. Considering the demanding bandwidth, density, energy and latency requirements, Silicon photonics is the technology of choice to realize these architectures. Scalable solutions can only be implemented by developing novel and reliable packaging schemes, with emphasis on thermal budgeting, reduced parasitics, and increased bandwidth density. This article covers some challenges seen when packaging photonic circuits for AI/ML systems and some innovative solutions that have been developed in the field.

Keywords—Packaging, PIC, Integration, Artificial Intelligence, Light Sources

I. INTRODUCTION

With the advent of GPT-4 The rapidly growing size and complexity of Machine learning (ML) and Artificial Intelligence (AI) models has crossed the trillion-mark w.r.t parameters involved [1]. The turn of the decade has seen a large number of ML machine learning models made public, each with billions of parameters. Fig. 1 shows the exponential trend of number of parameters in published ML models over the last five decades. This exponentially growing number of parameters also brings in the need for parallelization of data over tens of thousands of memory and processor nodes. Each of these nodes requires ultra-low latency and power to meet standards, Tb/s optical I/Os and high-speed interconnects between the multiple processing units involved. For instance, early publications report NVIDIA DGX systems consisting of 8 H100 GPUs, designed with a 7.2 Tb/s off chip bandwidth [2].

Despite developments in new interconnect technologies like NVLink and CXL, the bandwidth and energy requirements of the compute-loads of the future cannot be met with this technology since it primarily relies on electrical interconnects [3].

From a standpoint of computing, conventional computers are based on a centralized processing architecture (with a physically separate memory), more suited towards sequential execution. The current AI/ML workloads tend to be distributed and massively parallel and cannot be implemented efficiently on conventional
processor architectures. Matching hardware to the algorithms themselves would be necessary for faster and energy-efficient processing.

Silicon photonic integrated circuits show great promise in this regard as photons guided by a Silicon waveguide inherently dissipate lower power than electrons guided through metal traces. In addition, higher data rates can be achieved using Opto-Electronic (OE) conversion through modulators, paving the way for co-packaged optical I/O and CPUs/GPUs [4-5].

II. ROLE OF PHOTONICS IN AI/ML

The role of photonics in AI/ML is not to replace conventional computers but to enable applications which require parallelization, low latency and high bandwidth such as nonlinear programming, machine learning acceleration (matrix multiplications etc.) and quantum computing.

Disaggregated architecture for AI/ML computing is one such application that decouples memory and storage (DRAM) from processors and accelerators (e.g., CPU, GPU) [6]. Disaggregation also provides large amounts of memory access at reduced latency for processor nodes using features such as remote direct memory access (RDMA) and GPU-Direct. The signal pathways in such architectures can be implemented by leveraging standard silicon photonic platforms offered by several foundries such as GF, TSMC, Tower Semiconductor, IMEC, AMF and the rest [7-10].

Though AI/ML chips are leveraging photonics to overcome the issues mentioned earlier, they still require a large density of electrical interconnects for a range of functions such as control systems for ring resonators, temperature stabilization, modulator drivers, Trans-Impedance Amplifiers (TIA) for photodiodes, control loops for laser diodes, and in general, biasing electrical or optoelectronic devices on the PIC/ASIC. In fact, the required number of electrical ports is reported to scale quadratically with the number of optical ports [11]. The approach employed by most entities in the field is integration of CMOS electronics and photonics.

III. PHOTONIC INTEGRATION

Typical integration approaches employed in Photonic Integrated Circuits (PICs) for datacenter applications are equally suitable for photonic AI/ML processors. Fig. 2 shows simplified illustrations of a few integration techniques that are historically/commonly used [12].

Fig. 2(a) illustrates Monolithic Integration, an approach that integrates electronics and photonics on the same substrate. A typical example is the 45SPCLO process offered by GF [13]. Though this is theoretically the most appealing integration method and aims to balance electronic circuit performance with that of photonics, the differences in the feature sizes involved often lead to a compromise on the Electrical IC (EIC) with respect to size and power. As an example, Luxtera (now part of Cisco Systems Inc.) initially developed a monolithic transceiver.
One of the most popular approaches to integration in systems involving digitally controlled analog electronic circuits is 2D Integration (Fig. 2(b)), where the application specific integrated circuit (ASIC) (serving as the EIC) and the PIC are mounted on a common PCB, with wire bonds routing signals to both. However, this solution is not readily scalable. As the number of electrical I/Os increases, the area occupied by wire bonds and associated pads makes routing physically impossible under standard DRC constraints. In addition, larger chip sizes are necessitated, making it prohibitively expensive. Lastly, the wire bonds themselves add significant parasitic inductance and reduce the bandwidth of any high-speed devices that they interface to.

The second popular option that most of the industry has moved towards is flip chip bonding where the ASIC and the Photonics IC are designed, optimized, and sometimes even processed separately in different foundries. The ASIC and the PIC are designed to have matching electrical pads with a common interposer (Fig. 2(c)) onto which they are bonded. This scheme is called 2.5D Integration. As compared to wire bonds, the electrical interconnections have reduced parasitic inductance owing to their short lengths. Since the number of interconnects also scales naturally with the area of the ASIC and PIC, to support higher electrical I/O density, and to further minimize parasitics, the ASIC can also be flipped and bonded or soldered onto the PIC. This technique, termed 3D Integration is represented in Fig. 2(d). The main differentiating factor from 2.5D integration is that a third chip such as memory is now integrated onto the ASIC. However, using a PIC as an interposer between the PCB and ASIC is sometimes still referred to as 3D Integration in literature.

One of the major drawbacks of the 2.5D/3D integration approach is thermal management on the PIC and mechanical stability of the integrated system. Since the ASIC is generally the major source of heat, with the heat dissipated varying under the operating load, some elements on the PIC might require well designed control loops to prevent performance drifts. Typically, modulators based on rings, multiplexers based on rings and any passives that are sensitive to temperature are affected. This is particularly true since PICs for acceleration and computing typically employ several wavelengths across different channels and corresponding Multiplexer (MUX) and Demultiplexer (DEMUX) elements that tend to be temperature sensitive. If the sizes of the ASIC and PIC become large, flexing/warping of dies is another problem that needs to be considered.

As mentioned, solutions such as addition of control loops to maintain devices in the desired operation regimes and designing devices to be athermal are approaches that are employed to overcome the issues outlined above.

Some foundries also offer Through-Dielectric-Vias (TVD) and Through-Silicon-Vias (TSV) to route signals from the ASIC to the PIC, and substrate to the PCB. TSVs bring in high integration density, simplify routing to an extent (as traces need not be routed over extended distances to wire bond pads), and are great for realizing PICs for AI/ML applications. However, they introduce added thermal complexities as they are sources of heat if they carry sizable currents. Depending on TSV density requirements, the mechanical stability of the dies also needs careful consideration. Though TSVs increase the electrical interconnect density, exclusion zones often limit the placement of optical devices and involve more reliability tests under different mechanical stress conditions. Nevertheless, foundries are now invested in offering TSVs as a process capability and it is a scalable path forward w.r.t integration approaches.

High performance compute systems are developed to handle AI/ML workloads by integrating processor dies, high-bandwidth memories (HBM), and co-packaged optics in a single 2.5D/3D package (System in-package (SiP)). Considering the cost and limited number of available wavelengths (8, 16 or 32) in today’s Wavelength Division Multiplexed (WDM) sources, it is highly desired to achieve +100Gb/s/wavelength data-rates to increase bandwidth density and reduce the static laser power overhead for direct detect applications [15].

IV. PACKAGING LIGHT SOURCES

One of the continual challenges faced by Silicon photonics is light generation on chip. Though the lack of developed on chip light sources does not gate the development of AI/ML PICs, in many such implementations, there is no need to route light off the chip, making it desirable to have an integrated light source to benefit from the scalability and size benefits it would bring in. Some potential solutions that have been explored include strain engineering in Si/Ge to realize light sources, rare-earth element doping in Si waveguides, and integration of III-V light sources onto PICs. The latter cannot be directly or easily achieved owing to the lattice mismatch between Si and III-V materials. However, approaches typically involve bonding light sources implemented on III-V and evanescently coupled onto the PIC, and micro-packages containing internal light sources.

Integration of group III–V dies with Si has also been achieved by bonding wafers with group III–V quantum wells to silicon waveguides [16,17]. Finally, group III–V quantum dots (QD) have been grown directly on silicon as
unlike quantum well based lasers, QDs can tolerate lattice mismatch without the loss of their optical gain properties.

Intel Labs recently announced a fully integrated 8-channel DFB laser array to serve as Dense Wavelength Division Multiplexed (DWDM) light sources with controlled wavelength spacing and power [18]. The approach involves patterning waveguides on Silicon on Insulator (SOI) prior to a III-V wafer bonding process and marks a significant advancement in terms of the ability to fabricate lasers in high volume and integrate them reliably with Si PICs.

Despite the developments listed above, many entities in the field tend to prefer external laser packages with either edge or grating coupled interfaces on the PIC, where the laser is mounted on the printed circuit board (PCB). Typically, decoupled heat sinks are designed to reduce thermal crosstalk between the laser and the PIC.

Regardless of the light sources used, some added challenges seen in the data center products such as alignment tolerances during fiber array unit (FAU) attach are applicable in this application as well. If large substrates are used alongside high fiber counts, the FAU attach process should have the ability to deal with warpage which can introduce additional loss at the gratings or edge couplers. The epoxy selected for the FAU attach process should have a suitable coefficient of thermal expansion (CTE) and remain stable when subjected to significant thermal cycling with the typical temperature range being 70°C.

V. SUMMARY

Packaging is a complex, interdisciplinary process which requires expertise in materials engineering, fabrication processes, mechanical and thermal design, assembly, and photonics while keeping in mind the end application. The growth of Silicon photonics and the added demands in terms of I/O density, latency and bandwidth density in terms of Tb/s per mm of package edge (referred to as the shoreline), while managing demanding thermal conditions and ensuring a small footprint have served to reinforce the importance of developing scalable packaging solutions.

Packaged PICs should eventually satisfy industry reliability standards in terms of life expectancy, aging, moisture sensitivity and thermal tolerance. In particular, PICs for telecommunications (or in general, PICs used in transceivers) are expected to meet the Telcordia (Bellcore) testing standards [19], with the added customer requirements (generally less demanding). Hence, there is a general move towards the development of standard package designs, reliable integration methods and increased collaboration between design houses, foundries and packaging partners as the proliferation of Silicon Photonics as a technology in the industry is more governed by packaging than design.

REFERENCES


Abstract

Sustainable electronics is a broad concept that encompasses environmental, social, and economic considerations across the device life cycle. It aims to identify strategies to minimize natural resource usage and CO₂ emissions. It goes beyond net-zero manufacturing and embraces the research of new materials, efficient re-cycling and re-use to achieve sustainability by design. Here, we provide a picture of the state and roadmap towards net-zero targets of semiconductor industry and the situation of electronic waste management and recycling. Risks associated with raw materials are also briefly discussed with emphasis on European Commission studies and directives. The paper is a starting point for sustainable electronics and far from being comprehensive, as it omits cutting-edge research in new materials and technologies.

I. Introduction

The dramatic advancement in information and communication technology (ICT) in the last decades has revolutionized our daily lives. The rise in ICT has resulted in a proliferation of consumer devices, networking technologies, and data centres. Despite its enormous societal benefits, ICT has incurred an increasing environmental footprint [1]. Here are a couple of key figures to crystallize the current situation:

• ICT accounted for up to 3% of the global energy demand as of 2015 with a projected 7% by 2030. The equivalent CO₂ emission in 2021 reached 900 megatons which is about 1.8% of global anthropogenic emissions;

• within this sector, Integrated Circuits (IC) chip manufacturing plays a significant role in the overall life cycle of most consumer products. For example, research indicates that nearly 75% of the carbon footprint of a mobile device results from its manufacturing, with almost half of that attributable to IC manufacturing;

• recent studies estimate that the IC manufacturing industry could contribute up to 3% of total emissions by 2040. This projection reflects the substantial annual growth of the IC industry and the increased energy consumption and complexity associated with each new technology node.

Figure 1 is illustrative of the increasing CO₂ emissions and resource consumption of silicon foundries.

Another problem relates to electronic waste (e-waste) that is exacerbated by the proliferation of electronic devices and systems, and the shortening of the lifetime of some consumer products. In 2019, the world generated 53.6 million tons of e-waste, of which less than 20% is documented to be recycled. This e-waste is expected to increase at a rate of 6.5% yearly, propelled by the Internet of Things (IoT) scenario, which predicts the deployment of trillions of smart connected devices. Progress in disposal has been hindered by the large palette of products and materials making e-waste one of the most complex waste streams. IoT electronics are also increasingly integrated in other – formerly non-electronic – products, straining the idea of one waste stream even further. This complexity and the high costs of proper disposal lead to the deplorable practice of exporting e-waste to developing countries, where most of it ends in open waste dumps and results in environmental and health hazards for local residents, even when low tech recycling is occurring at these sites.

These numbers are alarming and indicative of a situation that is no longer sustainable in the long term. Solutions require a holistic approach that accounts for the end-to-end impact of electronic devices and sees the synergetic contributions of industry, governmental bodies and research labs.

Sustainable electronics is a concept that refers to the design, production, and use of electronic devices in a manner that minimizes their negative impact on the environment and human health, while also considering their entire lifecycle. This approach aims to reduce resource consumption, hazardous materials, energy consumption, and electronic waste (e-waste) while promoting renewable materials and efficient manufacturing processes.

References


To achieve sustainability in electronics, a holistic approach is required that articulates along three pathways: (i) new sustainable materials; (ii) efficient manufacturing; (iii) efficient recycling, all converging to the concept of “safe and sustainable by design” that includes safety, environmental, social, and economic sustainability requirements into the specifications. Life Cycle Assessment (LCA) of electronic systems is, however, complex and it must go beyond the analysis of operational footprint and consider end-to-end impact (Figure 2).

The paper is organized in three main paragraphs that discuss the operational and embodied footprint of semiconductor devices (paragraph II) with a focus on the Greenhouse Gas Protocol (GHG) protocol classification of CO₂ emissions and the trends related to technology node scaling. Paragraph III is about critical raw materials and the recent initiatives of the European Commission to minimize supply risks and economic independence. Paragraph IV focuses on the waste generated by electronic devices and products and the recycling of metals.

II. Operational and Embodied Footprint
Moore’s law has enabled the fabrication of systems that have billions of transistors and 1,000 higher energy efficiency. For salient applications, such as AI, molecular dynamics, video encoding, and cryptography, systems now comprise specialized hardware accelerators that provide orders-of-magnitude higher performance and energy efficiency. Moreover, data centres have become more efficient by consolidating equipment into large, warehouse-scale systems, and by reducing cooling and facility overhead to operate at near-optimal power usage effectiveness. However, assessment of the energy and resource consumption of computer systems and architecture must go beyond their operational lifetime and consider the full lifecycle. Similar to infrastructure, optimization must account for operational (OF) and embodied footprint (EF). Therefore it is possible to categorize carbon emissions into OF- and EF-related activities with the former from hardware use and energy consumption and the latter from facility infrastructure construction and chip manufacturing, such as procuring raw materials, fabrication, packaging, and assembly. Figure 1 shows the evolution over the last decade of OF and EF for two electronic systems: (i) the iPhone and (ii) the data centre. The operational footprint has decreased due to the improved energy efficiency of the computing devices while the embodied footprint has increased due to the increased complexity of the manufacturing of more sophisticated hardware. For consumer electronic devices (i.e. iPhones) the dominating source of carbon footprint has shifted from being OF- to CF. The data centre operational emissions, between 2010 and 2018, have increased by 6% while infrastructure capacity, which corresponds to embodied hardware emissions, has increased by a factor 6x (Figure 3).

Another remarkable example comes from the 2019 “Apple Environmental Responsibility Report” data [2]. In 2019, Apple reported a carbon footprint of 25 million metric tons of CO₂. Hardware manufacturing of integrated circuits (IC’s), boards and flexes, displays, electronics, steel, and assembly, accounts for over 74% of Apple’s footprint. By comparison, operational emissions from running Apple’s devices amount to 19% of the total emissions.

A. GHG protocol
A common method accounting standard for quantifying organization-level carbon output is the GHG protocol. Many technology companies, including AMD, Apple, Meta,
Google, Huawei, Intel, and Microsoft publish annual sustainability reports using the GHG Protocol, which categorizes emissions into scope 1, scope 2, and scope 3 [3].

- **Scope 1** emissions arise directly from fabs, primarily from process gases with high global warming potential (GWP) that are used during wafer etching, chamber cleaning, and other tasks; they can also come from high-GWP heat transfer fluids that may leak into the atmosphere when fabs use them in chillers;
- **Scope 2** emissions arise directly from purchased electricity, steam, heating, and cooling equipment; the major sources include production tools and facilities/utilities;
- **Scope 3** emissions include all other indirect emissions in a company's value chain; upstream emissions are those generated by suppliers or their products, while downstream emissions are related to the usage of products containing semiconductors.

### B. Footprint of IC manufacturing

A closer look at the manufacturing of 12-inch wafers reveals that about 60% of the carbon footprint derives from the energy required during the processes and about 40% is related to direct emission from gas and wafer supply/production (Figure 4). The use of renewable energy sources will reduce the footprint drastically. The plot shows that renewable energy provides up to a 64 reduction in emissions from electricity, and overall emissions for wafers drop by 2.7 [1].

In July 2020, TSMC signed a 20-year deal with Orsted to buy the entire production of two offshore wind farms under development off Taiwan’s west coast. The plot in Figure 4, however, highlights the fact that while the transition to renewables is the most straightforward strategy to drastically reduce the footprint, it will not be enough to reach CO2 neutrality. The measures currently being implemented by semiconductor companies will fall short of aligning the industry with a 1.5°C trajectory by 2030. In fact, there is a risk that Scope 1 and 2 emissions could substantially increase beyond their current levels, driven by the rising production volume in the semiconductor sector and the transition to advanced nodes associated with higher expected emissions intensity. To chart a course toward a net-zero trajectory by 2030, the semiconductor industry requires a unified and vigorous approach that maximizes the application of current strategies while actively pursuing the development and integration of new technologies. Achieving this goal demands a collective effort to attain net-zero emissions by 2050, necessitating a 95% reduction in Scope 1 and 2 emissions compared to the 2020 conservative scenario. Specifically addressing Scope 1 emissions, semiconductor entities must significantly amplify their commitment to emission reduction. This objective calls for extensive utilization of existing technologies. Consider the following initiatives:

- **Process gas**: Semiconductor fabrication facilities could viably implement gas-abatement systems covering an average of 90 percent of tools. Optimization of processing gas chemistry is crucial to curtail greenhouse gas (GHG) usage. For instance, replacing nitrogen trifluoride (NF3) and tetrafluoromethane (CF4) with fluorine (F2) gas—boasting zero global warming potential—is a critical measure.
- **Heat transfer fluid (HTF)**: The industry needs to replace a minimum of 70 percent of HTF with low Global Warming Potential (GWP) alternatives. Additionally, efforts to minimize chiller leakage are essential.
- **Fuel consumption**: Semiconductor companies should transition from the current fuel supply to cleaner options such as hydrogen or biomass to effectively reduce emissions.

C. Technology node scaling

It is worth mentioning that current Life Cycle Assessment (LCA) methods are far from being complete and accurate, especially when they deal with the semiconductor industry. There are data sets, but they all have limitations and cannot be applied for all ICs on the market. The reasons lay in the lack of information on company and device specific processes as these are usually confidential. There is no common approach to generate the...
right data to cover the complexity of the ICT technologies and products consistently and fair. However, one study from IMEC estimates that the current situation will get worse with the technology node scaling [4]–[6]. In particular, the plots in Figure 5 show the energy consumption and CO₂ emission when the technology node scales from 28nm to 2nm. It is worth noting that the greatest increase in energy comes from the front end of the line processes, while the CO₂ emissions are greatly impacted by NF₃ gases that have a global warming potential that is 17.000 times more potent than CO₂.

D. Roadmap of technology players

Downstream tech players as Meta, Microsoft, Amazon, Qualcomm etc., are also actively working towards net-zero targets. Apple, for instance, plans to cut emissions by 75% along the supply chain. While this effort is laudable, semiconductor companies are still behind many customers because their sustainability programs started later (Figure 6). To meet customer expectations and ensure sustainability, many semiconductor companies have already begun to rethink their emissions goals [7].

III. Critical Raw Materials

The mounting pressure on resources is set to intensify, driven by a confluence of factors that include a burgeoning global population, industrialization, digital transformation, escalating demands from developing nations, and the shift towards climate neutrality. This heightened demand encompasses metals, minerals, and biotic materials crucial for low-emission technologies and products. According to Organisation for Economic Co-operation and Development (OECD) projections, the global appetite for materials is poised to more than double, surging from its current 79 billion tonnes to an anticipated 167 billion tonnes by 2060. This anticipated trajectory portends an intense global competition for resources in the coming decade, potentially leading to a shift in reliance from today’s oil dependency to a new dependence on critical raw materials. One of the essential prerequisites for attaining climate neutrality is the assurance of a stable and eco-friendly provision of primary and

Figure 5. Energy (top) and CO₂ equivalent emissions for some technology node. Image readapted from [6].

Figure 6. Roadmap of many end customers to achieve net-zero emission along their supply chain. Image taken from [7].
secondary raw materials, with a specific emphasis on critical raw materials. These resources are vital for key technologies and strategic sectors, including renewable energy, electric mobility, digital technology, space exploration, and defence. European Commission (EC) recognizes access to resources as a strategic security question to fulfill its ambition towards 2050 climate neutrality and increasing our climate ambition for 2030. In 2018 the EC launched the Raw Materials Initiative (RMI) [8] that pursues a diversification strategy for securing non-energy raw materials for EU industrial value chains and societal well-being. Studies accounting for the economic importance and supply risks have classified and identified critical raw materials for selected technology sectors and applications [9], [10]. Figure 7 report the global suppliers of critical raw materials (CRMs) assessed in the EU CRM report 2020 [10].

A. CRMs in Digital Technologies

Digitisation and digitalisation will transversally affect all the various technologies and sectors explored in the EC report as they increase productivity and efficiency of the industry and enable more customised and diversified product portfolios. Through “Internet of Things”, connected robots, autonomous vehicles and sensors will be more and more integrated in industrial processes, common goods and services, across the value chains.

One of the primary outcomes of the digitalization era is the generation and storage of an immense volume of data across data centres, enterprise infrastructures, and various endpoints, including PCs, smartphones, and IoT devices. The collective sum of this data is referred to as the ‘global datasphere,’ and it is undergoing exponential growth. According to the International Data Corporation, the global datasphere is projected to expand from 33 Zettabytes (ZB) in 2018 to a staggering 175 ZB by 2025. This escalating demand for data will significantly impact data storage technologies, leading to an increased need for materials used in memory production. As estimated by Ku in 2018 [11], accommodating the 2025 global datasphere would require approximately 80 kilotons of neodymium, which is roughly 120 times the current annual demand for this material in the European Union (EU). Alternatively, adopting emerging technologies like ferroelectric RAM would necessitate around 40 kilotons of platinum, representing approximately 600 times the EU’s current yearly demand for this precious metal. Digitalization will be also accompanied by the progression in sales of ICT devices, mainly smartphones. Despite the increasing sales of certain electronic devices, the projected utilization of associated critical raw materials is expected to either remain stagnant or experience only modest growth for materials such as palladium, gallium, dysprosium, and neodymium. However, the case of tantalum, primarily used in electronics, presents an intriguing scenario: the application of tantalum in electronic devices alone could potentially surpass the overall current usage of this material across all applications. Likewise, the advancement of digital technologies, particularly electronic displays, including flat screens and touchscreens, has significantly driven the demand for indium utilized in indium-tin-oxide (ITO) thin-films. Historically, indium witnessed a more than fivefold increase in primary production between 1993 and 2013. Indium is gaining increased attention due to its relatively high economic significance, the absence of substitutes, extraction as a by-product from carrier metal ores, low processing recovery efficiency, and a lack of recycling at the end of its product life cycle [12]. Figure 8 summarizes the main raw materials adopted for digital technologies and their functionality.
IV. E-Waste

The proliferation of electronic devices and systems, and the shortening of the lifetime of consumer products have exacerbated the problem of electronic waste (e-waste). E-waste, driven by the rapid growth of the Internet of Things (IoT), is expected to increase by 6.5% annually. European Commission has put in place two pieces of legislation: the directive on waste electrical and electronic equipment (WEEE Directive) and the directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS Directive). As a result, today, European countries are able to recycle about 66% of their e-waste, but, they still deliver more than 10 million tons per year to incinerators or to the landfill, with the risk of leaching heavy metal in the ground water, and with the emission of toxic fumes into the air [4]. Figure 9 shows the recycling rate of e-waste for the EU countries [13]. Progress in the disposal has been hindered by the large palette of products available, where the variation in the materials and components makes e-waste one of the most complex waste stream. The problem is further exacerbated by the presence of toxic and hazardous materials, such as lead and cadmium, which cannot be treated with conventional methods. The expense of proper disposal, hence, leads to the shipment of large amounts of e-waste to developing countries (i.e. China, India, Pakistan, Nigeria) where, despite the intents of national regulations, it is treated as general refuse with recovery of only a few materials of value. As dioxins, furans, and heavy metals are released, harm to the environment, workers, and area residents is inevitable [14], [15].

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V. Conclusion

In this paper, we have presented an overview of the current status and the path leading to net-zero objectives within the semiconductor industry, with reference to the broader sustainable electronics concept. Additionally, we have briefly examined the landscape of electronic waste management and recycling. We have touched upon the risks associated with raw materials, placing emphasis on studies and directives from the European Commission.

Sustainable electronics require new design approaches to incorporate these and additional complex topics in the industrial development practices. Fundamentally new materials that are economically and environmentally sustainable and radically improved manufacturing processes that minimize the consumption of resources are needed as the basis of these developments. Research in these areas is started, but transfer to industry takes time – possibly more time than we have in terms of climate goals and sustainable development. So more engineers and developers need to engage with sustainability now.

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References


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