



IEEE ELECTRONICS PACKAGING SOCIETY Newsletter



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Driving Innovation in Microsystem Packaging /// EPS.IEEE.ORG

PRESIDENT'S COLUMN



Kitty Pearsall
Boss Precision, Inc.
Austin, TX

Hi there from sunny, hot Texas!

As you know, EPS is the leader in the dissemination of technical knowledge in electronics packaging and is viewed as being at the forefront of the evolving electronics marketplace by the global packaging community. Per Market Research Future (MRFr), the electronic packaging market is estimated to grow to 3.12 B US\$ by the end of 2030. The electronic component industry has seen several innovative and emerging trends put a stake in the

ground and are having great impact. As I enter the last six months of my EPS Presidency, I must admit that I will miss being in this extremely rewarding role.

Now, I want to share some comments I recently made during the EPS 73rd ECTC Luncheon. "What is electronic packaging today"? Anindya Poddar, director of research and development for TI's Packaging group, expressed this nicely:

"Packaging is the bridge that enables electronic circuits to interact with the real world," Whether you're watching your flat-screen television, listening to your smart earbuds, appreciating the efficiency of machines in an automated factory or riding in an autonomous vehicle, the things we enjoy are enabled through the miniaturization and integration of packaging."

This statement, while made in 2021, is still relevant in 2023. Emerging market applications continue to drive this growth through applications that include automotive; medical, health, wearables; mobile and telecommunications; high-performance computing; smart manufacturing; internet of things; and artificial intelligence. Innovation in advanced packaging technology architecture continues to enable future semiconductor requirements.

I want to highlight a few achievements in support of our Strategic Plan for the past 12 months:

- While our society is small, we have a worldwide footprint that is growing. EPS now has 43 chapters and 28 student chapters. We can boast that our newest chapters include Guangzhou-China and Vietnam with new student chapters in Sri Sai Ram Engineering College-India, Trident Academy of Technology-Kolkata, and 2 in

Africa: Addis Ababa University and Enugu State University of Science & Technology.

- Last year we added two new geographies to the 25+ EPS conferences: Africa and India. The 1st Conference in Africa was held at the Addis Ababa University last year and again this past February. Partnering with the India Electronics and Semiconductor Association (IESA) EPS held its 1st Education Workshop in Bangalore last December and plans to do this again this year.
- Through partnering with other IEEE societies and Technical Activities Committees and Councils, EPS now has representation on the Quantum Initiative, the Nanotechnology Council, Future Directions, Digital Reality, and the IEEE/TA Education task force.
- The 12 Technical Committees (TCs) continue to increase the technical content and depth of the monthly EPS Newsletter through articles with a keen focus on disruptive technologies. To date each TC has provided two articles to the newsletter per calendar year.
- The CPMT Journal has been listed as a "high performer" in the top quartile for 2 successive quarters for average weeks submitted to 1st decision and average weeks submitted to online post.
- Non-Curricula Educational Materials and Activities for Students and Young Professionals are being developed as best practices. Two workshops have been held on said topic: the first, in India and the 2nd in Europe.
- The EPS Distinguished Lecturer Program has been strengthened through improved policies, recruitment, reporting, and CEU offerings.

(continued on page 11)

NEWSLETTER SUBMISSION DEADLINES

1 December 2023 for Winter issue 2024
15 June 2024 for Summer issue 2024

Submit all material to d.manning@ieee.org

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2024 Term End: Regions 1-6, 7, 9—Benson Chan, Pradeep Lall, Wolfgang Sauter, Region 10—Kishio Yokouchi, Chuan Seng Tan, Chin-Pin (CP) Hung
2025 Term End: Regions 1-6, 7, 9—Jose Schutt-Ainé, Luu Nguyen, Region 8—Karlheinz Bock, Tanja Braun, Grace O'Malley, Region 10—Shaw Fong Wong

Publications

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Chapters and Student Branch Chapters

Refer to eps.ieee.org for EP Society Chapters and Student Branch Chapters list

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2023 IEEE Rao R. Tummala Electronics Packaging Award



Sponsored by IEEE Electronics Packaging Society

“For scientific and technological leadership in “More than Moore” (MtM) packaging, co-designing, and reliability.”

Guoqi (Kouchi) Zhang
Chair Professor,
Delft University
of Technology, the
Netherlands

Prof. Zhang made outstanding technical contributions to More than Moore (MtM) packaging, co-designing, and reliability. His technical achievements enabled many key applications including energy saving via LED packaging, IoE via sensor packages, 5G via AiP, and much more. He is one of the persistent leaders of developing co-designing methods that lays down the foundation for designing for reliability, lifetime diagnostics and prognostics, virtual prototyping/qualification, and digital twin of packaging. Zhang developed an accelerated test method for LED systems that substantially reduced testing time. His accelerated test method opened the way to commercialization of LED technology and has been a key technology in reducing global energy consumption.

An IEEE Fellow, Zhang is a chair professor at Delft University of Technology, Delft, the Netherlands.



Kevin Peterson – IEEE Division II Director with IEEE EPS Technical Field Award Recipient Guoqi (Kouchi) Zhang at ECTC 2023.

2023 IEEE Electronics Packaging Society Award Recipients



Dongkai Shangguan
Indium Corporation, USA

2023 IEEE EPS Electronics Manufacturing Technology Award

For leadership in miniaturization, reliability and sustainability of high density electronics in global manufacturing across industry segment.



Erdogan Madenci
University of Arizona, USA

2023 IEEE EPS Outstanding Sustained Technical Contribution Award

For over 25 years of outstanding sustained contributions to the failure, fracture, reliability, and multi-physics analyses of electronic packaging systems.



René H. Poelma
Nexperia B.V., the Netherlands

2023 IEEE EPS Exceptional Technical Achievement Award

For exceptional contributions in the field of novel packaging materials, interconnect technology, and processes.



Shaw Fong Wong
Intel, Malaysia

2023 IEEE EPS William Chen Distinguished Service Award (formerly David Feldman Outstanding Contribution Award)

For two decades of outstanding contributions and continuous support of EPS chapter development, conferences, engagements and professional leadership, especially in Region 10.



SivaChandra Jangam
Apple Inc., USA

2023 IEEE EPS Outstanding Young Engineer Award

For outstanding contribution in development of Silicon Interconnect Fabric (Si-IF) platform, SuperCHIPs protocol for intent-die communication and for successful demonstration of this novel integration scheme for DSP system-on-IF.



Yoichi Taira
Keio University, Japan

2023 IEEE EPS Regional Contributions Award - Region 10 (Asia & Pacific)

For contribution to the growth of electronic packaging technology in Region 10 through international collaborations and significant technical achievements in optical and electrical packaging.



Yousef Safari
McGill University, Canada

2023 IEEE EPS PhD Fellowship

For contribution to large-scale heterogeneous integration, specifically, formulation of scalable methodologies and architectures, and development of EDA tools for optimization of power delivery, thermal management, and hardware security in high-performance wafer-scale chiplet-based platforms and 3D-ICs.



Electronics Manufacturing Technology Award Recipient Dongkai Shangguan with Kitty Pearsall.



Exceptional Technical Achievement Award Recipient Rene H. Poelma with Kitty Pearsall.



Outstanding Sustained Technical Contribution Award Recipient Erdogan Madenci with Kitty Pearsall.



IEEE Fellow Andrew Tay with Kitty Pearsall, EPS President.



Outstanding Young Engineer Award Recipient SivaChandra Jangam.



Regional Contributions Award Region 10 (Asia and Pacific) Recipient Yoichi Taira



William Chen Distinguished Service Award recipient Shaw Fong Wong (right) with presenter William Chen (left)

Congratulations to IEEE EPS Senior Members

New IEEE EPS Senior Members

The members listed below were elevated to the grade of Senior Member between December 2022 and April 2023.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields for a total of 10 years and have demonstrated 5 years of significant performance.

For additional information or to apply online: <https://www.ieee.org/membership/senior/>

Sylvester Ankamah-Kusi—Dalla Section
Harshpreet Singh Phull Bakshi—Dallas Section
Chandra Rao Bhesetti—Singapore Section
Xu Chen—Central Illinois Section
Dustin Demetriou—Mid-Hudson Section
Dragan Dinulovic—Germany Section
Michael Freda—Twin Cities Section
Md Hasnine—Dallas Section
Shivakumar Hunagund—Phoenix Section
Jerry Johnson—Eastern North Carolina Section

Dongsu Kim—Seoul Section
Ying Ying Lim—Tokyo Section
Hai Liu—Santa Clara Valley Section
Dairoku Muramatsu—Tokyo Section
Ovidiu-Aurel Pop—Romania Section
Ali Roshanghias—Austria Section
Nancy Stoffel—Schenectady Section
Tony Tang—Dallas Section
Yoshitaka Toyota—Hiroshima Section
Huaiyu Ye—Guangzhou Section
Jiantao Zheng—San Diego Section

ECTC 2023 Travel Award Winners

Congratulations to the winners of the 2023 ECTC travel award. The award is intended to assist students to attend ECTC.

- **Krutikesh Sahoo** University of California, Los Angeles
- **Sung Hoon Lee** Georgia Institute of Technology
- **Atsushi Shinoda** Tohoku University
- **Akari Watanabe** Kyoto Institute of Technology
- **Debabrata Mondal** Auburn University
- **Madison Manley** Georgia Institute of Technology
- **Hafiz Waqas Ali** Université de Sherbrooke
- **Hussein Hamieh** Université de Sherbrooke
- **Dong Jun Kim** Korea Advanced Institute of Science and Technology (KAIST)
- **Golam Rakib Mazumder** Auburn University
- **Kankanige Udara Somarathna** Binghamton University
- **Michael Molter** University of Illinois Urbana-Champaign
- **Varun Thukral** Delft University of Technology, Netherlands
- **Alexander Wilcher** University of Florida
- **Wei Chen** Fudan University



Left to right - Krutikesh Sahoo, Sung Hoon Lee, Madison Manley, Akari Watanabe, Golam Rakib Mazumder, Kitty Pearsall.



Left to right - Hafiz Waqas Ali, Kitty Pearsall, Hussein Hamieh, Atsushi Shinoda, Dong Jun Kim, Michael Molter, Varun Thukral, Kankanige Udara Somarathna

Congratulations to the ECTC Volunteer Award Recipients

The EPS/ECTC Volunteer Award is given to those individuals who contribute to the success of the ECTC by volunteering in one of the conference committees, year after year. Here are the 2023 EPS/ECTC Volunteer Award winners:

10 Year Volunteers

Grace Yi Li
Yu-Hua Chen
Takafumi Fukushima
Mark Gerber
Xiaoxiong Gu

Nathan Lower
Michael Mayer
Jintang Shang
Chuan Seng Tan
Paul Tiner

Masao Tokunari
G.Q. (Kouchi) Zhang
Peter Ramm

25 Year Volunteers

Harry Kellzi
Timothy Lenihan
Ping Zhou

EPS Major Awards Nomination Period Starts on September 15

The EPS Major Award nominations require online submission. The nomination period to input all the required documents runs from September 15 to January 21. The Electronics Packaging Society offers the following awards for the purpose of recognizing outstanding service and contributions to furthering the professional purposes of IEEE and EP Society.

Outstanding Sustained Technical Contributions Award: To recognize outstanding sustained and continuing contributions to the technology in fields encompassed by the EP Society.

Prize: \$3,000 and Certificate

Basis for Judging: Technical contributions must be sustained and continuing over a period of at least 15 and preferably 20 years. One major contribution will not qualify. Must be documented by open literature publications such as papers, patents, books and reports (available to the public).

Eligibility: Recipient must have been a member of IEEE and EPS for at least the past three years and renewed for the year of the Award.

A minimum of 3 endorsements is requested. (Endorsers do not need to be current EPS members).

Electronics Manufacturing Technology Award: To recognize major contributions to Electronic Manufacturing Technology in fields encompassed by the EP Society.

Prize: \$3,000 and Certificate

Basis for Judging: Contributions may include technical development of, or management (directing) of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes, etc. Contributions must be sustained and continuing over a period of at least 15 and preferably 20 years. Work in the management of EPS Conferences or its BoG may be contributory, but it is not a requirement for the award.

Eligibility: Membership in IEEE or the EPS is not required.

A minimum of 3 endorsements is requested. (Endorsers do not need to be current EPS members)

William Chen Distinguished Service Award: To recognize and honor outstanding service and leadership to the Electronics Packaging Society and its sponsored activities.

Prize: \$5,000 and Certificate

Basis for Judging: Recipient is required to have made outstanding contributions to expanding the Society's impact in the electronic packaging field and profession through service and leadership within the EPS organization, including activities at the Chapter, Regional or BoG level or through the society's primary conferences and workshops. Examples would include serving as a conference chair, society officer, regional director, etc.

Eligibility: At the time of nomination, the nominee must have been continuously a member for the previous ten (10) years of IEEE and EPS with respect to the year of presentation of the award, and have already renewed the membership for the year of presentation of the award.

A minimum of 3 endorsements is requested. (Endorsers do not need to be current EPS members)

Exceptional Technical Achievement Award: To recognize an individual, or group of individuals (no more than three), for exceptional technical achievement in the fields encompassed by the EP Society.

Prize: \$2,500 and a Certificate.

Basis for Judging: Technical contributions of the nominee(s) must be such that they are considered to be exceptional, not achieved by most members. A single major contribution will qualify for this award. The contribution could be a significant invention, introduction of a significantly new and important technology or product (in which case, the nominee may be a team leader), or significant work that advances the state-of-the-art in EPS's field of interest. The technical contributions must be documented by open literature publications such as papers, patents, books, and reports (available to the public). Technical recognition and awards from the organization employing the individual as well as awards from other IEEE and non-IEEE technical societies may also be contributory.

Eligibility: Recipient(s) must have been a member of IEEE and EPS for at least the past three years and renewed for the year of the Award.

A minimum of 3 endorsements is requested. (Endorsers do not need to be current EPS members)

Outstanding Young Engineer Award: To recognize outstanding contributions to the fields encompassed by the EP Society through invention, technical development, publications, or new product implementation.

Prize: \$1,500 and Certificate

Basis for Judging: Technical contributions through patent invention, contributions to technology or product development within the EPS Field of Interest. May encompass management (directing) of significant new product introduction or implementation of major new electronic manufacturing processes; significantly increasing yield and/or reliability of

established manufacturing processes. Contributions to the Society, through the BoG, Conferences, Chapters, etc., will also be considered. Proof of contributions may consist of open literature publications (preferred) such as papers, patents, books, and reports (available to the public). At least three (3) letters from peers and management at the nominee's place of employment attesting to the accomplishment(s) can be accepted in lieu of publications.

Eligibility: Recipient must be a current member of IEEE and EPS, and have been a member of IEEE and EPS for at least the past three years and renewed for the year of the Award. Recipient must be less than 35 years of age on 31 December of the year before the award year.

A minimum of 2 endorsements is requested (Endorsers do not need to be current EPS members)

Regional Contributions Award: To recognize significant and outstanding leadership and contributions to the growth and impact of EPS programs and activities at the Region level. Maximum of one award annually from each Region/ Groups of Regions (3 awards): Regions 1-7 & 9; Region 8; and Region 10.

Basis for Judging: Demonstrated service and leadership in areas that may include but are not limited to Chapter activities, Conference/Workshop activities, Membership Development, Student Programs and Technical Activities. The respective EPS Regional Advisory Committees will receive nominations, evaluate candidates, select a candidate(s), and present candidate(s) to EPS Awards Committee for review and approval.

Eligibility: Recipient has been a member of IEEE and EPS for at least the past three years and renewed for the year of the Award. Self-nominations will not be accepted.

Guidelines for Nominators:

- A recipient of any EPS Major Award will be eligible for nomination for another EPS Major Award *after two award cycles have passed*. (i.e., Recipient of XX Award in 2021 becomes eligible for nomination for YY Award in 2024). For lists of past awardees, see <http://eps.ieee.org/awards.html>
- Past recipients of an award are not eligible to receive that same award. For lists of past awardees, see <http://eps.ieee.org/awards.html>
- An individual may submit only one nomination per award but may submit nominations for more than one award.
- An individual may submit only one endorsement per award but may submit endorsement for more than one award.
- It is the responsibility of the nominator to ensure quality documentation to assist the Awards Committee in evaluating the candidate.
- Outstanding Sustained Technical Contribution Award is designed for the "practitioner", while the Electronics Manufacturing Technology Award intended for "Corporate Leadership".
- Complimentary material, such as candidate's picture, CV, list of publications and/or patents should be submitted separate from the award nomination.
- Self-nominations **will not** be considered.

EPS PhD Fellowship:

To promote, recognize, and support PhD level study and research within the Electronics Packaging Society's field of interest.

Prize: A certificate and a single annual award of US\$5,000, applicable towards the student's research.

Basis for Judging: Demonstration of his/her significant ability to perform independent research in the fields of electronic packaging and a proven history of academic excellence, as documented in:

- Nomination by an IEEE EPS Member. Only one nomination per member per year.
- Two-page (maximum) statement by the student describing his or her education and
- Research interests, accomplishments, and impact on the electronics package industry.
- Proof of contributions to the community may consist of open literature publications (preferred) such as papers, patents, books, and conference presentations and reports (available to the public).
- At least one letter of recommendation from someone familiar with the student's work
- Student resume

Eligibility: Candidate must be an IEEE EPS member, at the time of nomination, and be pursuing a doctorate degree within the EPS field of interest on a full-time basis from an accredited graduate school or institution. The candidate must have studied with her/his advisor for at least 1 year, at the time of nomination, to be eligible. A Student who received a Fellowship award from another IEEE Society, within the same year, or is a previous EPS Fellowship winner is ineligible.

All Award nominations must be **online**. Nominations questions can be sent to the Society Awards Program director:

*Patrick McCluskey
mcclupa@umd.edu*

Winners will be notified by April 2024, and the awards will be presented at the 74th Electronic Components and Technology Conference (ECTC) at the Gaylord Rockies Resort in Denver, CO.

MEMBERSHIP NEWS



Society Member Digital Library

The Digital Library allows members to view and download a wide selection of journals and conference proceedings.

Members have unlimited access to the full archive of EPS sponsored Transactions, journals, and conference proceedings via Xplore. This includes current and prior editions to the early nineties of more than 15 Transactions and journals and 35 conferences, including the ECTC, EPTC, ESTC, iTHERM and more.

IEEE Senior Membership: Are You In?

If you have been involved in the electronics packaging field for 10 years or more, chances are that you probably already have the necessary qualifications to be an IEEE Senior Member.

Senior membership is the highest IEEE membership grade that can be applied for and is a recognition of sustained and significant performance in an IEEE-designated field. Individuals who are IEEE members can apply themselves for elevation to Senior Member or they can be nominated by others. Since a member can be nominated by someone else for Senior Membership, Society Chapters can play an important role in helping to identify and support applications for elevation. Nominating individuals in our Chapters is a great way to recognize their professional achievements and

foster deeper personal and professional relationships with our peers. Individual members shouldn't hesitate to apply for Senior Member elevation on their own as well and call upon their IEEE colleagues for support for their application. The requirements for Senior Member eligibility are very straightforward:

- The candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE-designated fields
- Candidates shall have been in professional practice for at least ten years
- Candidates shall have shown significant performance over a period of at least five of those years

As a member of EPS, the IEEE-designated field criteria will generally have been met. The criteria for ten years of professional practice can also take into account some portion of your

educational experience as well as time spent in one's job or career, so a ten-year employment record isn't necessarily required. The final criteria of demonstrating significant performance over at least five of those ten years can be met in many different ways, including technical work, managerial responsibility, and publications to name a few. IEEE provides detailed information on the requirements for Senior Member grade at <https://www.ieee.org/membership/senior/senior-requirements.html>, along with sample cases that can be helpful for comparison to your own professional experiences.

Individuals applying for or nominating someone for Senior Member elevation can find additional information on the IEEE website at <https://www.ieee.org/membership/grade-elevation.html> and clicking on the Senior Member Grade link found there. Candidates applying for Senior Membership will need to supply three references from current IEEE members who are Fellows, Senior

Members, or Honorary Members, and this is where EPS colleagues can support one another. Members of EPS chapters already have a group of local contacts that can help with nomination and reference support, simplifying and streamlining the process. Prospective applicants can find potential references through IEEE Collabratec via a link at the top of the EPS Membership page. There is also a link to the general Collabratec page on the [MGA Senior Member Requirements page](#).

IEEE Senior Membership is a way for the Society to recognize the dedication and achievements of our members as well as a way to support our colleagues. If you have any questions about the Senior Membership application process or requirements, please don't hesitate to reach out to your local chapter or to us here at EPS for assistance.

Thanks

Alan Huffman, EPS VP Membership

PUBLICATIONS NEWS

2022 CPMT Best Transactions Paper Awards

Each year, the Editors of the IEEE Transactions on Components, Packaging and Manufacturing Technology select the best papers published in the prior year. The papers are selected from among over 200 published papers and represent the best, based on criteria including originality, significance, completeness and organization.

Subscribers to this publication can access the papers on-line in IEEE Xplore at: <http://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=5503870>

Electrical Performance Category

“Fast and Stable Circuit Simulation via Interpolation- Supported Numerical Inversion of the Laplace Transform” Emad Gad; Ye Tao; Michel Nakhla; Volume. 12, Issue 1, January 2022

Abstract:

The modified numerical inversion of the Laplace transform (dubbed NILT) has been recently proposed as a fast and provably stable numerical simulation for general circuits. Although it has enabled increasing the simulation time step, it highlighted the need for robust approach that can recover the full waveform in between the time points generated by NILT. This article presents a new approach that addresses this challenge. The proposed approach leverages the NILT framework from a high-order approximation paradigm that computes points on the circuit waveforms to a methodology that computes high-order derivatives of the waveforms at the same points. Using those derivatives, an interpolation approach based on Hermite interpolation is used to construct the circuit waveforms on dense points. Numerical experiments are presented to demonstrate the accuracy of both approaches.

URL: <https://ieeexplore.ieee.org/document/9585596>

Components: Characterization and Modeling Category

“A Mechanistic Model for Plastic Metal Line Ratcheting Induced BEOL Cracks in Molded Packages” Chun-Pei Chen; Yaxiong Chen; Ganesh Subbarayan; Hung-Yun Lin; Siva Gurrum, Volume. 12, Issue 3, March 2022

Abstract:

Metal line ratcheting and passivation cracking in back-end-of-line (BEOL) structures are significant reliability concerns for molded packages that are in widespread use at the present time. When metal lines plastically deform due to ratcheting, the passivation overcoat accumulates stress at the corner upon temperature cycling and is eventually susceptible to fracture. Since packaging materials' interaction with the die is the cause of the failure, the problem is inherently multiscale in nature requiring the analysis model to span from package dimension



Left to right - Chun-Pei Chen, Kitty Pearsall, Yaxiong Chen, Ganesh Subbarayan.



Best Paper Award Recipient Emad Gad with Kitty Pearsall.

to BEOL length scale. In this article, the mechanistic cause for stress accumulation is elucidated. Furthermore, a global–local modeling strategy is applied to model the passivation crack initiation and growth. A global model with coarse mesh was built of the package. The local region around the interconnect

metal line in the die was modeled using boundary conditions extracted from the global model. A novel load decomposition technique is developed to identify the loading mode that best correlates with the experimentally observed fracture. It is shown that shear is the dominant loading mode inducing the observed die cracks. Furthermore, it is demonstrated that the thermal expansion mismatch between the mold compound and the lead frame with the silicon die induces the shear load on the BEOL structure. Due to the fact that mold compound is applied at a temperature that is higher than that seen during thermal cycling, the direction of the induced shear load is constant regardless of whether the package is heated or cooled. As the metal line plastically yields during every temperature cycle, the plastic deformation ratchets or accumulates in the same direction over the course of the thermal cycling test. The yielding of metal line results in stiffness reduction, leading to steady accumulation of stress in the passivation corner, causing it to fracture eventually.

URL: <https://ieeexplore.ieee.org/document/9706464>

Best Associate Editor Award

To recognize the work and efforts of our Associate Editors, EPS instituted the Best Associate Editor Award. The 2023 recipients are:

- Karlheinz Bock, TU Dresden—IAVT, Germany**
- Xuejun Fan, Lamar University—USA**
- Patrick Fay, University of Notre Dame—USA**
- Luu Nguyen, PsiQuantum—USA**
- Suresh Sitaraman, Georgia Institute of Technology—USA**



Left to right - Xuejun Fan, Luu Nguyen and Suresh Sitaraman (proxy pictured) with Kitty Pearsall.



Best Associate Editor Award recipient Karlheinz Bock with Kitty Pearsall.

Become a Reviewer for the IEEE Transactions on Components, Packaging and Manufacturing Technology (T-CPMT)

Contribute to the research in your field by becoming an IEEE peer reviewer. Peer reviewers fulfill a vital role in the publishing process by giving detailed and professional commentary.

T-CPMT Associate Editors select potential peer reviewers who are experts in the topics that are covered in the article submission. After identifying reviewers, the system will send out invitations. Most invitations will include information about the article, such as the title and abstract, to help the reviewer decide if they should accept the invitation.

Selection Criteria:

- Minimum of bachelor's or master's degree in Material Science, Electrical Engineering, Mechanical Engineering or any related inter disciplinary field.
- Notable Publications in the field of expertise.
- Considerable Industry or academia experience.

Please submit your latest resume [here](#).

Once you submit your resume the selection committee will review your application and get back to you.

Receiving a peer review invitation

When you receive a review invitation, you should consider whether you have sufficient expertise in the article's subject area. You should also consider if you can complete the review by the deadline provided in the review invitation.

- If the answer to either of those questions is “no,” you should promptly decline the invitation. Suggestions of other potential reviewers are always appreciated.
- If you decide to accept the invitation, follow the instructions in the email to signal your acceptance. You will then receive information on how to access the article and conduct your review.

Submitting feedback and Timeline

T-CPMT uses an online submission system to facilitate peer review. Once you have accepted the review invitation, you will be given access to the article. You should evaluate the article with the following questions in mind:

- Is the study well designed and well executed?
- Is the existing body of relevant work acknowledged?
- Are the results interpreted and reported correctly? Have all other possible interpretations been duly considered?
- Are the results overly preliminary or speculative?
- Does the research contribute to the body of scientific knowledge in the field?
- Is the article appropriate for this publication?
- Is the article written in clear, concise language?

Follow the publication's instructions for submitting feedback, suggestions, and a recommended decision. Remember that your commentary should always be thorough and professional.

Timeline for T-CPMT Journal:

- a. AE/GE assigns reviewers: 5 Days
- b. Reviews back: 14 Days
- c. AE/GE + SAE make a decision: 7 Days

Most Popular Articles according to Xplore® usage statistics

In-Line Vector Modulator Integration in Dielectric-Filled Waveguide

Jaakko Haarla; Juha Ala-Laurinaho; Markku Lahti; Mikko Varonen; Mikko Kantanen; Jan Holmberg; Ville Viikari
Publication Year: 2023, Page(s):153–160

Recent Advances and Trends in Advanced Packaging

John H. Lau
Publication Year: 2022, Page(s):228–252

Recent Advances and Trends in Cu–Cu Hybrid Bonding

John H. Lau
Publication Year: 2023, Page(s):399–425

Universal Chiplet Interconnect Express (UCIe): An Open Industry Standard for Innovations With Chiplets at Package Level

Debendra Das Sharma; Gerald Pasdast; Zhiguo Qian; Kemal Aygun
Publication Year: 2022, Page(s):1423–1431

Recent Advances and Trends in Multiple System and Heterogeneous Integration With TSV Interposers

John H. Lau
Publication Year: 2023, Page(s):3–25

President's Column (Continued from page 1)

- The HIR Roadmap (3rd edition) continues to set the strategic direction for the electronic component industry through many HIR seminars, workshops, and presentations throughout the year. This is just a snapshot of our Society accomplishments, and these could not have been made without you! I want to express my sincere gratitude to all EPS Board of Governors, EPS volunteers,

and the EPS staff for their outstanding efforts in support of our mission. It is through your enthusiasm, tireless efforts, unfaltering commitment, and contribution to the EPS mission that keep us well positioned to serve the electronic packaging community.

Kitty Pearsall

EDUCATION/CAREER NEWS

EPS Distinguished Lecturer Program

EPS Distinguished Lecturers are selected from among EPS Fellows, Award winners, and Society leaders, who are members of the technical community and experts in their field. They are available to present lectures and/or courses at EPS events—Chapters, Conferences, Workshops or Symposia, as well as IEEE Student Chapter events.

The EPS Distinguished Lecturer Program (DLP) aims at serving communities interested in the scientific, engineering, and production aspects of materials, component parts, modules, hybrids and micro-electronic systems for all electronic applications.

The Program strives to support EPS Chapters worldwide by helping them to invite leading researchers in their respective fields and IEEE Student Chapters to encourage students to pursue EPS related fields and to join the EPS society. The DLP talk is a major event in the life of the inviting Chapter.

EPS Distinguished Lecturers

Ramachandra Achar (7/1/2020–6/30/2024)

Department of Electronics, Carleton University
Ottawa, Ontario, CANADA

Topics: CAD tools and methodologies for interconnects, packages, and systems with an emphasis on signal, power and EMI integrity

Mudasir Ahmad (1/2022–12/2025)

Google
CA, USA

Topics: Internet of Things (IoT), Advanced Packaging, 2.5D, Heterogeneous Silicon Photonics, Advanced Reliability (Thermo-mechanical, Mechanical Shock), Numerical Modeling, Advanced Thermal Solutions, Stochastic Analysis, Bayesian Inference, Machine Learning, Artificial Intelligence

Kemal Aygün, Ph.D. (7/1/2020–6/30/2024)

Intel Corporation
Chandler, AZ USA

Topics: Package/socket/board/interconnect technologies, electrical simulation methodology and lab metrologies

Muhannad Bakir, Ph.D. (1/2020–1/2024)

School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, GA USA

Topics: Emerging interconnection architectures and technologies; heterogeneous system design and integration

W. Dale Becker, Ph.D. (7/1/2020–6/30/2024)

Retired
Hyde Park, NY USA

Topics: Electronic Package design and integration, system design, electrical modeling tools

Wendem Beyene, Ph.D. (7/1/2020–6/30/2024)

Meta
San Jose, CA

Topics: Electrical modeling and simulation techniques for analysis of interconnects, packages, and systems. Machine learning techniques

Karlheinz Bock, Ph.D. (7/2020–7/2024)

Technische Universität Dresden
Dresden, Germany

Topics: Multifunctionality & heterosystemintegration & additive manufacturing (IoT, Industry 4.0, tactile internet), packaging for mechanical, digital and power co-integration (automotive, machines, robots.), 2.5D and 3D electro-optical-RF interposer and board (high performance), heterointegration for flexible, bio, organic and large area electronics (open form factor)

Bill Bottoms, Ph.D. (6/2021–6/2025)

Third Millennium Test Solutions
Santa Clara, CA USA

Topics: Heterogeneous Integration, Semiconductor test technology, Emerging research materials, Packaging of electronic components and systems, the global network and its future requirements, the internet of things and Smart manufacturing

Chris Bower, Ph.D. (6/2021–6/2025)

X-Celeprint Inc.
North Carolina, USA

Topics: novel assembly methods, elastomer stamp micro-transfer-printing, heterogeneous integration, three-dimensional integration, manufacturing of micro-assembled displays and other large-format electronics.

William T. Chen, Ph.D. (1/2020–1/2024)

ASE (U.S.) INC
Santa Clara, CA USA

Topics: Semiconductor and Electronics Industry Trends and Roadmap

Xuejun Fan, Ph.D. (1/2020–1/2024)

Lamar University
Beaumont, TX USA

Topics: Design, modeling and reliability in micro-/nano-electronic packaging and microsystems

Madhu Iyengar, Ph.D. (7/1/2020–6/30/2024)

Google
Mountain View, CA, USA

Topics: Thermal component and system design for packages, servers, and data centers.

Subu Iyer, Ph.D. (6/2021–6/2025)

University of California, Los Angeles
Los Angeles, CA USA

Topics: Heterogeneous Integration; Flexible hybrid electronics; 3D interposer, and wafer scale integration and stacking.

Beth Keser, Ph.D. (1/2020–1/2024)

Intel
San Diego, CA USA

Topics: Fan-Out Wafer Level Packaging and Wafer Level Packaging structures; processes, materials, tools, design rules and roadmaps; photoimageable liquid polymer films

Pradeep Lall, Ph.D. (1/2020–1/2024)

Auburn University
Auburn, AL USA

Topics: Semiconductor Packaging, Modeling and Simulation, Reliability in Harsh Environments, Shock/Drop/Vibration, Cu Wirebonding, Flexible Hybrid Electronics, Additive Manufacturing, Prognostics and Health Management, LEDs, Micro CT Measurements

John H. Lau, Ph.D. (1/2020–1/2024)

Unimicron Technology Corporation
Palo Alto, CA USA

Topics: Electronics and Photonics 2D and 3D packaging and manufacturing

Ravi Mahajan, Ph.D. (7/2020–7/2024)

Intel Corporation
Arizona, USA

Topics: Advanced Packaging Architectures, Assembly Processes and Thermal Management

James E. Morris, Ph.D. (1/2020–1/2024)

Department of Electrical and Computer Engineering
Portland State University
Portland, Oregon USA

Topics: Electrically conductive adhesives; Electronics packaging; Nanotechnologies

Rajen Muguran, Ph.D. (7/2022–7/2026)

Texas Instruments
Dallas, TX, USA

Topics: Multiphysics and System Co-Design modeling for complex analog and mixed-signal packaging, mmWave/THz signal integrity, power electronics packaging, and System-Level EMI/EMC modeling, analysis, and characterization.

Eric D. Perfecto (1/2020–1/2024)

IBM Research
Poughkeepsie, NY USA

Topics: Fine pitch interconnect, chip to chip and chip to laminate connection, UBM and solder selection, chip package interaction and 2.5D fabrication

Mark Poliks, Ph.D. (1/2020–1/2024)

Binghamton University (SUNY)
Binghamton, NY USA

Topics: Materials and Processes, Advanced Manufacturing, Flexible Hybrid Electronics, High Speed and Additive

Gamal Refai-Ahmed, Ph.D. (7/1/2022–6/30/2026)

Xilinx
San Jose, CA USA

Topics: Thermo-mechanical Semiconductor and Electronics Industry Roadmap and directions, Advanced holistic Thermo-mechanical solution, assembly and reliability of Heterogeneous Packaging and Silicon Photonics, Future thermo-mechanical technology, architecture for component and system

Jose Schutt-Aine, Ph.D. (1/2020–1/2024)

University of Illinois
Champaign, IL, USA

Topics: High-Frequency Measurements, Mixed-Signal Design, High-Performance Computing, electromagnetic Modeling, Signal Integrity, CAD Tools for Interconnects and Packages, Machine Learning for High-Speed System Modeling

Dongkai Shangguan, Ph.D. (7/1/2023–6/30/2027)

Thermal Engineering Associates, Inc.
San Jose, CA, USA

Topics: Heterogeneous Integration and SiP; Electronics Packaging and Miniaturization; Materials; Thermal management; Reliability; Electronics manufacturing technology; Flexible hybrid electronics

Rohit Sharma, Ph.D. (1/2023–1/2027)

Indian Institute of Technology Ropar
Punjab, India

Topics: Design of High-speed Graphene-based and 2D materials-based nanoelectronics; Electrical-Thermal co-design of electronic packages and microsystems; Application of Machine Learning in design and analysis of interconnects; Heterogeneous integration.

Nihal Sinnadurai (1/2020–1/2024)

Suffolk IP11 9RZ UK

Topics: Accelerated Ageing for Reliability Assurance -theory and practical methods—including HAST (my invention originally); The use of encapsulation and plastic packaging and reliability evaluation method; PCB & Hybrid technologies; Thermal management and design

Ephraim Suhir, Ph.D. (1/2020–1/2024)

Los Altos, CA 94024 USA

Topics: Accelerated life testing; Probabilistic physical design for reliability; Bonded assemblies; Thermal stress; Predictive modeling; Fiber optics structures: design for reliability; Dynamic response to shocks and vibrations

Andrew Tay, Ph.D. (1/2023–1/2027)

SHINE Center, National University of Singapore
Singapore

Topics: Thermomechanical reliability of microelectronics packages; Thermal and failure analysis of microelectronic devices; Thermal management of electronic and EV battery systems; Solder joint reliability; Delamination and fracture; Moisture effects; Modelling and simulation.

Manos Tentzeris, Ph.D. (7/2023–6/2027)

Georgia Institute of Technology
Atlanta, GA USA

Topics: RF/mmW/3D/electronics industry/nanotechnology/materials/packaging/3D printing/energy harvesting-zero power

Rao Tummala, Ph.D. (1/2020–1/2024)
Microsystems Packaging Research Center (PRC)
Georgia Institute of Technology
Atlanta, GA USA
Topics: Electronics Packaging

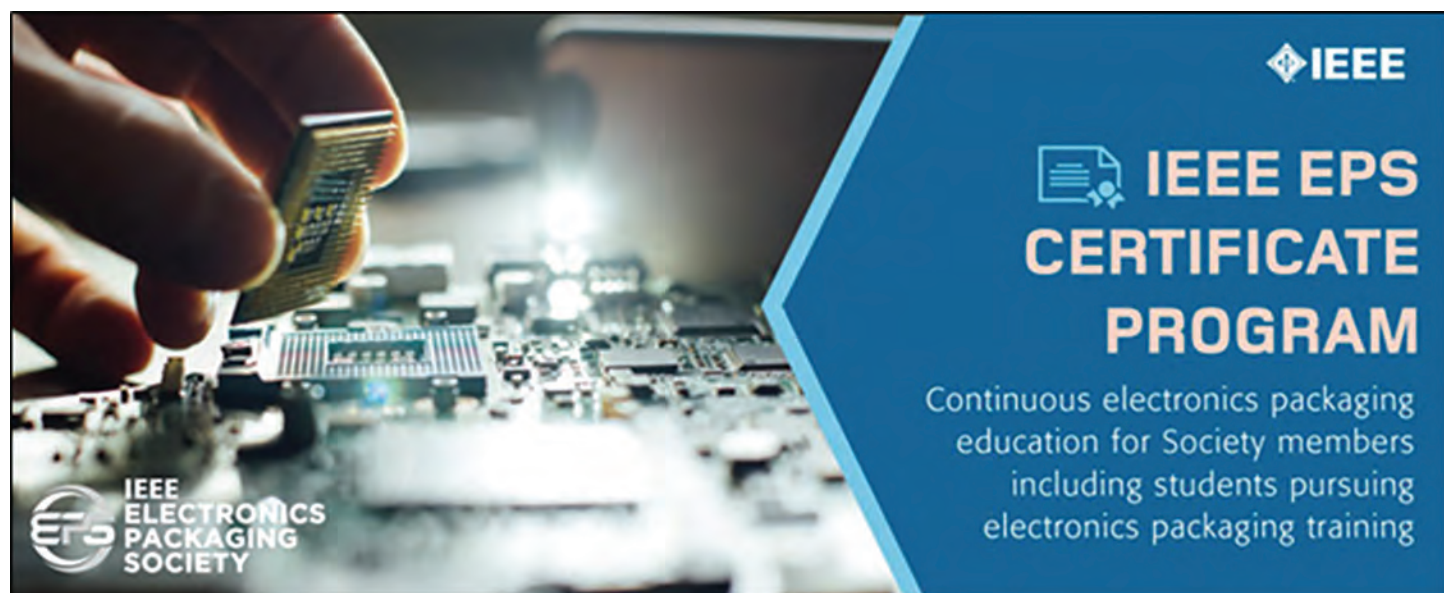
E. Jan Vardaman (1/2020–1/2024)
TechSearch International, Inc.
Austin, TX USA
Topics: International developments in semiconductor packaging, manufacturing and assembly; SiP: Business and technology Trends; drivers in advanced packaging; Flip chip and wafer level packaging

Paul Wesling (1/2020–1/2024)
Saratoga, CA USA

Topics: Origins of Silicon Valley and the Electronics Packaging Society; the IEEE/SEMI/ASME Heterogeneous Integration Roadmap and how to use it (as editor for the 2019 Roadmap).

C.P. Wong, Ph.D. (1/2020–1/2024)
Georgia Institute of Technology
Atlanta, GA, USA
Topics: Materials

Jie Xue, Ph.D. (1/2020–1/2024)
Cisco Systems, Inc
San Jose, CA, USA
Topics: Advanced Packaging for Networking Application; Impact of Internet of Everything (IoE) to Semiconductor Industry eco-system; High performance substrate technologies; Trends and challenges of Silicon Photonics for datacenter and networking applications



EPS Certificate Program

The IEEE Electronics Packaging Society Certificate Program provides a pathway for early and mid to late-career professionals to highlight their accomplishments.

Criteria for all Certificates: Must be an IEEE Electronics Packaging Society Member.

There are three Certificates you may apply for, which are noted below.

EPS Achievement Certificate

The first level *EPS Achievement Certificate* is aimed at early-career professionals working in the field of electronics

packaging. It is especially intended to encourage the career development of young professionals including advanced graduate students.

Criteria: Current EPS Member

To receive your certificate, 15 professional development hours (PDHs) must be completed. This can be obtained from a combination of the following:

- 1) IEEE EPS Webinar (1 PDH) – must complete **PDH evaluation**.
- 2) Professional Development Courses – must complete survey and CEU credit form. Previous ECTC PDCs from the last 10 years can be used towards this if the CEU application was completed at the time of the course. PDCs from ESTC and EPTC 2018 and forward can be used.



- Electronic Components and Technology Conference (USA) = 4 PDHs
 - Electronic Systems-Integration Technology Conference (Europe) = 3 PDHs
 - Electronic Packaging Technology Conference (Asia) = 4 PDHs
- 3) Author of IEEE T-CPMT and/or EPS conference paper(s) (5 PDHs) – paper must be published in IEEE Xplore within the last 5 years.
- 4) Reviewer for IEEE T-CPMT (3 Reviews = 5 PDH) within the last 5 years.

Once you have completed any combination of the above and received 15 PDHs, please complete the certificate form to request your Electronics Packaging Society Certificate of Achievement.

IEEE Distinguished Achievement Certificate for Technical Leadership and Expertise

Criteria: Must be a current EPS member

There are five high-level focus areas for this new certificate. These areas include:

- 1) Being a recognized authority of technical expertise in electronics packaging.
Examples include being an advanced member of the technical staff at a company (e.g. Fellow, Senior Technical Staff, Distinguished Engineer, etc.), making technical contributions as a Member or Fellow of professional associations/societies related to electronics packaging (e.g., IEEE, IMAPs, SMTA, ASME, etc.), and being an invited speaker at companies, technical conferences, and EPS Chapter meetings.
- 2) Being a subject matter expert (SME) in electronics packaging at conferences, keynotes, webinars, blogs, etc.

Methods to demonstrate participation as a SME include abstracts accepted and papers presented at conferences, giving keynote lectures at conferences or professional society meetings, presenting webinars for EPS and other IEEE Societies, and serving on technical panels at conferences and other venues.

- 3) Demonstrating sustained technical contributions to the electronics packaging industry.

Examples of sustained technical contributions include publishing well-cited technical papers at conferences and in journals, book chapters, and patents; serving as an editor of a journal or reference book; and being a leader or participant in industry blogs, focus groups, technical roadmaps, newsletters, and forums.

- 4) Documenting advanced technical recognitions in electronics packaging.

Methods to document technical recognitions include receiving technical awards from a company, institute, professional society, or academic institution; being the acknowledged inventor of a seminal technology or process important to industry; serving as the point person for global high-level task force activity; and being elected to be a Member of an organization such as the US National Academy of Engineering, Royal Academy of Engineering, Chinese Academy of Engineering, IBM Academy of Technology, etc.

- 5) Provide at least one endorsement letter.

Nominations for the Distinguished Achievement Certificates will be accepted two times per year: Jan 1–June 30 and Aug 30–Oct 31.

IEEE Distinguished Achievement Certificate for Professional Engagement and Service

Criteria: Must be a current EPS member

There are four high-level areas of focus for this new certificate. These areas include:

- 1) Demonstrating leadership in the electronics packaging field.
Leadership and broad impact activities in electronics packaging can be documented from outstanding accomplishments during industry employment or for notable volunteer contributions to the profession and society.
- 2) Illustrating broad impact/influence in the electronics packaging field.

Examples of significant professional service include serving as an officer in a technical society at the international, national, or local chapter level; participating in packaging related technical



committees, councils, or affinity groups; contributing to technology roadmaps such as the Heterogeneous Integration Roadmap (HIR); and receiving a professional society or industry award based on service contributions.

3) Providing extensive service and “give back” to the profession and/or industry; and

Documentation of “give-back” to one’s technical community can be accomplished via demonstrations of coaching and mentoring of co-workers, young professionals, and students.

4) Provide at least one endorsement letter.

Nominations for the Distinguished Achievement Certificates will be accepted two times per year: Jan 1–June 30 and Aug 30–Oct 31.

More details on the Certificate Program are available on the EPS website at <https://eps.ieee.org/education/eps-certificate-program.html>. The EPS Certificate Program is sponsored by the IEEE EPS VP Education and is offered only to EPS members. For questions, please contact Eric Perfecto (eperfecto@gmail.com).

EPS Achievement Certificate

Congratulations to the EPS Member on receiving the IEEE Achievement Certificate from the IEEE Electronics Packaging Society and completing the required number of professional development hours.

Dr. Kaustubh Basu, TASK Microelectronics

EPS Resource Center

The IEEE EPS Resource Centers contains valuable, technical content from reputable experts to enhance research or industry work, implement trainings, or earn CEU/PDH credits--all of which are universally available on demand.

IEEE EPS Resource Centers benefits include:

- Access to valuable technical community content
- Access to content 24 hours a day, 7 days a week through an easy-to-use global portal

- Available at no cost for EPS members
- Opportunities to earn CEUs and PDHs

Top webinars:

- Chiplet Design and Heterogeneous Integration Packing
- Powering Heterogeneous Integration: An overview of the Integrated Power Electronics Chapter of the HIR Roadmap
- The Evolution of Lead-Free Solder Alloy
- Recent Advances and Trends in Advanced Packaging
- Thermal Management Challenges and Opportunities for Heterogeneous Packages

<https://resourcecenter.eps.ieee.org/>

CONFERENCE NEWS

The 73rd ECTC Conference.

Submitted by Przemyslaw Gromala, Assistant Program Chair, IEEE EPS ECTC 2024

This year's IEEE EPS Electronic Components and Technology Conference (ECTC) took place in Orlando, Florida, at the newly renovated JW Marriott Orlando, Grande Lakes hotel, from May 30 to June 2, 2023. The conference brought together a total of 1,619 industry professionals, academics, and students in attendance from 26 countries.

The 73rd ECTC included 369 technical presentations, which were organized into 36 oral sessions and five interactive presentation (IP) sessions. There were 10 special sessions including two panels, one plenary session and a keynote opening the conference. The 13 professional development courses (PDCs) were attended by 325 attendees. The conference had 118 exhibitors at the Technology Corner Exhibit, a tribute to the quality of the conference and its attendees. The conference benefited from a strong number of sponsors and sponsorship, further testament to the value delivered by this flagship IEEE EPS conference.

Preparations for the 73rd ECTC conference began on 3–4 November 2022 in Dallas, where the ECTC Executive Committee and representatives of 10 technical sub-committees met and decided about the conference sessions based on 618 abstracts received, of which 335 were from first-time ECTC authors. In the end, 60% of the submissions were accepted. 56% of the submitted abstracts were from industry, and 44% were from academia and research institutions. In a testimony to the diversity of the industry and the conference, abstracts were received from 26 countries with the United States, Taiwan, China and South Korea leading the way in number of abstract submissions.

Based on the feedback from the participants of the 72nd ECTC and lively discussion during the preparation meeting in Dallas a series of novelties were introduced in this year's ECTC program:

- We have introduced a two-stage submission process to allow reviewers to streamline the peer-review process.



- Accommodation of the larger rooms with the full-time AV support at the conference.
- A full program of special sessions on Tuesday.
- On Wednesday morning at 8 am, we had for the first time, a plenary session with our ECTC 2023 keynote speaker.
- Six parallel technical sessions followed at 9:30 am. Technical presentations were shortened to 20 minutes including Q&A.
- Other plenary sessions were organized at 8 am on Thursday with our EPS Seminar, and on Friday with EPS President's Panel session.
- Breaks between technical sessions were extended to give all ECTC participants more opportunities for networking.

73rd ECTC conference kicked off on Tuesday, May 30, 2023. Each day at ECTC begins with the Speakers Breakfast in which the presenters and session chairs meet and take care of the preparatory work for their respective sessions. The PDC Chair, Kitty Pearsall, provided instructions to the PDC instructors and proctors on Tuesday morning, and Florian Herrault, the Program Chair, hosted these breakfast meetings on Wednesday till Friday.

As usual, the first day of the conference, the Tuesday following Memorial Day, featured PDCs, a workshop related to heterogeneous integration roadmap (HIR) and a variety of special sessions. This year, the conference had seven morning PDCs, running from 8 a.m. to noon, and another six afternoon PDCs, running from 1:30 to 5:30 p.m. The total number of PDC attendees was 325. The courses continued to serve a convenient way for students



and engineers to quickly get “up to speed” on the current topics of importance in electronics packaging. A total of two PDCs were new.

On Tuesday morning, parallel to the PDC we had an opportunity to contribute to the IEEE EPS Heterogeneous Integration Roadmap (HIR) special workshop chaired by William Chen, Bill Bottoms and Ravi Mahajan. The workshop started at 8:00 am and lasted until 4:30 pm. Session has been divided into four topics: AI/ML in package Co-Design for Chiplets Perspective; Heterogeneous Integration of MEMS & Sensors – Challenges and Opportunities; The Chips and Science Act; and Additively Manufactured Electronics for Heterogeneous Integration.

Similarly, as during the 72nd ECTC in San Diego, on Tuesday there were four special sessions 90 mins long, a networking panel for young professionals, and an IEEE EPS seminar. In the morning, from 8:30 to 10:00 am, Tanja Braun - Fraunhofer IZM and Przemyslaw Gromala - Robert Bosch GmbH, held a special session on Advanced Packaging and HIR for Harsh Environments - Current Status and Opportunities, with seven invited panelists from GM, Bosch, Samsung, ASE, Amkor, Henkel and Georgia Tech, covering the entire supply chain. Attendees were offered an overview of why SW-defined vehicles and highly automated driving require consumer-inspired electronics, such as CPUs and GPUs, and the challenges of qualifying these electronic components for harsh environments.

Next, at 10:30 am to 12:00 pm, Jan Vardaman – TechSearch International, Thomas Gregorich – Infinera and Chaoqi Zhang – Qualcomm, led a session Copper Hybrid Bond Interconnections for Chip-to-Wafer Applications. Presenters from IMEC, Intel, Synopsis, AMD, EVG and BeSi discussed the challenges and solutions for the expanded use of C2W copper hyper bonds. The topic of the panel interested so many conference participants that many of them stood and listened to the discussion at the door of the auditorium.



After lunch, there was another emerging topic that brings every year more contributions and interests at the ECTC Conference. Stephane Bernabe – CEA LETI, and Hiren Thacker – Cisco, organized a special session entitled: Photonic Integrated Circuit Packaging: Challenges, Pathfinding, and Technology Adoption. Six leading practitioners from industry and academia – CEA Leti, Teramont, IBM, Tyndall National Institute and FiconTEC Service GmbH – discussed the greatest challenge for photonic integrated circuit (PIC) – packaging technologies to reach high volume manufacturing and high throughput and yield.

CHIPS Act is an important milestone to strengthen the US manufacturing of electronics packaging in North America. Nancy Stoffel – GE Research, Jan Vardaman – TechSearch International and William Chen - ASE, invited speakers from industry: Marvel, Promex Industries, Micron; academia: University of California; and funding agencies: NIST, DARPA to discuss how to revitalize manufacturing of advanced packaging in North America. Participants had a chance to review the targets and developing plans of the US government, funded through the Chips Act.

The ECTC Student Reception, sponsored by Texas Instruments, was traditionally held on Tuesday from 5:00 to 6:00 pm. A steady stream of student attendees took advantage of the opportunity to mingle and network with professionals in the field. Right after this, the General Chair’s Speakers Reception was given from 6:00 to 7:00 pm for Speakers and Session Chairs. These receptions provided a great start to the conference and helped prepare everyone for the following three days filled with technical presentations and networking opportunities. The Young Professionals Networking Panel and Reception took place from 7:00 to 7:45 pm and was chaired by Yan Liu – Medtronic. The IEEE EPS board members were present to discuss with attendees about various ways to develop their professional network and career paths.



The Tuesday program ended with a room full of attendees for the IEEE EPS Seminar on High Density Substrates from 7:45 to 9:15 pm, chaired by Takashi Hisada – IBM, and Yasumitsu Orii – Rapidus. Panelists were invited from Shinko, Unimicron, Dai



Nippon Printing, Penn State University and IBM. ECTC participants had a chance to learn about ultra-fine-pitch substrate technologies for chiplets and heterogeneous integration, trends, challenges, requirements, and latest technical achievements.

On Wednesday, we started the conference day with the Keynote presentation. Ibrahim Guven – Virginia Commonwealth University and ECTC 2023 General Chair introduced this year’s keynote speaker Prof. Michael J. Manfra from Purdue University. The title of the keynote was: Unlocking the Potential of Quantum Computers: Challenges and Opportunities in Electronic Devices, Interconnects, and Packaging. In his keynote, Prof. Manfra emphasized that quantum computing will require advancements in new materials, innovations in interconnect and packaging technologies and novel thermal management, which are the core topics of the ECTC conference.



After the keynote, we started with the six technical sessions running in parallel throughout each of the three days. Each oral session featured seven paper presentations, and the interactive presentation sessions featured between 20 and 29 papers. Wednesday morning started with large crowds in the six sessions with titles “Heterogenous Chiplet Integration”, “High-Performance Packaging Materials”, “Advancements in Copper/Silicon-Oxide Hybrid Bonding”, “Assembly and Manufacturing Process Enhancement”, “Underfilling and Chip-Package Interaction”, and “Co-packaged Optical Assembly”. In parallel, the first



of five interactive sessions took place from 10:00 am–12:00 pm, with 20 paper presentations.

During lunch, Patrick Thomson, ECTC Finance Chair who is attending ECTC already for a 40th time, shared a magnificent 73-year history of the ECTC conference. It gave a chance to all of us to learn how the conference evolved and how large the impact of this conference is on the entire microelectronics industry. Afterwards, Awards for Best and Outstanding Papers from the 72nd ECTC 2022 and the Intel Best Student Paper Award were presented by Kitty Pearsall.



In the afternoon, high attendance in the sessions was noticeable, with the topics “Large Formfactor Dense System Integration by Fan-Out”, “Novel Reliability Test Methods”, “Innovations in Copper Chip-to-Wafer Bonding”, “Packaging Interconnections”, “Additive Manufacturing and Packaging for Flexible Electronics”, and “mm Wave Antenna-in-Package and Arrays”. In parallel to the technical session, the second interactive session took place from 2:30–4:30 pm, with 29 paper presentations. On Thursday, Interactive presentations session in the morning with 28 presentations and afternoon with 26 presentations. Last conference day, Friday, we had only a morning session with student interactive presentations having 23 presentations. Attendees of the ECTC rated all oral and interactive session paper ratings only through the ECTC mobile app “Whova”.

The Technology Corner exhibit area hosted 118 exhibitors. Exhibitors had multiple resources available within their booth, offering introductions, brochure materials, staff contact information, and an opportunity to submit inquiries and discuss directly with exhibit members their latest developments, tools, and services. In the late Wednesday’s afternoon we had a chance to meet all the exhibitors during the exhibition reception and enjoy the excellent food and atmosphere of the venue hotel.

On Wednesday evening, co-organized with iTherm, we had a Diversity and Career Growth Panel: Diversifying our Technical Workforce to meet National Needs including the CHIPS Act Initiative. The Panel was chaired by Kim Yess – Brewer Science/ECTC, Nancy Stoffel – GE Research/ECTC, and Christina Amon – University of Toronto/iTherm. Discussion included four panelists from: University of Texas Arlington, NetFlex, GE Foundation, NIST CHIPS. Panel discussed the development of initiatives,

2022 ECTC Best Paper Awards

1) Best Session Paper

Advanced Fan-Out Packaging Technology for Hybrid Substrate Integration

Lihong Cao, Teck Chong Lee; Rick Chen; Yung-Shun Chang; Hsingfu Lu; Nicholas Chao; Yen-Liang Huang; Chen-Chao Wang; Chih-Yi Huang—ASE Group

2) Best Interactive Presentation Paper

Novel Zero Side-Etch Process for <math><1\mu\text{m}</math> Package Redistribution Layers

Pratik Nimbalkar, Pragna Bhaskar, Christopher Blancher, Mohanalingam Kathaperumal, Madhavan Swaminathan, and Rao Tumala—Georgia Institute of Technology

3) Outstanding Session Paper

Organic Interposer CoWoS-R+ (plus) Technology

M. L. Lin, M. S. Liu, H. W. Chen, S. M. Chen, M. C. Yew, C. S. Chen, and Shin-Puu Jeng—Taiwan Semiconductor Manufacturing Company

4) Outstanding Interactive Presentation Paper

Scalable through Mold Interconnection Realization for Advanced Fan Out Wafer Level Packaging Applications

Aurélia Plihon, Edouard Déschaseaux, Rémi Franiatte, Jérôme Dechamp, Simon Vaudaine, Jennifer Guillaume, Catherine Brunet-Manquat, Stéphane Moreau, and Perceval Coudrain—CEA-LETI

5) Intel Best Student Session Paper

Co-Design of Thermal Management with System Architecture and Power Management for 3D Ics.

Rishav Roy, Purdue University—School of Mechanical Engineering (G077); co-authors: Shidhartha Das, Benoit Labbe, Rahul Mathur, Supreet Jeloka—ARM, Inc.



policies and programs to increase and diversify the workforce, along with the metrics to assess progress.

On Thursday from 8:00 to 9:15 am, the ECTC Plenary session on “mm-Wave Phased Array Packaging for Next-Generation Communication and Radar Systems” took place. Kevin Gu – Metawave Corporation and Ivan Ndip – Fraunhofer IZM/Brandenburg University of Technology chaired the panel. Panelists were from Teledyne Scientific, Northrop Grumman Space Systems, Penn State University, Nokia Bell Labs and IBM Research. Top researchers and industry representatives discussed the current state-of-the-art, rapidly emerging research and latest advancement in integration and packaging technologies for design and implementing phased array front-end radar modules.

Thursday’s technical morning sessions were well attended and covered the topics “Wafer/Panel-Level and Advanced Substrate Technologies”, “Advances in Heterogeneous Integration Bonding Technology”, “Innovative Interpose and Through-Via Technologies”, “Sintering and Soldering for High-Power, High-Reliability, and RF Devices”, “Advanced Reliability Modeling and Characterization”, and “Advanced Photonic Packaging and Interconnect”.

The IEEE Electronics Packaging Society President, Kitty Pearsall, presided over the luncheon on Thursday and presented the EPS Society Awards and introduced the society to new Fellow. The recipients were each presented with a certificate and warm applause from the audience.

After luncheon we continued the technical sessions including: “Advances in 3D integration and Hybrid Bonding”, “Automotive/Board-Level Reliability”, “Fine-Pitch and Intermetallic Considerations in Advanced Solder Interconnections”, “Large substrate process integration challenges”, “Next generation quantum, AI

and Secure System Design”, and “High Speed Signal and Power Integrity”.

The 73rd ECTC 2023 Technical Program Committee meeting was held on Thursday at 5:30 p.m. Michael Mayer, who will serve as the Program Chair for 74th ECTC 2024, chaired this meeting and presented the statistics of the 73rd ECTC and the timeline for the run up to the 74th ECTC that is planned to be held in Denver next year. Michel Mayer also introduced Przemyslaw Gromala of the Robert Bosch GmbH as the Assistant Program Chair of the 74th ECTC. This meeting also enabled the ECTC technical program subcommittees to get in touch with potential new members of their committees.

The traditional ECTC Gala Reception takes place on Thursday evening. It was the highlight of the week for the conference attendees, exhibitors, sponsors, and their guests. It is an excellent place for networking, meeting friends or partners, and starting new professional relationships. During the evening there was live music played on the stage. It was a fabulous time allowing celebration of the success of the ECTC by socializing and enjoying the excellent food and beverages that were supported by the Gala Reception Gold and Silver sponsors.



On the last day of the conference, President of the IEEE EPS Kitty Pearsall, together with David McCann – Lyte, chaired a panel discussion entitled “How Can Photonics Enable the Bandwidth Densities with Lower Energy per Bit in Emerging SIP”. Amr Halmy from the University of Toronto led a panel composed of invited academia and industry experts from Lightmatter, University of Southern California and AT&S. Panelists discussed the tools, technologies and approaches that will enable the industry to enhance the bandwidth density of interconnections in SiPs supported by photonics.

The Friday morning technical sessions were also well attended, covering the topics “Next Generation High-Performance Computing Architectures”, “Materials Reliability”, “Next Generation Wafer-to-Wafer Copper Bonding”, “Process Enhancements in 3D, FOWLP and TSV Technologies”, “AI-based Prediction for Heterogeneous Integration and Advanced Packaging”, and “Trends in Encapsulants and Low Dk/Df Dielectrics”.

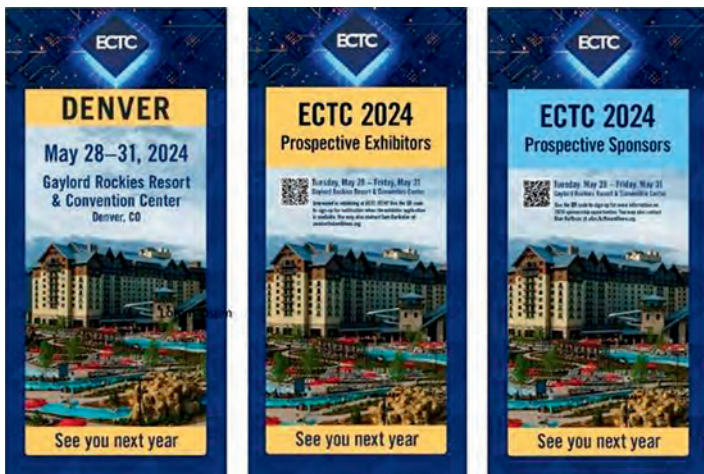
During Friday’s luncheon we had a traditional Raffle chaired by Alan Huffman - ECTC Exhibit Chair, having several prizes from

our sponsors including a hotel stay, free conference registration, IEEE EPS membership, books, and many other cool gadgets.

Friday afternoon included the sessions “MEMS sensor, Bio, and Advanced Interconnect Reliability”, “Thermo-Mechanical Modelling and Characterization”, “Advances in RDL, Via, TSV Technologies for Chiplet Integration”, “Bonding Assembly – Novel Packaging, Process, and Characterization”, “Packaging and Materials for Flexible Medical Technologies”, and “RF, Heterogeneous, and Chiplet Modules”.



Overall, the 73rd ECTC was an amazing experience, giving us an opportunity to meet in an excellent location, and have a lot of discussions regarding future development of electronic components. This was the second largest ECTC conference in respect of participation with the record attendance in Orlando. ECTC became a four-day conference. Changes were introduced in the program, such as special sessions on Tuesday and Wednesday to Friday morning. One of the many highlights was Wednesday’s keynote about Quantum Computing. Shortening technical presentations make the discussion much more dynamic. We also had a very strong exhibitor presence, excellent sponsorship, and many high-quality technical presentations with excellent presentation attendance. The ECTC Executive Committee sincerely thanks all the attendees, exhibitors, and conference sponsors (ECTC 2023 platinum sponsors: Amkor, ASE, JCET) for their support as well as all the committee



members and chairs who are volunteering their time to help organize the technical sessions and make ECTC such a success every year. Very special thanks also to our excellent event management team for bringing back the in-person reality flawlessly. See all the conference pictures at [Flicker](#) and keep in touch with the ECTC through [LinkedIn](#).

The 74th ECTC will be held at Gaylord Rockies Resort & Convention Center, Denver, Colorado, USA, May 28–31, 2024. Karlheinz Bock from Technical University Dresden will be the General Chair of this conference. The Call for Papers and PDC Proposals will be available at www.ectc.net, and the abstract submission will close on October 09, 2023. So get those abstracts ready and submit them as soon as abstract submission opens.

I look forward to meeting you at Gaylord Rockies Resort and Convention Center, Denver, Colorado, May 28–31, 2024.



25th Electronics Packaging Technology Conference (EPTC2023)

The IEEE EPS Electronics Packaging Technology Conference (EPTC) is an international event organized by the IEEE RS/EPS/EDS Singapore Chapter and co-sponsored by the IEEE Electronics Packaging Society (EPS). Since its inauguration in 1997, EPTC has been established as a highly reputable international electronics packaging conference and is the IEEE EPS flagship conference in the Asia and Pacific Region.

The 25th Electronics Packaging Technology Conference (EPTC2023) will take place from 5th December to 8th December 2023 at Grand Copthorne Waterfront Hotel, Singapore. It will feature keynotes, technical sessions, invited talks, panels, workshops, exhibitions, and networking activities. Topics include modules, components, materials, equipment technology, assembly, reliability, interconnect design, device and systems packaging, heterogeneous integration, wafer-level packaging, flexible electronics, LED, IoT, 5G/6G, emerging technologies, 2.5D/3D integration technology, smart manufacturing, automation, MEMs, sensors and AI.

As this year marks the 25th anniversary of EPTC, a special 4-day program has been arranged including many keynotes, panels, invited talks and a great social program. The following keynotes have been confirmed to date:

Confirmed Keynotes:

1) Dr. Douglas C. H. Yu, VP of R&D, TSMC



Title: Advanced System Integration Technology Trend

Abstract: HPC and AI/ML technologies have profound impact on human society. Semiconductor technology plays critical roles to realize these. Recent progress in generative AI drives AI/ML's impact to a new height. Higher performance computing with ever-increasing model size requires much higher level of computation performance, communication and memory bandwidth, all at higher energy efficiency (EE). Advanced nodes Si scaling is expected to continue providing higher performance computing with higher EE. Advanced heterogeneous system integration technologies, however, can provide even more values than before for the HPC and AI/ML systems. This can be achieved by the scaling up of classical(microelectronics)-based system integration, advanced photonics-based system integration, as well the two integrated.

2) Dr. Radha Nagarajan, Marvell Senior VP, CTO

Title: 2.5D/3D Heterogeneous Integration for Silicon Photonics Engines



Abstract: As, per lane, data rates continue to rise, optical interconnects are getting closer and closer to the processor to minimize overall system power consumption. To this end, to design what is essentially a processor with optical IO, higher levels of integration are needed to build optical engines. We will discuss various integration approaches that have been taken to accomplish very compact optical interconnect systems.



demanding high performance chiplet computing needs. This presentation will discuss innovative BGA, Fan-Out with FC technologies – FOCoS, plus 2.5D/3D packages, describing how the integration needs are optimized with higher precision, effective layout with enhanced electrical signal and power performance, very essential for new generation AI server, data center, 5G and latest edge computing applications.

3) Dr. C. P. Hung, VP Corporate R&D, ASE

Title: Advanced Packages Enriching Heterogeneous Integration

Abstract: Advanced IC Packages are typically Ball Grid Array (BGA) and Flip-Chip (FC) based with various structures to meet

Do not miss this opportunity to be part of EPTC2023! Please visit the conference website <https://www.eptc-ieee.net/> for more information and updates. To view a video of EPTC2022, please click [here](#).

Top Conference Papers Based on Usage

2022 IEEE 72nd Electronic Components and Technology Conference (ECTC)

(May 31–June 3, 2022)

Organic Interposer CoWoS-R+ (plus) Technology

M.L. Lin; M.S. Liu; H.W. Chen; S.M. Chen; M.C. Yew; C.S. Chen; Shin-Puu Jeng

3D Packaging for Heterogeneous Integration

Rahul Agarwal; Patrick Cheng; Priyal Shah; Brett Wilkerson; Raja Swaminathan; John Wu; Chandrasekhar Mandalapu

Buried Power Rails and Nano-Scale TSV: Technology Boosters for Backside Power Delivery Network and 3D Heterogeneous Integration

Anne Jourdain; Michele Stucchi; Geert Van der Plas; Gerald Beyer; Eric Beyne

Wafer to Wafer Hybrid Bonding for DRAM Applications

Jinwon Park; Byungho Lee; Heesun Lee; Dail Lim; Jiho Kang; Changyun Cho; Myunghee Na; Ilsup Jin

Chiplet-based System PSI Optimization for 2.5D/3D Advanced Packaging Implementation

Yoonjae Hwang; Sungwook Moon; Seungki Nam; Jeong HoonAhn

2022 21st IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)

(May 31–June 3, 2022)

Package level thermal analysis of backside power delivery network (BS-PDN) configurations

Herman Oprins; Jose Luis Ramirez Bohorquez; Bjorn Vermeersch; Geert Van der Plas; Eric Beyne

From 2.5D to 3D Chiplet Systems: Investigation of Thermal Implications with HotSpot 7.0

Jun-Han Han; Xinfei Guo; Kevin Skadron; Mircea R. Stan

Thermal Modeling and Analysis of High Bandwidth Memory in 2.5D Si-interposer Systems

Taehwan Kim; Jonggyu Lee; Jaechoon Kim; Eung-Chang Lee; Heejung Hwang; Youngdeuk Kim; Dan Kyung Suk Oh

Thermal Design of a Chiplet Module using Monolithic die and 2.5D/3D packages

Eric Ouyang; Xiao Gu; Yonghyuk Jeong; Michael Liu; Ravi Agarwal; Yin Hang

Thermal perspective design Analysis of 3D stacked chip integrated by TSV, Micro-bump and TMV with SOC

Youngsang Cho; Kyoungmin Lee; Kyojin Hwang; Heeseok Lee; Yunhyeok Im; Minkyu Kim

2022 9th Electronic System-Integration Technology Conference (ESTC)

(September 13–16, 2022)

Design, Fabrication and Measurement of FOWLP-based Series-Fed Antennas for 6G D-Band MIMO Applications

Thi Huyen Le; Oliver Schwanitz; Ivan Ndip; Friedrich Mueller; Tanja Braun; Martin Schneider-Ramelow

10 μm and 5 μm Die-to-Wafer Direct Hybrid Bonding

Emilie Bourjot; Alice Bond; Carine Ladner; Nicolas Bresson; Stéphane Moreau; Viorel Balan; Arnaud Cornélis; Renan Bouis; Catherine Euvrard; Noura Nadi; Loic Sanchez; Frank Fournel; Nicolas Raynaud; Pascal Metzger; Eric Ollier

Novel Cu-nanowire-based technology enabling fine pitch interconnects for 2.5D/3D Integration

Adil Shehzad; Ran Yin; Iuliana Panchenko; Maik Müller; Steffen Bickel; Olav Birlem; Sebastian Quednau; Jürgen M. Wolf

Low Height Wire bond Looping Technology using Wedge Bonding for the MMIC Package

Ah-Young Park; Jae Hak Lee; Seungman Kim; Sumin Kang; Seongheum Han; Seong-Il Kim; Jun-Yeob Song

PCB Embedding Technology for 5G mmWave Applications

Stefan Kosmider; Thomas Löher; Andreas Ostmann; Kavin Murgesan; Uwe Maaß; Martin Schneider-Ramelow; Le Thi Huyen; Michael Kaiser

2022 IEEE 24th Electronics Packaging Technology Conference (EPTC)

(December 7–9, 2022)

Demonstration of 50 nm Overlay Accuracy for Wafer-to-Wafer Bonding and Further Improvement Study

Hajime Mitsuishi; Hiroshi Mori; Hidehiro Maeda; Mikio Ushijima; Masanori Aramata; Minoru Fukuda; Masashi Okada; Masahiro Kanbayashi; Toshimasa Shimoda; Isao Sugaya

700nm pitch Cu/SiCN wafer-to-wafer hybrid bonding

Soon-Aik Chew; Serena Iacovo; Ferenc Fordor; Sven Dewilde; Katia Devriendt; Joeri De Vos; Andy Miller; Gerald Beyer; Eric Beyne

Cu CMP Dishing Control for Fine Pitch Wafer-to-Wafer (W2W) Hybrid Bonding

Hong Miao Ji; Gim Guan Chen; K.-J. Chui

Reliability of lead-free solders for die attach in automotive power modules

Bettina Ottinger; Joshua Holverscheid; Sebastian König; Edgar Jerichow; Sebastian Lunz; Mario Sprenger; Lars Müller; Christian Goth; Jörg Franke

Reduction of Aluminum Fluoride Formation during Fluorinated Plasma Etching of Dielectric Passivation Layer over Aluminum Pad

Darshini Senthilkumar; Kalyn Lim Tien Shee; B.S.S. Chandra Rao

Upcoming Conferences

The following is the current status of the EPS sponsored conferences for the remainder of 2023 which are all scheduled as in-person events. However, please reference the EPS conference page weekly for the latest updates.

2023 24th International Conference on Electronic Packaging Technology (ICEPT)

Shihezi City, China
Aug 8, 2023–Aug 11, 2023

2023 24th European Microelectronics and Packaging Conference & Exhibition (EMPC)

Cambridge, United Kingdom
Sep 11, 2023–Sep 14, 2023

2023 IEEE International Conference on Quantum Computing and Engineering (QCE)

Bellevue, WA USA
Sep 17, 2023–Sep 22, 2023

2023 45th Annual EOS/ESD Symposium (EOS/ESD)

Riverside, CA USA
Oct 1, 2023–Oct 6, 2023

2023 IEEE 68th Holm Conference on Electrical Contacts (HOLM)

Seattle, WA USA
Oct 4, 2023–Oct 11, 2023

2023 IEEE 32nd Conference on Electrical Performance on Electronic Packaging and Systems (EPEPS)

Milpitas, CA USA
Oct 15, 2023–Oct 18, 2023

2023 18th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)

Taipei, Taiwan
Abstract Submission Date: Jun 21, 2023
Oct 25, 2023–Oct 27, 2023

2023 IEEE International Conference on Microwaves, Communications, Antennas, Biomedical Engineering and Electronic Systems (COMCAS)

Tel Aviv, Israel
Nov 6, 2023 - Nov 8, 2023

2023 IEEE CPMT Symposium Japan (ICSJ)

Kyoto, Japan
Nov 15, 2023–Nov 17, 2023

2023 IEEE Symposium on Reliability for Electronics and Photonics Packaging (REPP)

Milpitas, CA USA
Abstract Submission Date: Aug 15, 2023
Nov 16, 2023–Nov 17, 2023

2023 IEEE 25th Electronics Packaging Technology Conference (EPTC)

Singapore
Dec 5, 2023–Dec 8, 2023

2023 IEEE Electrical Design of Advanced Packaging and Systems (EDAPS)

Rose-Hill, Mauritius
Dec 12, 2023–Dec 14, 2023

TECHNOLOGY

Packaging Power Sources for WSN IoT Edge Devices

Wireless Sensor Network (WSN) IoT edge devices bring benefits to industry and society, helping us monitor the performance, location and ‘well-being’ of machines, factories (energy and resource efficiency, agility), vehicles, renewable energy systems and even people. They help make the world a better connected, informed, safe, energy efficient & secure place. However big challenges exist on how to power them reliably, minimising maintenance and downtime, ideally with the battery outliving the application needs. A typical WSN node battery lifetime is currently 12-18 months for most applications versus a need of at least 5-10 years. This is perhaps the biggest impediment to the explosive growth of IoT devices. Longer battery life requires a strategy of finding ways of minimising device power consumption whilst using ambient energies where available (heat, vibrations, light) as an additional ‘energy harvesting’ (EH) source of power. Such systems are complex, requiring careful design and integration from material all the way to system integration. In particular, EH needs to be seen as much more than an electronics discipline but as a collaborative multi-disciplinary ecosystem, especially at the early conceptual stages (ref. Fig. 1). The EU EnABLES project position paper (<https://www.enables-project.eu/outputs/position-paper/>) describes this need and value proposition. Related to power electronics packaging, this includes MEMS & NEMS integration of materials and devices as well as packaging of the overall power source that replaces the battery. This extends further to the WSN node incorporating sensors, MCU (microcontroller), transceiver, interconnect, housing, etc. Without the assistance of such enabling technologies the potential of EH and related technologies cannot be unleashed.

Energy harvesting has been featured in PSMA’s (Power Sources Manufacturing Association) power technology roadmap (PTR) since 2017 and is expected to evolve from being an emerging technology to gaining widespread adoption, particularly to address the battery life problem (<https://ieeexplore.ieee.org/document/9800843>).

Further evidence of the strategic importance of energy harvesting can be found in the EU ECS-SRIA (<https://ecssria.eu/>) & IEEE HIR (<https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html>) & IRDS roadmaps (<https://irds.ieee.org/>), and PSMA’s white paper <https://www.pasma.com/basiccontentitems/psma-white-paper-energy-harvesting-green-internet-things>.



Figure 1. The Power IoT ecosystem (source EnABLES position paper).

Some wearable concepts

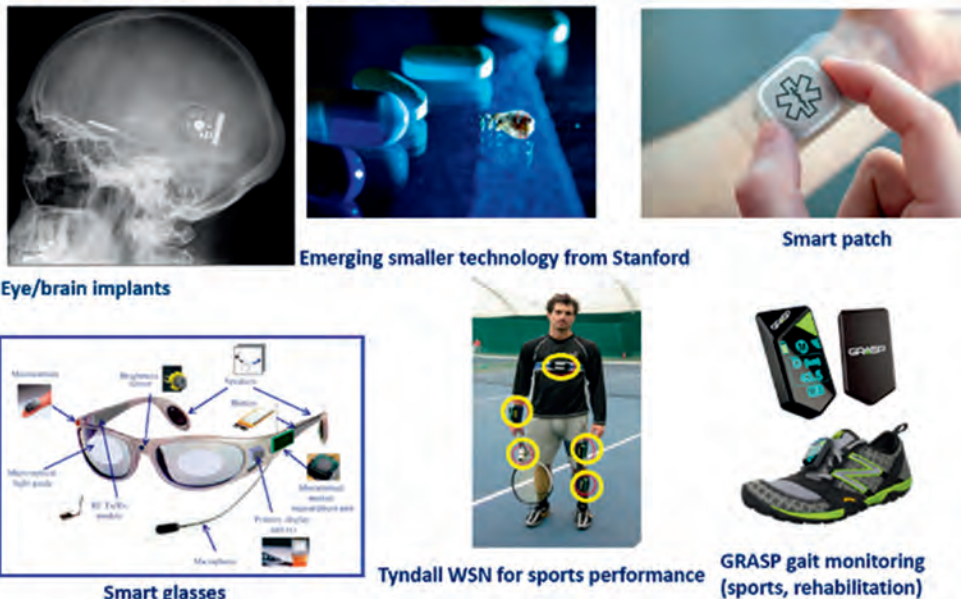


Figure 2. Some Wearable concepts.

Some attempts to self power

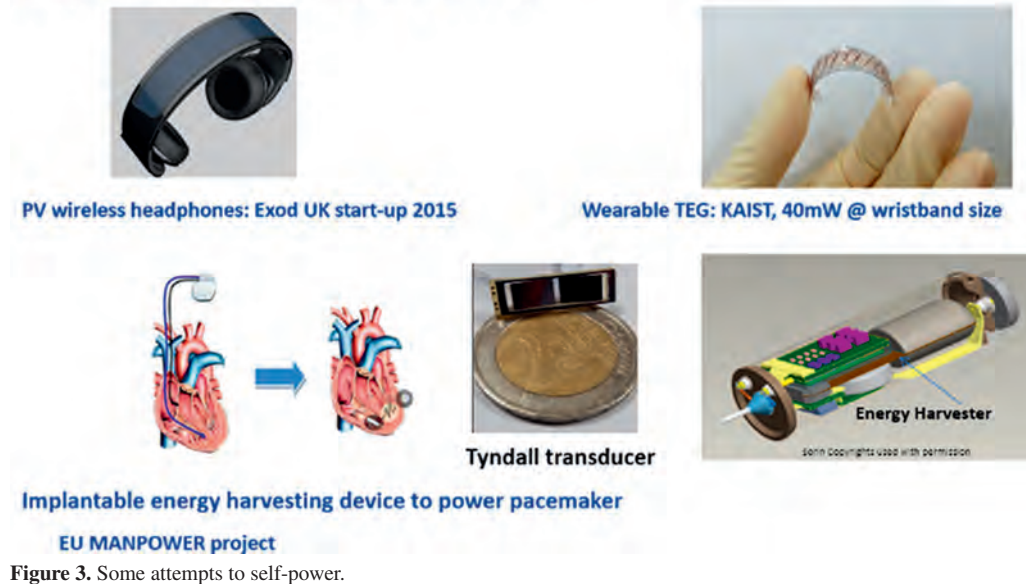


Figure 3. Some attempts to self-power.

One clear recurring message from various initiatives is the need for the entire community from developers and researchers to users and integrators to collaborate if we are to solve the ‘power IoT’ challenge. Furthermore, standardisation and interoperability with supporting simulation tools are seen as critical enablers for the various stakeholders to be able to collaborate and develop system optimised solutions.

IoT edge devices come in many sizes and shapes to meet application needs. Some wearables examples are shown in Fig. 3 below requiring various types of components, substrates, batteries, packaging, etc. For many applications the ability to reliably miniaturize and embed components becomes a key enabler. This not only includes sensors, micro-controllers, batteries and transceivers but also energy harvesting and storage devices. Flexible electronics, nanotechnology, additive manufacturing, material choices (e.g., for bio-compatibility and recyclability), process compatibility (e.g. for embedding passive and active devices onto silicon) are all examples of the need for stakeholders from many different technology disciplines to collaborate.

Looking at the challenges in developing PSiP (Power Supply in Package) and PwrSoC (Power Supply on Chip) solutions, the value of synergies should be clear. There is already evidence of such technology being commercialised by TSMC, already offering a standard process for embedding magnetics on silicon, and Murata (IPDIA)

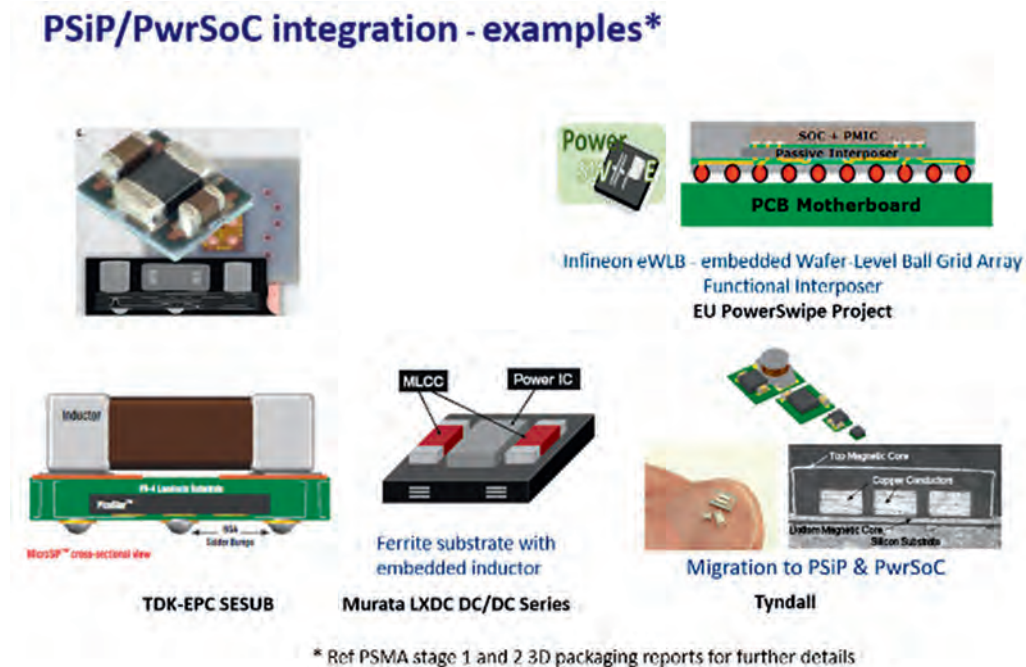


Figure 4. PSiP & PwrSoC Solutions.

There have also been several international and EU micro-power energy harvesting related projects/initiatives & networks such as ASSIST (personalised health monitoring — <https://assistcenter.org/>), EnSO (energy for smart objects — <https://cordis.europa.eu/project/id/692482>), HarvestAll (vibrational energy harvesters — <https://cordis.europa.eu/project/id/827645/results>), Energy ECS (smart mobility solutions — www.energyecs.eu), POLYSTORAGE (energy storage polymers — <https://www.polystorage-etn.eu/>), SYMPHONY (Smart Hybrid Multimodal Printed Harvesting of Energy — <https://www.symphony-energy.eu/>), SMART2GO (EH wearables — <https://smart2go-project.eu/>) and AMANDA (EH sensors for environmental monitoring and asset tracking — <https://amanda-project.eu/about>).

embedding CMOS compatible storage devices (albeit not yet at the energy levels required for mainstream IoT edge devices). Examples of various PSiP & PwrSoC solutions are illustrated in Fig. 4, which are discussed in PSMA’s stage 1 and 2 3D packaging reports (which can be obtained from <https://www.pdma.com/publications>). The creation of an updated report is currently under consideration by PSMA (in collaboration with IEEE EPS) in the light of recent technology developments (e.g. in printed and flexible electronics) and the expected explosion in demand for embedding of energy harvesting and related components.

PSiP and PwrSoC devices will become increasingly complex as we attempt to add in both energy harvesting and storage devices as well as embedding other components such as microcontrollers,

transceivers, magnetics and sensors into System on Chip and System in Package solutions. They can be partitioned in different ways (Fig. 5) depending on form factor, modularity and configurability needs of the end user applications. Integration of enclosures, antennae, etc. can be much more efficient if the various stakeholders collaborate during the system development rather than serially. This can be particularly effective and accelerate time to market as new emerging technologies in embedded-packaging, substrates, materials and components are considered at the system level, while taking into account manufacturability, process compatibility and testability. In addition, WSN nodes should ideally be easy to install, embed and be unobtrusive. Form factor, miniaturisation and use of technologies such as printed and flexible electronics will be critical for some applications.

Tyndall National Institute, Ireland in collaboration with the SFI CONNECT research centre (www.connectcentre.ie) has developed the concept of an eSiP (energy Source in Package) to foster collaborations between stakeholders and drive TRL progression of energy harvesting powered solutions. The idea is to create a series of eSiP concepts for various applications, mixing and matching COTS & emerging technologies. These in turn are integrated into EH powered WSN platforms. The 1st manifestation is a smart patch as shown in Figs. 6 & 7 whereby an array of TEGs (thermoelectric generators) are embedded on a flex circuit and energy harvested to measure body temperature readings.

Functionality can be improved accordingly as the energy harvested is increased. To achieve this requires the abovementioned ecosystem of collaboration, not only designing and integrating parts but also simulating and co-designing their integration to optimise performance, in this case with small temperature gradient and airflows.

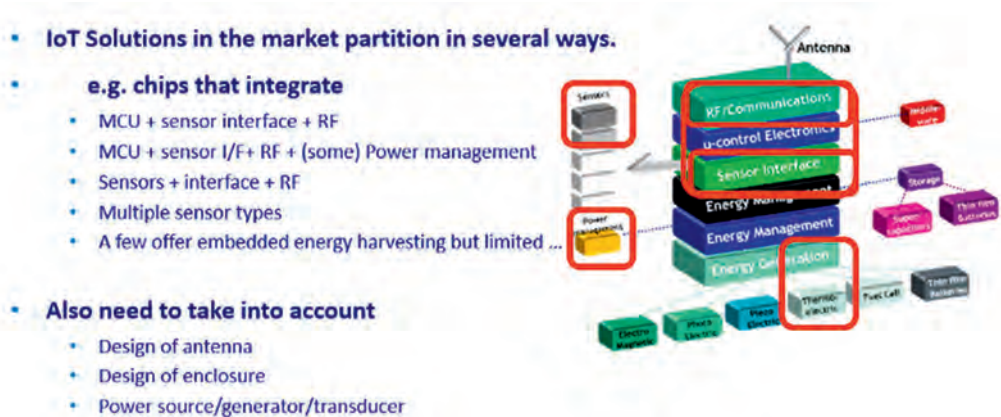


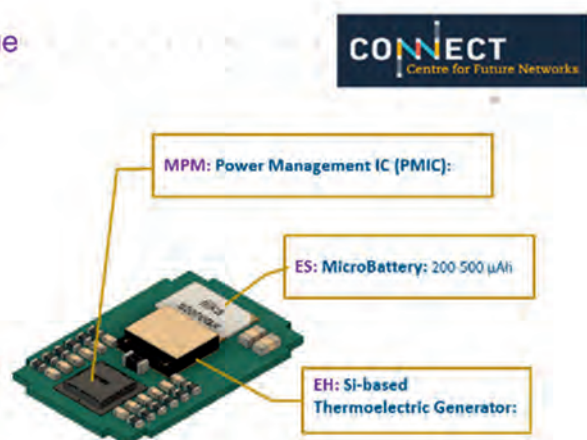
Figure 5. IoT edge device partitioning.

eSiP energy Source in Package – integration of EH, ES, MPM*

- Progress from COTS to research platforms

Integration Technologies:
 - PCB, PCB-embedding, Flexible
 - Micro-Transfer Printing (MTP)

Integrate into SELF POWERED demo



* EH: Energy Harvesting ES: Energy Storage MPM: Micro Power Management
 COTS = Commercial Off The Shelf

Figure 6. eSiP concept.

EnTiCe Smart Patch Demo Energy harvesting Testbed for Integrated and Connected eSiPs

Value proposition = miniaturised, wearable, med tech, self-powered

- Self powered (30µW) with 35°C temp source
- BLE temp reading every 78 sec to mobile app
- Reconfigurable (can miniaturize)
- Simulation models will optimise for lower airflow and/or increased functionality (e.g. pulse, motion, SPO₂)

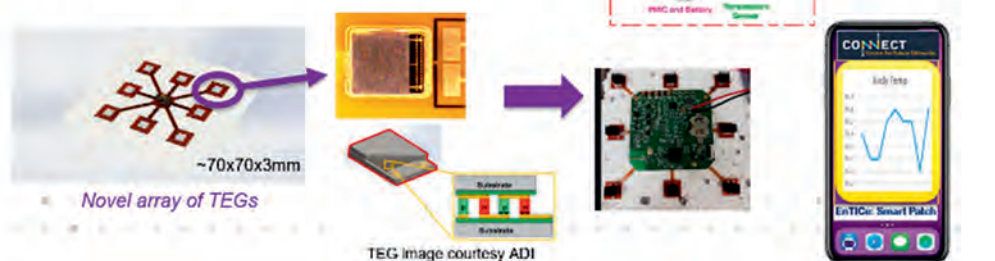


Figure 7. Smart Patch WSN platform.

Sustainable IoT: “Just Enough”

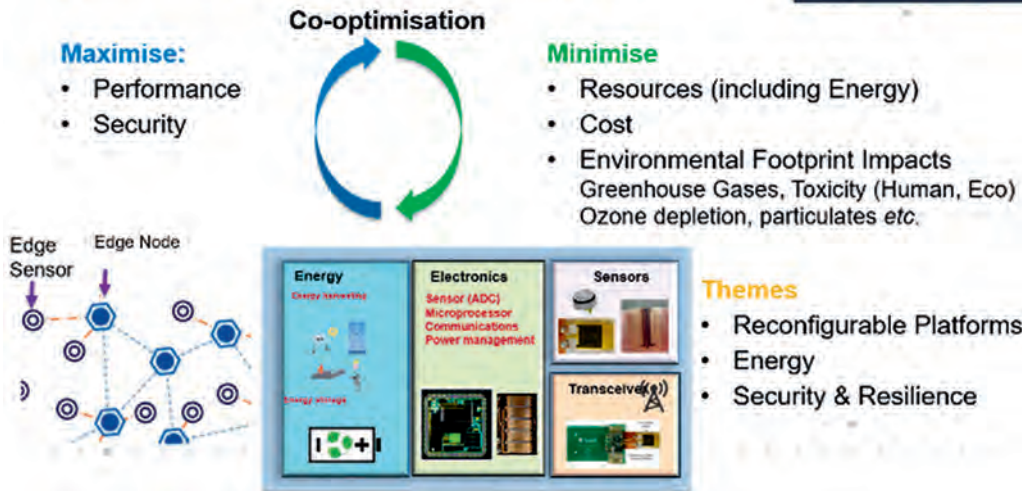


Figure 8. CONNECT sustainable IoT activities.

Sustainable Fabrication



- Sustainable precursor materials and manufacturing processes
- Complementary modelling and design of green sensors, supercaps and compostable antennas
- Novel solutions for sustainable and reconfigurable sensing

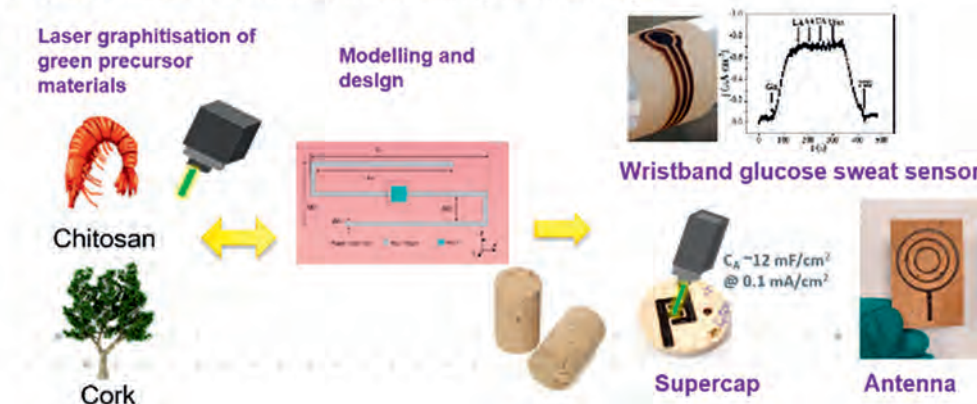


Figure 9. Sustainable materials and fabrication.

Sensors themselves have been integrated into various packaging form factors with varying degrees of success. They suffer from the same issue as the ambient energies transducers we have in mind for energy harvesting, i.e. ‘how do we expose them to the external environment whilst still protecting them from damage, ingress, etc.’ The replacement of a battery with an energy harvesting power source also brings many assembly, packaging and integration challenges, particularly the energy harvesting transducers which rely on precise placement for their successful and repeatable operation (alignment and proximity to the heat, light or vibrational source). Similar problems arise with wireless power transmission systems.

Finally, environmental aspects must be taken into account, all the way from the sustainability of the materials used to the life-cycle footprint of WSN devices and minimising of the number of batteries going to landfill. Are the materials available in abundance from multiple sources and do they come from stable sources (environmen-

tally and geopolitically)? What is the energy and carbon footprint associated with sourcing and processing these materials and integrating them into devices and assemblies? What happens to the materials, device and assembly beyond operational life? Are they recyclable, will they self-decompose in the environment, can they be disassembled, re-used or re-purposed, are they incinerable, are they toxic? In addition to eSiPs, the Sustainable IoT group in CONNECT is also developing “green” sensors, supercaps and antennae. The team uses a combination of biodegradable, abundant and renewable material components such as cork and chitosan (from crustacean shells) and low environmental footprint fabrication methods (such as laser writing techniques), which operate at room temperature, without use of chemicals or solvents and produce no waste (Figs. 8 & 9).

In summary, there is a major opportunity to use WSN technology to make the world a better, connected, efficient, safe and secure place but there are challenges to offer reasonable battery life. We need to bring various communities of experts from various disciplines together and foster closer and earlier collaboration for mutual benefit. The technologies encompass low power sensors, micro power management, Wireless Sensor Network design, energy harvesting devices and systems, embedding of materials and devices in sub-assemblies and packages on

silicon. It is underpinned by various other enabling technologies such as flexible electronics, additive manufacturing, nanotechnology, lower power electronics as well as multi-physics simulation models to help design system optimised solutions from the onset.

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Brian Zahnstecher, PowerRox

Acknowledgement:

CONNECT (project code 13/RC/2077_P2) is the world leading Science Foundation Ireland (SFI) Research Centre for Future Networks and Communications. It is funded under the SFI Research Centres programme, which has established a network of SFI Research Centres focusing on key research areas in Ireland.

New generation of lead-free solder alloys with high thermal reliability for applications in harsh environments

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I. INTRODUCTION

Lead-free solder alloys have been widely adopted by the electronics industry since the Restrictions on Hazardous Substances (RoHS) regulations were implemented in the European Union in July 2006. In the past decades, lead-free SnAgCu ("SAC") solder alloys such as Sn3.0Ag0.5Cu (SAC305) and Sn3.8Ag0.7Cu (SAC387) have been used extensively in portable, computing, and mobile electronics, which operate in temperatures of 125°C and below. Automotive electronics must operate in temperatures around 150°C for under-the-hood devices and below 125°C for devices in the passenger compartment. These electronics must also be able to function in very low temperatures, requiring an operational range of -40°C to +150°C.

For such harsh environments, the traditional binary or ternary lead-free Sn-rich solder alloys are not reliable enough to survive. Relative to the melting temperature of most Sn-rich solders, the homologous temperature at 150°C equals to 0.876 for SnAgCu-3Bi, 0.863 for SnAgCu, 0.856 for Sn-3.5Ag and 0.846 for Sn-0.7Cu, indicating that atomic diffusion will facilitate microstructural evolution and accelerate joint degradation. Higher operating temperatures result in increased rates of microstructural coarsening and joint degradation. The disclosed high-reliability solders for higher-service-temperature applications reflect consideration of metallurgical designs to approach environmental performance issues. These designs slow down the microstructural evolution of the joint solder body and interfacial intermetallic compound (IMC) growth originating from atomic diffusion under thermal migration, which in return maintains the joint fatigue resistance.

In addition to temperature, automotive electronics need to survive continuous vibration and mechanical shocks during vehicle movement and braking. Ductile joints are desired because of their improved vibration/shock resistance. However, interfacial IMC growth and microstructural evolution render the joint more brittle, especially at higher temperatures. Thus, it is desirable to design a ductile joint sustainable during operation under harsh conditions.

High-temperature and high-reliability Sn-rich solder can be used for high-brightness (HB) LED chip module assembly and die-attachment in power semiconductor modules. For power semiconductor modules, the joule heat generated from the loaded electrical current will increase the joint junction temperature to 150°C or even higher, depending on the module design. Higher current densities cause increased joint temperatures if the heat-dissipation method remains the same.

During operation, the HB-LED will heat the joints (both the anode and cathode joints as well as the thermal pad joint between the two electrodes) up to 150°C or even higher rapidly depending on the operational electrical current and the cooling pad design, similar to that in power modules. The transit heat in the high-power devices, including both HB-LED and power modules, would severely stress the bonding joint. Thus, the design of the high-reliability solder for power devices must improve the joint resistance to both current and thermal stressing, which can be implemented by controlling the atomic diffusion under both electro-migration and thermal migration.

To address the need for solder materials for the automotive industry and power devices, novel metallurgical designs for high-reliability lead-free solders focus on stabilizing the microstructural evolution and slowing down the interfacial IMC growth under both thermal and current stressing conditions.

II. ENHANCED RELIABILITY BY ANTIMONY ADDITION

In the recent development of high-performance lead-free solder alloys, antimony (Sb) plays a key role in improving the thermal fatigue resistance of solder joints in harsh thermal cycling or thermal shock conditions. According to the binary Sn-Sb phase diagrams [1, 2], the solubility of Sb in Sn is approximately 0.5 wt. % at room temperature and about 1.5 wt. % at 125°C. Solid solution strengthening is thus expected in these alloys due to the dissolution of Sb in Sn-based lead-free solders [3].

Alloying with Sb (1.5-9.0wt%) has showed different thermal fatigue resistances [1]. The fine SnSb IMC particles nucleate and grow into nano/micron-sized clusters under certain stoichiometric ratios after reflow solidification. These in-situ SnSb particles inside Sn matrix could be reversely dissolved back to form a solid solution under high temperatures and then precipitate out again after cooling down. Sufficient Sb is required to strengthen the solder alloy with both solid-solution and precipitation [4]. When Sb is reduced below 3.0 wt%, fine SnSb particles are completely dissolved back into the Sn matrix to form a Sn-Sb solid solution if serving at 150°C and above; no SnSb fine particles remain to strengthen the alloy. Strengthening in alloys is associated with interrupting the dislocation movement. Both fine particles embedded in the alloy matrix and solute atoms in the solid solution act as obstacles to inhibit the dislocation slide along the favorable lattice directions. Atomic diffusion favors dislocation movement at high temperatures (homologous temperature > 0.6). For small obstacles like

solute atoms, atomic diffusion can easily assist the dislocation to bypass or “climb over” obstacles. For large obstacles like precipitates, more atomic diffusion steps are needed to allow the dislocations to bypass the obstacles. Thus, precipitates are more effective to maintain high-temperature strength through interfering dislocation movements.

Therefore, 4.5 wt% and more Sb is expected to strengthen the alloys with sufficient precipitates, even above 150°C. However, above 10 wt% of Sb addition, the solder alloys will have a liquidus temperature above 266°C, making it challenging to be reflowed well with the conventional SAC305 process (the peak reflow temperature is usually below 245°C). The optimal Sb content balancing the strengthening and the reflow was found to be at 5.5 wt.% [4–6]. This led to the development of the 90.6Sn-3.2Ag-0.7Cu-5.5Sb (Indalloy®276) high-reliability solder alloy [4].

It has also been reported that Sb slows the growth rate of the interfacial Cu₆Sn₅ IMC [5, 7, 8]. Figure 1 shows the relative growth rate of IMC thickness in SMR0805-resistor joints of the SAC305 and Indalloy®276 during thermal cycling of -40/125°C. The relative growth rate was calculated based on interfacial IMC thickness of 0 cycle. Before the thermal cycling test, the IMC layer thickness in both SAC305 and Indalloy®276 was very close—1.51 and 1.62µm, respectively. After 2000 cycles, the IMC layer in SAC305 grew more than 60% to 2.48µm, nearly tripling the Indalloy®276 growth. Furthermore, between 2000 and 3000 cycles, the IMC layer in SAC305 grew significantly to 170% greater than its value at 0 cycles, while the Indalloy®276 only grew to 70% relative to its starting thickness. Fast interfacial IMC growth on Cu surfaces tends to produce irregular and non-uniform IMC layers. This can lead to reduced mechanical reliability by inducing fractures at IMC interfaces or through the IMC in-drop shock loading [9].

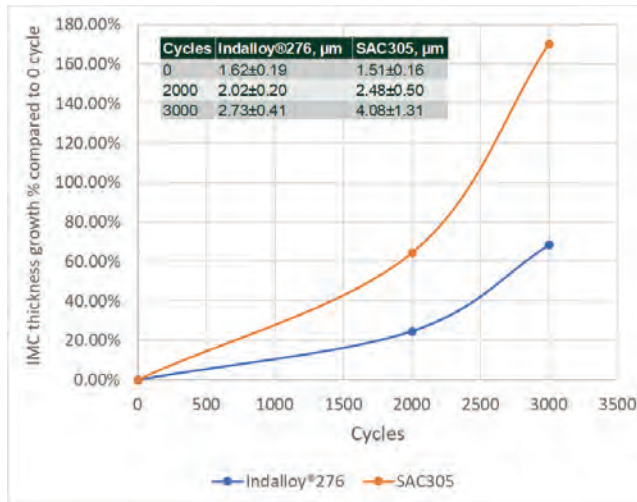


Figure 1. The IMC layer thickness growth rate (compared to zero cycle) in SMR0805 resistors (on ImSn surface finish) of SAC305 and Indalloy®276 at 2000 and 3000 cycles under thermal cycling of -40/125°C.

Figure 2 shows the calculated crack ratios in the joints (SMR0805 resistor on ImSn surface finish) at various intervals of thermal cycling under -40/125°C. The crack ratio

after 3000 cycles was more than 70% in SAC305 while only 23% in Indalloy®276. The crack resistance is much improved in Indalloy®276 compared to SAC305. The observations displayed in Figures 1 and 2 indicate that alloying with Sb may improve thermal fatigue performance through slowing the IMC growth apart from the solid solution strengthening and precipitation hardening mechanisms.

Presumably, the mechanisms involve solid solution strengthening and precipitation hardening, as well as the positive effect brought by Sb to slow down the IMC layer growth. To obtain optimal strengthening, the Sb content was set to 5.5 wt.% to provide enough Sb to have solid solution strengthening and precipitation hardening. This mass density of Sb may cause the alloy to reach an optimal volume fraction of micro-sized SnSb intermetallic precipitates, which are reported by Lu, et al. [10] and El-Daly, et al. [11] to be distributed throughout the Sn dendrites. In this case, the SbSn precipitates form within the Sn dendrites, unlike the well-known SAC Ag₃Sn mechanism where the precipitates form at the Sn dendrite boundaries. The SbSn precipitates appear to resist recrystallization by strengthening the Sn dendrites [12].

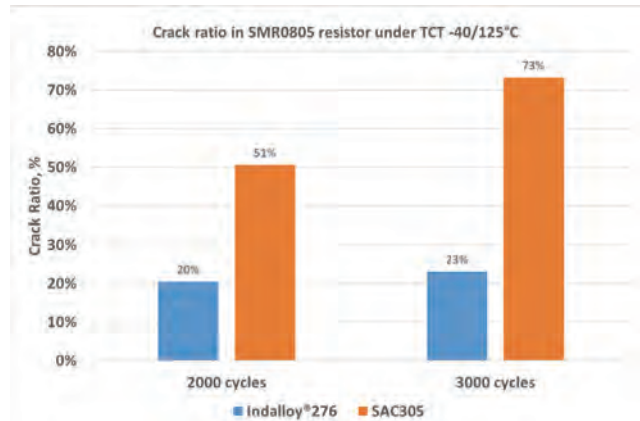


Figure 2. The crack ratio in SMR0805 resistors (on ImSn surface finish) of SAC305 and Indalloy®276 after 2000 and 3000 cycles under thermal cycling of -40/125°C.

III. INCORPORATION OF BISMUTH, INDIUM, AND NICKLE

To further improve the reliability of the SnAgCuSb based solder alloys, bismuth (Bi), Indium (In) and Nickel (Ni) are effective additives. The addition of Bi to the SnAgCuSb alloys can decrease the solidus and liquidus temperatures, thereby decreasing the reflow peak temperature. Bi also reduces the surface tension of the molten solders and improves wettability. Bi does not form any IMC precipitates with Ag, Cu, Sb or Sn. Bi, depending on the content, can strengthen the solder body through Bi particles at low temperatures and hardens the solder body through the formation of solid solutions at high temperatures. Since Bi is brittle, Bi additions beyond 4 wt.% reduce ductility significantly, although strength continues to increase. This embrittlement significantly worsens thermal fatigue resistance. Bi

continuously decreases the melting temperature with its increasing content in the solder and even forms the low melting Bi-Sn phases. These are not desired for high-temperature and high-reliability applications. Therefore, Bi addition of 1.5-3.5 wt% is preferred in the novel high-reliability lead-free solder alloys for harsh-service-environment electronics applications.

In also reduces the solidus and liquidus temperatures of solder. In is much softer than Bi and Sb, which helps to increase ductility and reduces brittleness introduced by the addition of Bi and Sb. In the novel high-reliability lead-free solder alloys with 1.5-3.5 wt% Bi and 5 to 9wt% Sb, enough In adoption minimizes the brittleness introduced by both Bi and Sb. In is prone to being incorporated into the IMC formation similar to Sn, i.e., $Ag_3(SnIn)$, $Cu_6(SnIn)_5$, $Ni_3(SnIn)_4$, and even $(CuNi)_6$ and $(SnIn)_5$, etc [1, 2]. The complicated IMC structure, requiring more atoms to diffuse towards the IMCs to continue the growth, slows down the coarsening of IMC precipitates and the thickening of interfacial IMC layers under elevated temperatures, stabilizing the joints and reducing the joint embrittlement. However, In is more prone to oxidize than Bi, which reduces wetting and increases voiding during reflow if more than 4.5wt% In is added into the solder. Thus, In addition of 4.5 wt% or below is preferred. A preferred In content in the alloy also depends on the Sb content. The addition of In strongly decreases the alloy melting temperature. To maintain high temperature performance of the joint, In addition is preferred to be less than 3.0 wt% to avoid forming these low incipient melting phases in the alloy. Table 1 summarizes the impact of each individual alloying element of Bi, Sb, and In to the Sn-Ag-Cu based solder alloys.

TABLE I. IMPACT OF INDIVIDUAL ALLOYING ELEMENT

Element	Desired Concentration	Strengthening Mechanism	Interfacial IMC formation
Sb	3.0–6.5 wt%	SS + PS(SnSb)	Slow the interfacial reaction
Bi	1.5–3.5 wt%	SS + PS(Bi)	No interfacial reaction with Cu/Ag/Ni at low concentration
In	< 3.0 wt%	SS + Partitioning into $Ag(SnIn)$ and $Cu(SnIn)$ IMC formation	Participate into the interfacial reaction with Cu/Ag/Ni

*SS: solid solution strengthening in Sn matrix

*PS: precipitate strengthening

The addition of small amounts of Ni (0.05-0.25 wt%) effectively improved the alloy's mechanical properties and solder joint reliability performance. During soldering, enough Ni is incorporated into the interfacial IMC formation, especially on Cu metallization, to form $(CuNi)_6Sn_5$ instead of Cu_6Sn_5 . The existence of Ni inside the $(CuNi)_6Sn_5$ layer slows the IMC growth during reflow and post-reflow service, which is important to maintain interface stability and joint ductility. Ni has very limited solubility in Sn. The solder's liquidus

temperature is dramatically increased when Ni is more than 0.3 wt%. Coupled with the reactivity of Ni to oxidation, the negative impacts on wetting and soldering with more than 0.3wt% Ni are observed. These effects are especially pronounced for fine powder solder paste. The interface IMC stabilization is marginal for less than 0.05 wt% Ni content due to insufficient Ni incorporation into the interfacial reaction. Therefore, 0.05-0.25 wt.% of Ni is preferred.

A solder alloy with a composition of 86.7Sn-3.2Ag-0.7Cu-5.5Sb-3.2Bi-0.5In-0.2Ni (Indalloy®292) was developed to achieve high thermal and electrical reliability based on the findings. Power cycling reliability test using HB-LED were carried out for four solder alloys (Table 2), including the commonly used SAC305.

To accelerate the power cycling test (PCT), the electrical current powering the LED was kept at a constant mode of 1A, which overloaded the LED by more than 60% (0.6A working current). Solder joint failures were evaluated in a faster way without damaging the internal wire-bond. The LED power cycler, as shown in Figure 3, was customized by the R&D team at the Indium Corporation. They are capable of testing 8 LED assemblies simultaneously. The LEDs were repeatedly powered on-and-off until failure. The power-on was carried out in a constant current mode for 8 seconds and then was powered-off for 20 seconds. Forced-air circulation was provided to continuously cool the backside of each LED assembly. The voltage, the current, and the backside temperatures of each LED assembly were recorded during power-on with a sample rate of 1Hz. Failure was identified by a sudden electrical current drop, i.e., the LED could not be powered-on anymore.

TABLE II. THE COMPOSITIONS OF SOLDER ALLOYS FOR THE LED POWER CYCLING TEST

Alloy	Sn	Ag	Cu	Sb	Bi	In	Ni
SAC305	96.5	3	0.5	--	--	--	--
276	90.6	3.2	0.7	5.5	--	--	--
276N	90.5	3.2	0.7	5.5	--	--	0.1
292	86.7	3.2	0.7	5.5	3.2	0.5	0.2

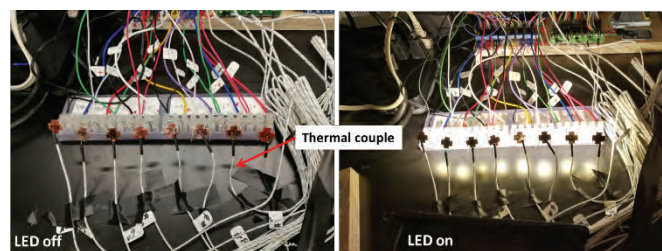


Figure 3. The LED power cycler designed by Indium Corporation. Left: power-off and Right: power-on.

Twelve LED assemblies for each alloy were made and subjected to PCT. Using a two-parameter Weibull analysis, the characteristic life (η , the number of cycles to achieve 63.2% failure N63) and slope (β) were deduced from the failure data. The results are shown in Figure 4 and summarized in Table 3. The characteristic life of Indalloy 292 nearly triples that of SAC305 (4230 cycles) and doubles that of Indalloy 276. When compared Indalloy 276 and 276N,

we find that the addition of 0.1 wt% Ni increases the characteristic life by 37%, from 6092 cycles in Indalloy 276 to 8327 cycles in 276N. The Weibull plot slopes of the four alloys were similar, as shown in Figure 4, indicating they may have a similar failure mode.

TABLE III. POWER CYCLING FAILURE WEIBULL ANALYSIS

Alloy	Slope (β)	Characteristic life (η)
SAC305	3.65	4230
276	4.52	6092
276N	4.06	8327
292	3.11	12160

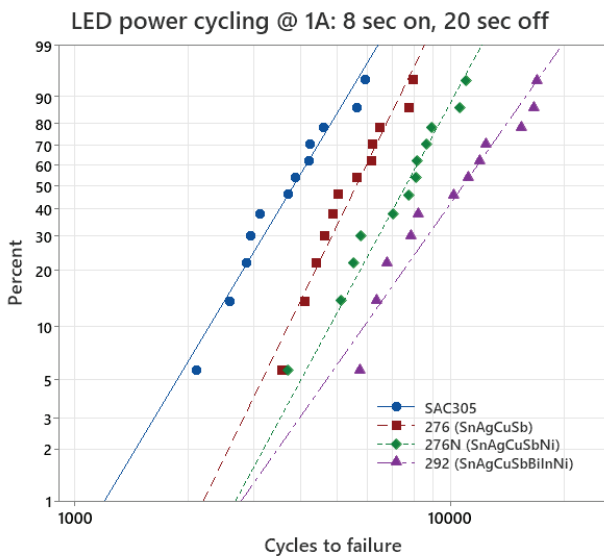


Figure 4. Weibull plot of LED power cycling reliability test

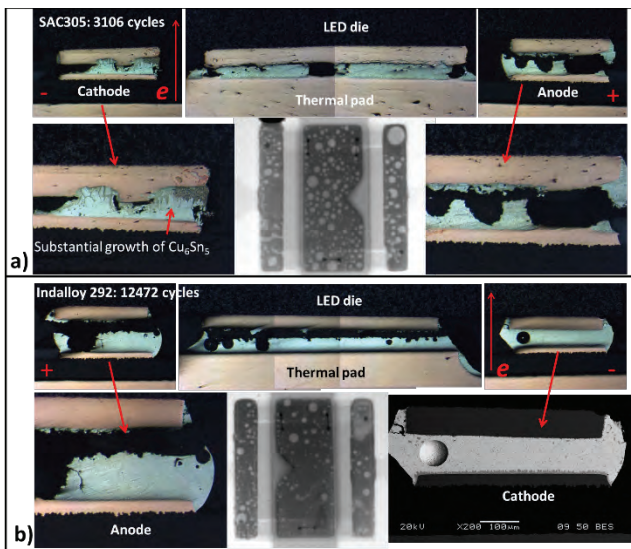


Figure 5. Optical and backscattered electron images showing the detailed microstructure of joints failed after PCTs. The X-ray image is shown in the middle. a) SAC305 failed at 3,106 cycles, b) Indalloy 292 failed at 12,474 cycles.

Figure 5 reveals the morphology of the failed joints after PCT for the SAC305 and Indalloy 292 alloys. The anode joint of SAC305 was open to fail. However, the cathode joint of SAC305 (Figure 5a, failed at 3106 cycles) had substantial growth of Cu_6Sn_5 beneath the LED chip, in which the Cu pad of the cathode joint beneath the LED chip was partially consumed, and Cu_6Sn_5 grew into the Cu pad. The growth of Cu_6Sn_5 in the thermal joint and anode did not penetrate into the Cu pads. The substantial growth of Cu_6Sn_5 and the consumption of the Cu pad were not observed in the cathode joint of Indalloy 292 but were observed in the final microstructure of the electrode joints after failure.

However, that was not the case for the thermal pad. Precipitation and growth of Cu_6Sn_5 at the cathode caused the Cu pad to be quickly consumed and resulted in a void formation at the contact area. The void reduced the contact area and displaced the electrical path, resulting in the current crowding and Joule heating inside the solder bump. Significant Joule heating inside solder joints can cause melting of the solder and quickly lead to failure. The effect of void propagation on current crowding and Joule heating was clearly seen in the X-ray images of the electrodes (Figures 5). However, this kind of Cu_6Sn_5 growth was found to be significantly slowed in the joints of Indalloy 292. This suggests the alloying of Sb, Bi, In, and Ni could effectively slow down the consumption of Cu at the electrodes, resulting in the increase of the characteristic life of the LED by 187% at 4230 cycles for SAC305 and at 12,160 cycles for Indalloy 292. Comparing Indalloy 276, 276N, and Indalloy 292 (Tables 2 and 3) indicates that adding Ni, Bi and In can further slow the consumption of Cu and enhance the reliability to both electrical current and thermal fatigue. The fundamental mechanism of the combination of positive alloying effects brought about by Sb, Bi, and In requires further investigation.

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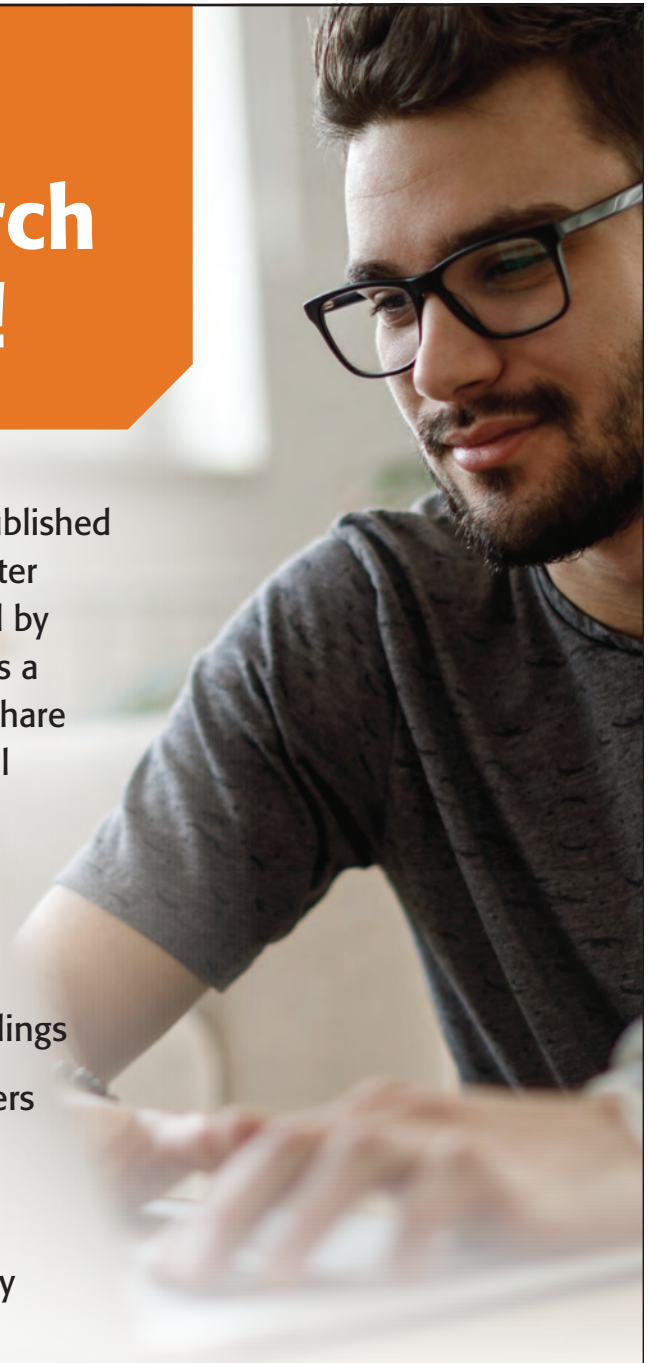
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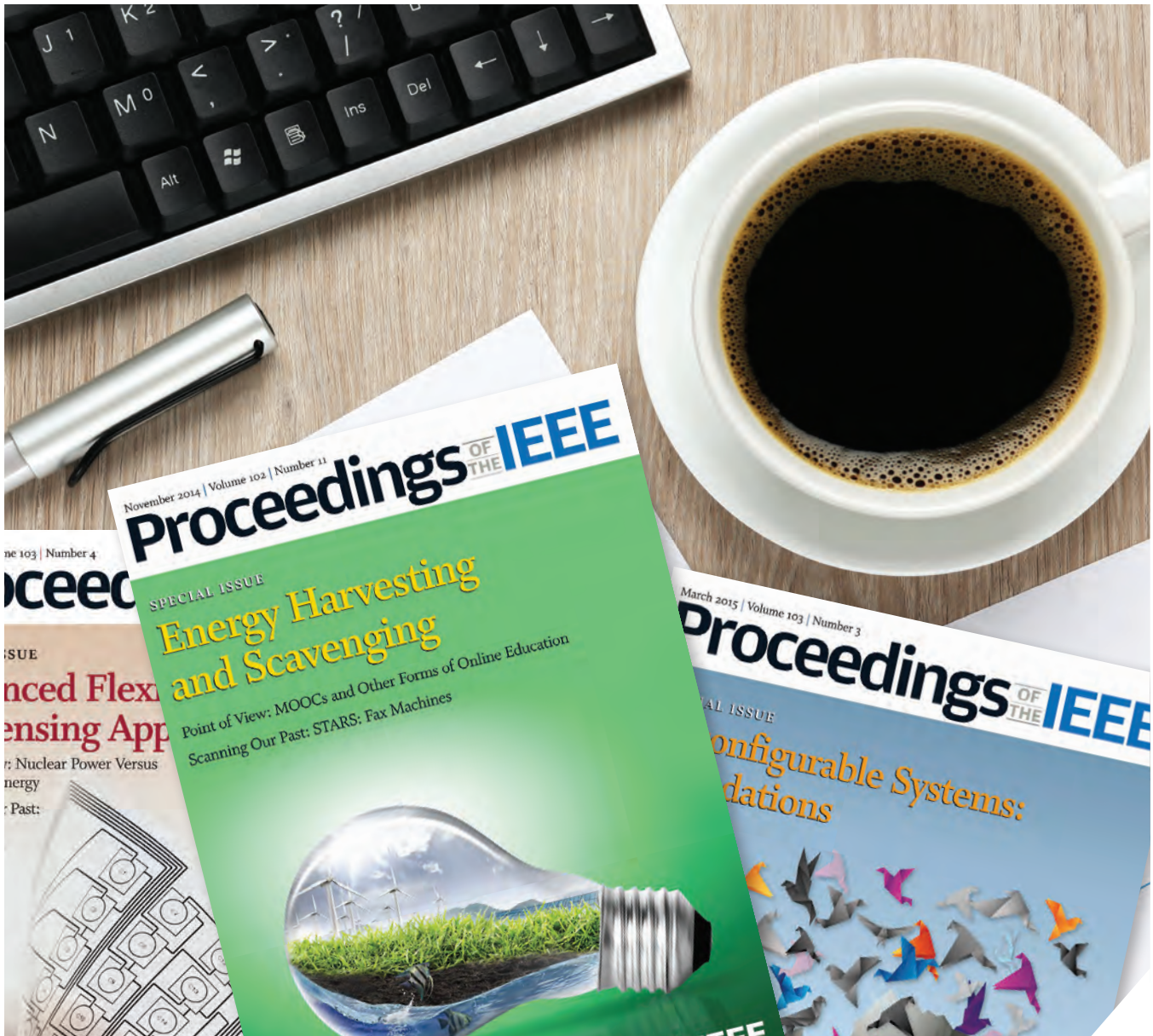
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