IEEE ELECTRONICS PACKAGING SOCIETY Newsletter

JULY 2021
VOL. 43 NO. 2
ISSN 1077-2999

Driving Innovation in Microsystem Packaging /// EPS.IEEE.ORG

PRESIDENT'S COLUMN

Chris Bailey
University of Greenwich
London, UK

As we enter the summer break, I would like to thank you—our members—for your continued support and engagement with the Electronics Packaging Society. In my first president's column (winter 2020), I highlighted our 5-year strategic plan and its goals that I was keen to see progress during my term as president. Working with our functional teams—membership, conferences, education, and technology—I am delighted to summarise some of the achievements we have made over the last 18-months towards these goals:

- *Membership*: Our new resource center provides access to an extensive portfolio of educational material. You can now access webinar material, publications, and other educational resources all within one place. In addition, we have expanded our comprehensive EPS certificate program, which recognizes accomplishments for members who are early-career or mid-late career (details of this certificate program can be found in this newsletter).
- *Technology*: EPS has seen significant growth in its technical committee (TC) activities. Two new committees—Test and Reliability—have been established. The TC's now provde regular articles to this newsletter, the latest being from our Reliability TC, which you can find in this edition. The HIR continues to be a resounding success, with regular workshops and chapter downloads of over 35,000. The 2021 edition is currently being prepared for release this autumn.
- *Conferences and chapters*: Although we have faced lockdowns over the last year, our conference organizers and chapter chairs have adapted to virtual or hybrid event formats, and over 80% of our conferences and planned chapter events went ahead. The number of society chapters has increased to 38 chapters worldwide, and I would like to welcome our recently formed chapter in Dallas to our society.
- *Student programs*: Engaging with the next generation of electronics packaging engineers is extremely important for our society. We have seen significant growth in our student branch chapters over the last 18-months growing from 13 to 19 chapters.

Of course, these achievements towards our strategic goals would not be possible without the dedication and contributions from our volunteers on the board of governors, members of our technical committees, members on the HIR technical working groups, our chapter committees, our conference organisers, and our staff at the EPS office. A special thank you to them all.

This is the second year that both ECTC and ITHERM have taken place using a virtual format throughout June. I was delighted to participate in some of the live panel sessions and witness the engagement with the conference attendees that worked incredibly well. The quality of the presentations and papers delivered at both events was excellent. My thanks to the organizing committees for both events and to Kitty Pearsall (EPS President-Elect) and Jeff Suhling (VP Education) for organizing the professional development courses (PDC's) where attendance was at record numbers. As a community, we have learned a lot about running online events. This experience will undoubtedly factor into our plans as we move beyond the pandemic and maximize our offer to our members worldwide.

Within this newsletter are the lists of the recipients of the 2021 EPS awards. On behalf of the EPS, I send my congratulations to all recipients for their achievements and their outstanding contributions to our society and community.

I hope you agree with me that during the last 18-months, we as a society have accomplished much to address our commitment to you, our members, and the wider electronics packaging community. I also hope you will find the opportunity to engage with EPS as one of our volunteers on the board of governors or contribute

(continued on page 14)

NEWSLETTER SUBMISSION DEADLINES

1 December 2021 for Winter issue 2022

15 June 2022 for Summer issue 2022

Submit all material to d.manning@ieee.org

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2021 Term End: Regions 1-6, 7, 9—Philip Garrou, Eric Perfecto, Pradeep Lall, Region 10—C. Robert Kao, Chih-Pin (C.P.) Hung, Kishio Yokouchi

2022 Term End: Regions 1-6, 7, 9—Rozalia Beica, Xuejun Fan, Subramanian S. Iyer, Region 8—Tanja Braun, Karlheinz Bock, Region 10— Gu-Sung Kim

2023 Term End: Regions 1-6, 7, 9—Mark Poliks, Annette Teng, Patrick McCluskey, Jin Yang, Region 8—Steffen Kroehnert, Region 10—Yoichi Taira, Young Professional—Yan Liu

Publications

Transactions on Components, Packaging and Manufacturing Technology

Managing Editor:
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RF & Thz Technologies:
Manos Tentzeris

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Gnyaneshwar Ramakrishna

3D/TSV:
Peter Ramm

Reliability:
Richard Rao

Test:
Pooya Tadayon

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Lecturers: Ramachandra Achar, Mudasir Ahmad, Kemal Aygün, Muhannad Bakir, Ph.D., W. Dale Becker, Wendem Beyene, Karlheinz Bock, Ph.D., Bill Bottoms, Ph.D., Chris Bower, Ph.D., William T. Chen, Ph.D., Xuejun Fan, Ph.D., Philip Garrou, Ph.D., Subu Iyer, PhD., Beth Keser, Ph.D., Pradeep Lall, Ph.D., John H. Lau, Ph.D., Madhu Iyengar, Ravi Mahajan, PhD., James E. Morris, Ph.D., Mervi Paulasto-Kröckel, Ph.D., Eric D. Perfecto, Mark Poliks, Ph.D., Jose Schutt-Aine, Ph.D., Nihal Sinnadurai, Ph.D., Ephraim Suhir, Ph.D., Chuan-Seng Tan, Ph.D., Rao Tummala, Ph.D., E. Jan Vardaman, Paul Wesling, CP Wong, Ph.D., Jie Xue, Ph.D.

Chapters and Student Branch Chapters

Refer to eps.ieee.org for EP Society Chapters and Student Branch Chapters list

IEEE Electronics Packaging Society Newsletter is published quarterly by the Electronics Packaging Society of the Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016-5997. US $1.00 per member per year is included in Society fee for each member of the Electronics Packaging Society. Printed in U.S.A. Periodicals postage paid at New York, NY, and at additional mailing offices. Postmaster: Send address changes to IEEE EPS Newsletter, IEEE 445 Hoes Lane, Piscataway, NJ 08854.

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SFI Logo

2021 IEEE Electronics Packaging Technology Award

CHIN C. LEE
University of California, Retired
Irvine, CA USA

Sponsored by IEEE Electronics Packaging Society

For contributions to new silver alloys, new bonding methods, flip-chip interconnect, and education for electronics packaging

The IEEE Electronics Packaging Award, sponsored by the IEEE Electronics Packaging Society, recognizes meritorious contributions to the advancement of components, electronic packaging or manufacturing technologies. The technical field for this award includes all aspects of device and systems packaging, including packaging of microelectronics, optoelectronics, RF/wireless and micro-electro-mechanical systems (MEMS), enhancement of technology, impact on the relevant technical community and the profession, benefit to society, and the quality of the nomination.

Chin C. Lee's innovative bonding methods and materials and new packaging technologies have been integral to developing high-temperature and high-power electronics. His work on silver wire bond reliability resulted in a wider process window, lower cost, and higher yield in packaging components. He also discovered that silver alloy is anti-tarnishing, which has had enormous economic and technical impact for applications including optics, astronomy telescopes, and LED packaging. His fluxless soldering technology has enabled numerous bonding designs and is critical to packaging electronics for applications where oxidation effects from solder materials can be problematic. Lee also developed solid-state flip-chip interconnects and formulated quantum bonding theory. He established a materials and manufacturing technology graduate program in 2007 at the University of California, Irvine, which was one of a few such programs at that time.

An IEEE Life Fellow, Lee is a professor (retired) with the University of California, Irvine, CA, USA.

2021 IEEE Electronics Packaging Society Award Recipients

Yong Liu
ON Semiconductors, USA
2021 IEEE EPS Electronics Manufacturing Technology Award
For extensive research and development in the field of analog and power packaging manufacturing assembly process modeling, reliability prediction and innovation.

Wilmer R. Bottoms
3 Millenium Test, USA
2021 Outstanding Sustained Technical Contribution Award
For outstanding entrepreneurship and sustained visionary leadership that continues to foster microelectronics packaging innovation and comprehensive technology roadmapping.

Beth Keser
Intel, USA
2021 Exceptional Technical Achievement Award
For seminal contributions and leadership in Fan-out Wafer Level Packaging.

Tanja Braun
Fraunhofer IZM, Germany
2021 Exceptional Technical Achievement Award
For seminal contributions and leadership in Fan-out Wafer Level Packaging.

Paul Svasta
University Politehnica Bucharest, Romania
2021 David Feldman Outstanding Contribution Award
For strongly promoting and implementing Electronic Packaging and IEEE EPS activities in Europe, Region 8, for establishing a functional networking bridge from Academia to Industry.

Bo Song
HP Inc., USA
2021 Outstanding Young Engineer Award
For outstanding contribution to the development of advanced packaging materials and nanofabrication technology, as well as his service to the IEEE EPS society.

Ranjan Rajoo
Globalfoundries, Singapore
Regional Contributions Award—Region 10 (Asia and Pacific)
For growing R10 flagship conference EPTC through strategic partnerships with the entire microelectronics supply chain, and for contributions to Singapore EPS.

Abhishek Deshpande
University of Maryland, College Park, USA
2021 PhD Fellowship
For his contributions in the development of multiaxial microscale solder joint test specimens and cyclic test setups for demonstrating the differences in solder joint vulnerability to tensile fatigue vs. shear fatigue.

Congratulations to IEEE EPS Senior Members New IEEE EPS Senior Members

The members listed below were elevated to the grade of Senior Member between December 2020 and April 2021.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields for a total of 10 years and have demonstrated 5 years of significant performance.

For additional information or to apply online: https://www.ieee.org/membership/senior/

Che Faxing, Singapore Section
Mei Yunhui, Beijing Section, China
Ken Nakahara, Kansai Section, Japan
Sourajeet Roy, Uttar Pradesh Section, India
Chenxi Wang, Harbin Section, China
Joel Wong, Buenaventura Section, USA
Tieyu, Zheng, Seattle Section, USA

ECTC 2021 Travel Award Winners

Congratulations to the winners of the 2021 ECTC travel award. The award is intended to assist students to attend ECTC. Since ECTC 2021 was virtual, the winners were provided free registration for ECTC 2021.

Ramon Sosa	Georgia Institute of Technology
Claudio Alvarez	Georgia Institute of Technology
Yuki Susumago	Tohoku University
Woosol Lee	University of Florida
Tomo Odashim	Tohoku University
Peng Zhao	Nanyang Technological University
Kai-Cheng Shie	National Chiao Tung University
Seokkan Ki	Kyung Hee University
Sunil Kumar Panigrahy	National Tsing Hua University
Jia Juen Ong	National Chiao Tung University

Congratulations to the ECTC Volunteer Award Recipients

The EPS/ECTC Volunteer Award is given to those individuals who contribute to the success of the ECTC by volunteering in one of the conference committees, year after year. Here are the 2021 EPS/ECTC Volunteer Award winners:

Wendem Beyene	10 years
Abhilash Goyal	10 years
Vikas Gupta	10 years
Ibrahim Guven	10 years
Robert Kao	10 years
Wei Koh	10 years
Nancy Stoffel	10 years
Shaw Fong Wong	10 years
Rao Bonda	25 years
Craig Gaw	25 years
Eric Perfecto	25 years
Suresh K Sitaraman	25 years
Jan Vardaman	25 years

EPS Major Awards Nomination Period Starts on September 15

For the first time all the EPS Major Award nominations will require line submission. The nomination period to input all the required documents runs from September 15 to January 21. The Electronics Packaging Society offers the following awards for the purpose of recognizing outstanding service and contributions to furthering the professional purposes of IEEE and EP Society.

Outstanding Sustained Technical Contributions Award: To recognize outstanding sustained and continuing contributions to the technology in fields encompassed by the EP Society.

Prize: $3,000 and Certificate

Basis for Judging: Technical contributions must be sustained and continuing over a period of at least 15 and preferably 20 years. One major contribution will not qualify. Must be documented by open literature publications such as papers, patents, books and reports (available to the public).

Eligibility: Must have been a member of the IEEE and EP Society for the past three (3) years (2019–2021), and renewed for 2022.

Electronics Manufacturing Technology Award: To recognize major contributions to Electronic Manufacturing Technology in fields encompassed by the EP Society.

Prize: $3,000 and Certificate

Basis for Judging: Contributions may include technical development of, or management (directing) of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes, etc. Contributions must be sustained and continuing over a period of at least 15 and preferably 20 years. Work in the management of EPS Conferences or its BoG may be contributory but it is not a requirement for the award.

Eligibility: No need to be a member of IEEE and EP Society.

David Feldman Outstanding Contribution Award: To recognize outstanding contributions to the fields encompassed by the EP Society through executive or managerial directions.

Prize: $2,500 and Certificate

Basis for Judging: Contributions to the organizations or enterprises connected with the field; contributions to EPS Chapter or Board of Governors activities; contributions to the fields encompassed by the EP Society.

Eligibility: Recipient must have been a member of IEEE and EPS for the past five (5) years (2017–2021), and renewed for 2022.

Exceptional Technical Achievement Award: To recognize an individual, or group of individuals (no more than three), for exceptional technical achievement in the fields encompassed by the EP Society.

Prize: $2,500 and a Certificate.

Basis for Judging: Technical contributions of the nominee(s) must be such that they are considered to be exceptional, not achieved by most members. A single major contribution will qualify for this award. The contribution could be a significant invention, introduction of a significantly new and important technology or product (in which case, the nominee may be a team leader), or significant work that advances the state-of-the-art in EPS's field of interest. The technical contributions must be documented by open literature publications such as papers, patents, books, and reports (available to the public). Technical recognition and awards from the organization employing the individual as well as awards from other IEEE and non-IEEE technical societies may also be contributory.

Eligibility: Recipient(s) must have been a member of IEEE and EPS for the past three (3) years (2019-2021), and renewed for 2022. There are no requirements for service to the IEEE or EP Society.

Outstanding Young Engineer Award: To recognize outstanding contributions to the fields encompassed by the EP Society through invention, technical development, publications, or new product implementation.

Prize: $1,500 and Certificate

Basis for Judging: Technical contributions through patent invention, contributions to technology or product development within the EPS Field of Interest. May encompass management (directing) of significant new product introduction or implementation of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes. Contributions to the Society, through the BoG, Conferences, Chapters, etc., will also be considered. Proof of contributions may consist of open literature publications (preferred) such as papers, patents, books, and reports (available to the public). At least three (3) letters from peers and management at the nominee's place of employment attesting to the accomplishment(s) can be accepted in lieu of publications.

Eligibility: Must have been a member of the IEEE and EPS (member grade or above) for the past three (3) years (2019–2021), and renewed for 2021, and must be 35 years of age, or younger, on December 31, 2022.

Regional Contributions Award: To recognize significant and outstanding leadership and contributions to the growth and impact of EPS programs and activities at the Region level. Maximum of one award annually from each Region/Groups of Regions (3 awards): Regions 1–7 & 9; Region 8; and Region 10.

Basis for Judging: Demonstrated service and leadership in areas that may include but are not limited to Chapter activities, Conference/Workshop activities, Membership Development, Student Programs and Technical Activities. The respective EPS Regional Advisory Committees will receive nominations, evaluate candidates, select a candidate(s), and present candidate(s) to EPS Awards Committee for review and approval.

Eligibility: Recipient(s) must have been a member of IEEE and EPS for the past three (3) years (2019–2021), and renewed for 2022.

Guidelines for Nominators:

- A recipient of any EPS Major Award will be eligible for nomination for another EPS Major Award after two award cycles have passed. (i.e., Recipient of XX Award in 2019 becomes eligible for nomination for YY Award in 2022). For lists of past awardees, see http://eps.ieee.org/awards.html

- Past recipients of an award are not eligible to receive that same award. For lists of past awardees, see http://eps.ieee.org/awards.html
- An individual may submit only one nomination per award but may submit nominations for more than one award.
- An individual may submit only one endorsement per award but may submit endorsement for more than one award.
- It is the responsibility of the nominator to ensure quality documentation to assist the Awards Committee in evaluating the candidate.
- Outstanding Sustained Technical Contribution Award is designed for the "practitioner", while the Electronics Manufacturing Technology Award intended for "Corporate Leadership".
- Complimentary material, such as candidate's picture, CV, list of publications and/or patents should be submitted separate from the award nomination.
- Self-nominations will not be considered.

EPS PhD Fellowship:

To promote, recognize, and support PhD level study and research within the Electronics Packaging Society's field of interest.

Prize: A plaque and a single annual award of US$5,000, applicable towards the student's research.

Basis for Judging: Demonstration of his/her significant ability to perform independent research in the fields of electronic packaging and a proven history of academic excellence, as documented in:

- Nomination by an IEEE EPS Member. Only one nomination per member per year.
- Two-page (maximum) statement by the student describing his or her education and
- Research interests, accomplishments, and impact on the electronics package industry.
- Proof of contributions to the community may consist of open literature publications (preferred) such as papers, patents, books, and conference presentations and reports (available to the public).
- At least one letter of recommendation from someone familiar with the student's work
- Student resume

Eligibility: Candidate must be an IEEE EPS member, at the time of nomination, and be pursuing a doctorate degree within the EPS field of interest on a full-time basis from an accredited graduate school or institution. The candidate must have studied with her/his advisor for at least 1 year, at the time of nomination, to be eligible. A Student who received a Fellowship award from another IEEE Society, within the same year, or is a previous EPS Fellowship winner is ineligible.

All Award nominations must be **online.** Nominations questions can be sent to the Society Awards Program director:

Eric Perfecto
Eric.Perfecto.US@ieee.org

Winners will be notified by April 2022, and the awards will be presented at the 72nd Electronic Components and Technology Conference (ECTC). **Date and venue will be announced when determined.**

Best Associate Editor Award

To recognize the work and efforts of our Associate Editors, EPS instituted the Best Associate Editor Award. The 2021 recipients are

Wendem Beyene—Facebook
Prof. Abhijit Chandra—Iowa State University
Cemal Basaran—SUNY at Buffalo
Xiaobing Luo—Huazhong Univ. of Science & Technology
Chuan Seng Tan—Nanyang Technological University
Paragkumar Thadesar—Qualcomm

MEMBERSHIP NEWS

IEEE Senior Membership: Are You In?

If you have been involved in the electronics packaging field for 10 years or more, chances are that you probably already have the necessary qualifications to be an IEEE Senior Member. Senior membership is the highest IEEE membership grade that can be applied for and is a recognition of sustained and significant performance in an IEEE-designated field. Individuals who are IEEE members can apply themselves for elevation to Senior Member or they can be nominated by others. Since a member can be nominated by someone else for Senior Membership, Society Chapters can play an important role in helping to identify and support applications for elevation. Nominating individuals in our Chapters is a great way to recognize their professional achievements and foster deeper personal and professional relationships with our peers. Individual members shouldn't hesitate to apply for Senior Member elevation on their own as well, and call upon their IEEE colleagues for support for their application. The requirements for Senior Member eligibility are very straightforward:

- The candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE-designated fields
- Candidates shall have been in professional practice for at least ten years
- Candidates shall have shown significant performance over a period of at least five of those years

As a member of EPS, the IEEE-designated field criteria will generally have been met. The criteria for ten years of professional practice can also take into account some portion of your educational experience as well as time spent in one's job or career, so a ten-year employment record isn't necessarily required. The final criteria of demonstrating significant performance over at least five of those ten years can be met in many different ways, including technical work, managerial responsibility, and publications to name a few. IEEE provides detailed information on the requirements for Senior Member grade at https://www.ieee.org/membership/senior/senior-requirements.html, along with sample cases that can be helpful for comparison to your own professional experiences.

Individuals applying for or nominating someone for Senior Member elevation can find additional information on the IEEE website at https://www.ieee.org/membership/grade-elevation.html and clicking on the Senior Member Grade link found there. Candidates applying for Senior Membership will need to supply three references from current IEEE members who are Fellows, Senior Members, or Honorary Members, and this is where EPS colleagues can support one another. Members of EPS chapters already have a group of local contacts that can help with nomination and reference support, simplifying and streamlining the process. Prospective applicants can find potential references through IEEE Collabratec via a link at the top of the EPS Membership page. There is also a link to the general Collabratec page on the MGA Senior Member Requirements page.

IEEE Senior Membership is a way for the Society to recognize the dedication and achievements of our members as well as a way to support our colleagues. If you have any questions about the Senior Membership application process or requirements, please don't hesitate to reach out to your local chapter or to us here at EPS for assistance.

Thanks
Alan Huffman, EPS VP Membership

The Value of Involvement in IEEE

For career growth, development, and expanding my network, I have found a lot of value in volunteering for and attending IEEE conferences. Specifically, I have been reviewing abstracts for IEEE's Electronic Components and Technology Conference (www.ectc.net), since 2001 as a part of the Packaging Technologies subcommittee. There is a lot of learning gained reviewing abstracts from cutting edge companies like Intel, TSMC, IBM, Qualcomm, Xilinx, etc. 8 months before publication. I am also able to meet wonderful people who I see every year at the abstract selection meeting in Dallas, TX, USA, in November. After 10 years of volunteering for ECTC, I was invited to join the Executive Committee to help organize the conference. This was a 7-year commitment resulting in me being General Chair in San Diego in 2015. This further expanded my network, but I stayed technical while on the EC by publishing 1 or more papers at the conference every year.

Along the way, I was invited to run for an IEEE Electronics Packaging Society (eps.ieee.org) Board of Governors seat and was part of the BOG from 2012–2020. My roles as VP of Education allowed me to propose new EPS Distinguished Lecturers, solicit

EPS Webinar topics, and create an EPS Certificate program for members' growth. I also had a motion approved to create an IEEE EPS Ph.D. Student Fellowship which has been available now for several years. As VP of Conferences, I was responsible for making sure our conference best practices were spread worldwide and was invited to attend events in Pisa, Italy and Kyoto, Japan. By instituting a Women's Panel at IEEE EPS' Flagship conferences, I was

able to travel to Grenoble and Dresden to Chair the panel in 2016 and 2018, respectively, as well as at ECTC in San Diego in 2015 and Las Vegas in 2016.

There are also a lot of opportunities for women to learn from each other through the Women In Engineering (wie.ieee.org) section. WIE hosts an International Leadership Conference (ieee-wie-ilc.org) in Silicon Valley each year as well as other regions around the world. I was very impressed by this conference when I attended the inaugural event in 2014 and then again 2015 where Intel CEO Brian Krzanich and AMD CEO Lisa Su spoke at the event. WIE differs from the Society of Women Engineers (SWE) because it caters specifically to women in the electronics industry.

I highly recommend getting involved in IEEE. Whether you want to review papers for a publication, attend a conference, be part of a committee, or just publish a paper, I can help you get started.

Best Regards,
Beth Keser, Ph.D.
beth.keser@intel.com

PUBLICATIONS NEWS

2020 CPMT Best Transactions Paper Awards

Each year, the Editors of the IEEE Transactions on Components, Packaging and Manufacturing Technology select the best papers published in the prior year. The papers are selected from among over 200 published papers and represent the best, based on criteria including originality, significance, completeness and organization.

Subscribers to this publication can access the papers on-line in IEEE Xplore at: http://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=5503870

Advanced Packaging Technologies Category
"Thin Film Metallization Stacks Serve as Reliable Conductors on Ceramic-based Substrates for Active Implants" Patrick Kiele, Paul Čvančara, Michael Langenmair, Matthias Mueller, Thomas Stieglitz; Volume 10, Issue 11, November 2020

Abstract:
Substrates and packages of active implantable medical devices are often fabricated from ceramics, such as alumina. Screen-printed PtAu paste is the state-of-the-art metallization for functional structures. Due to solid-state and liquid diffusion of Au during thermal exposure, solder times are limited. Otherwise, metal structures tend to delaminate. Moreover, it was shown that PtAu with solder fails after 37.4 years. We established a thin film metallization on the alumina process to overcome these disadvantages. We used sputtered platinum with an underlying adhesion layer made of tungsten-titanium to increase the adhesion strength of the alumina substrate. We avoided using gold in this work due to its high diffusion tendency. All used materials provided relatively low diffusion properties, which increases independence from joining techniques and mechanical longevity during use. Utilizing the Design of Experiment (DoE) methodology, we derived an optimal Pt thickness of 500 nm with 43 nm of WTi as an adhesion-promoting layer. After accelerated aging at 150 °C, corresponding to 125 years at body temperature (37 °C), the contact pad adhesion strength was 32.75 ± 7.08 MPa. This exceeded the safety limit of 17 MPa by far, set as a recommendation for robust screen-printing metallization processes. Soldering times of up to 120 s did not influence the adhesive strength. The new process reduced the minimum track distance to 50% of screen-printing values and is capable to be transferred into rapid prototyping techniques. It helps to make the assembly process independent of the manufacturing person in order to increase the yield of device fabrication and-most important in implantable device manufacturing-to make it more robust and thereby safer for the patient.

URL: https://ieeexplore.ieee.org/document/9205660

Components: Characterization and Modeling Category
"Experimental Study of Relationship between Arc Light Intensity and Temperature in Low Voltage Switching Devices" Dongkyu Shin, Thomas G. Bull, John W. McBride; Volume 10, Issue 11, November 2020

Abstract:
Arc motion in a quenching chamber has a significant influence on switching performance in a low-voltage switching device (LVSD). A high-speed optical arc imaging system (AIS) has been used to investigate the influence of the design parameters of a quenching chamber on arc motion. Arc light intensity is transmitted to the photodiodes of the AIS through optical fibers during the switching process. The AIS and associated software enable the detailed arc motion to be tracked inside the chamber at an image sampling rate of 1 MHz. Since higher arc temperature leads to greater radiation, it is assumed that the arc light intensity measured by the AIS is related to the arc temperature. However, there has been a little empirical study of the correlation between the arc temperature and light intensity measured by the AIS. In this article, the relationship between the arc temperature and light intensity is investigated by measuring arc spectra and arc images. Arc spectra are captured by a spectrometer when the arc is ignited by copper wire in a narrow enclosed chamber, and they are used to calculate the arc temperature by the Boltzmann plot method. At the same time, the AIS records the arc images from points adjacent to the fiber of the arc spectrometer. It is found that the arc light intensity measured by the AIS is directly related to the arc temperature; the correlation between the fourth power of temperature and the light intensity is an approximately linear trend.

URL: https://ieeexplore.ieee.org/document/9151104

Components: Characterization and Modeling Category

2020 "Steady-State Parametric Optimization and Transient Characterization of Heat Flow Regulation with Binary Diffusion" Tanya Liu, James W. Palko, Joseph S. Katz, Feng Zhou, Ercan M. Dede, Mehdi Asheghi, Kenneth E. Goodson; Volume 10, Issue 12, December 2020

Abstract:

Thermal regulators and switches are nonlinear devices that can greatly aid in the management of transient and/or spatially varying heating events. Various physical mechanisms have been harnessed to achieve nonlinear and switchable thermal behavior, though device characteristics are often evaluated in terms of steady-state performance only. Accurately capturing the transient behavior of these devices is a crucial missing link required for assessing the effectiveness of implementation in real-world scenarios. Here, we explore the physics of binary vapor diffusion through a noncondensable gas cavity as a promising mechanism for high-resistance contrast thermal regulation. Through a parametric steady-state optimization, we present a roadmap for future designs that can potentially reach switching ratios of up to 14.5. In addition, we perform a transient investigation to characterize the thermal response time of the device. The device possesses an extremely desirable attribute under certain transient heat loads, where the effective switching ratio appears significantly greater than the steady-state ratio due to a temporary increase in the OFF-state resistance immediately after switching. This work informs future experimental efforts for design optimization of binary-diffusion-based regulators and establishes simple modeling schemes to approximate device performance in system-level regulation scenarios.

URL: https://ieeexplore.ieee.org/document/9130141

Electronics Manufacturing Category:

2020 "Effects of Thickness and Crystallographic Orientation on Tensile Properties of Thinned Silicon Wafers"

Sangmin Lee, Jae-Han Kim, Young Suk Kim, Takayuki Ohba, Taek-Soo Kim; Volume 10, Issue 2, February 2020

Abstract:

Thinning silicon wafers for stacking in limited space is essential for the 3-D integration (3D!) technology of semiconductors. Due to the lack of research on the mechanical properties of thinned silicon wafers, it is difficult to assess and improve the mechanical reliability of 3D! semiconductor devices. This article reports the effects of thickness and crystallographic orientation on the tensile properties, such as Young's modulus, elongation, and strength, of the thinned silicon wafer. Tensile properties of a {100} silicon wafer are measured using a direct tensile testing system, where a digital image correlation method is adopted for accurate strain measurement. Femtosecond laser patterning for accurate shape control is used to fabricate dog-bone-shaped specimens with various thicknesses and crystallographic orientations. The effect of crystallographic orientation is investigated for (110), (320), (210), and (100) orientations. The Young's modulus of each orientation closely matches the theory of anisotropic elasticity. The surface energy ratios between crystallographic planes are calculated using fracture mechanics analysis. As the thickness decreases from 100 to 10 μm, the elongation and strength increase threefold, while Young's modulus is constant along the (110) direction. The strength results are analyzed with a Weibull statistical size effect model, where the Weibull modulus is calculated to be 2.35, which correlates strength only with thickness variation. Using this value and the Weibull size effect model, the expected strength of specific thickness can be calculated easily without additional experiments.

URL: https://ieeexplore.ieee.org/document/8778794

Most Popular T-CPMT Articles According to May 2021 Usage Statistics

A Review of 5G Front-End Systems Package Integration

Atom O. Watanabe; Muhammad Ali; Sk Yeahia Been Sayeed;
Rao R. Tummala; Markondeya Raj Pulugurtha
Publication Year: 2021, Page(s): 118–133

3-D Printed Metal-Pipe Rectangular Waveguides

Mario D'Auria; William J. Otter; Jonathan Hazell; Brendan T. W. Gillatt;Callum Long-Collins; Nick M. Ridler; Stepan Lucyszyn
Publication Year: 2015, Page(s): 1339–1349

Air Jet Impingement Cooling of Electronic Devices Using Additively Manufactured Nozzles

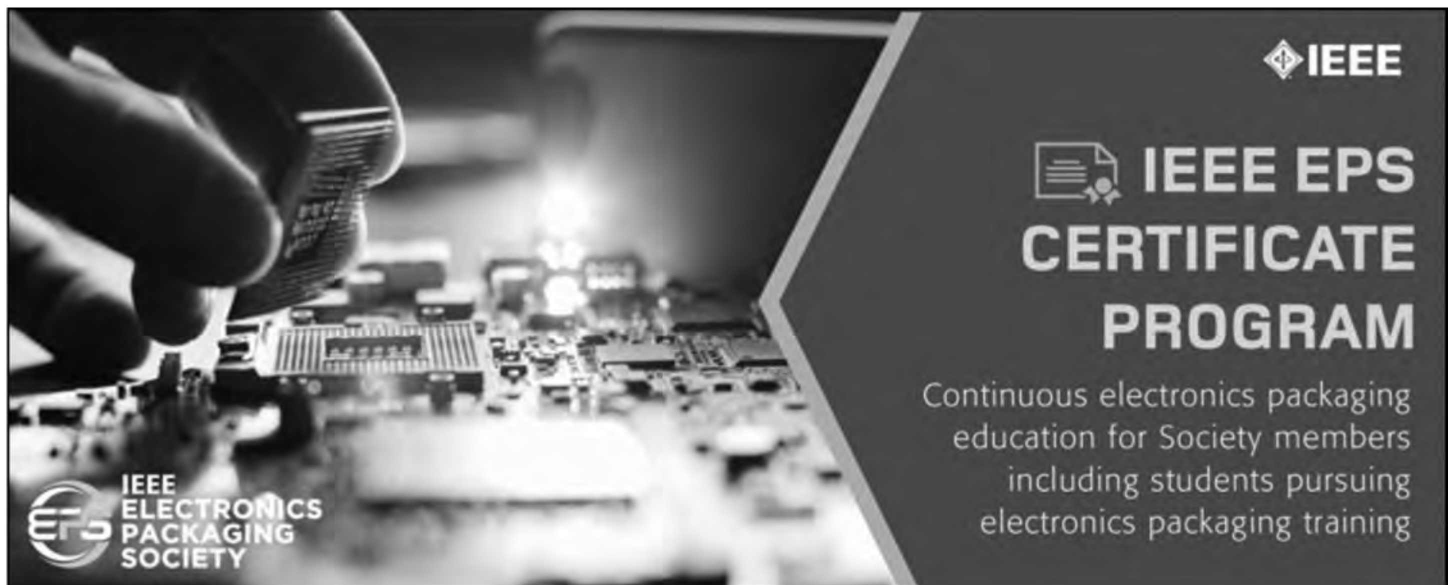
Beomjin Kwon; Thomas Foulkes; Tianyu Yang;
Nenad Miljkovic; William P. King
Publication Year: 2020, Page(s): 220–229

Power Delivery for High-Performance Microprocessors—Challenges, Solutions, and Future Trends

Kaladhar Radhakrishnan; Madhavan Swaminathan;
Bidyut K. Bhattacharyya
Publication Year: 2021, Page(s): 655–671

Silicon-Interconnect Fabric for Fine-Pitch (≤10 μm) Heterogeneous Integration

SivaChandra Jangam; Subramanian S. Iyer
Publication Year: 2021, Page(s): 727–738



Comprehensive EPS Certificate Program

The IEEE Electronics Packaging Society is pleased to announce that it has expanded its Certificate Program to include a new *EPS Distinguished Achievement Certificate*. This new level of recognition builds on the initial *EPS Achievement Certificate* aimed at early-career professionals, and provides a pathway for mid-career to late-career professionals to highlight their more advanced level accomplishments.

EPS Achievement Certificate

The EPS Certificate Program was initially established in January 2019 to encourage continuing education and professional development of EPS members. The original offering consisted of an *EPS Level One Achievement Certificate* that can be earned by completing 15 Professional Development Hours (PDHs) of continuing education in the area of electronics packaging. A variety of mechanisms exist to satisfy the continuing education requirement including attending online IEEE EPS Webinars (1 PDH per 1 hour webinar), attending registered Professional Development Courses (PDCs) at one of the EPS Conferences (ECTC, EPTC, and ESTC) (1 PDH per hour of PDC course attendance), authoring papers at EPS sponsored conferences and the IEEE CPMT Transactions that are published in IEEE Xplore (5 PDH per published conference/journal paper), and serving as a reviewer for IEEE CPMT Transactions papers (5 PDH per 3 reviews completed). Once an EPS member has achieved at least 15 PDHs through a combination of the above approaches, he/she can then self-nominate for the Certificate via an online form at https://eps.ieee.org/education/eps-certificate-program.html.

The first level *EPS Achievement Certificate* is aimed at early-career professionals working in the field of electronics packaging. It is especially intended to encourage the career development of young professionals including advanced graduate students. To date, over 25 EPS members have been recognized. Since there was an overwhelming response to the initial program, the EPS Vice President Education formed an adhoc Committee from members of the EPS Education Functional Team to further develop the Certificate Program. In particular, the goal was to add a new more advanced certificate that could capture an individual's technical growth, technical and service contributions, and other achievements. This process resulted in the establishment of a new *EPS Distinguished Achievement Certificate* that was recently approved by the EPS Board of Governors.

EPS Distinguished Achievement Certificate

This new level of recognition builds on the *EPS Achievement Certificate* that is earned by achieving 15 PDHs of continuing education, and provides a pathway for mid-career to late-career professionals to highlight their more advanced level continuing education and career accomplishments. The new *EPS Distinguished Achievement Certificate* will be awarded for advanced technical and service contributions to the industry and EPS. Two different categories of recognition are offered:

- Distinguished Achievement Certificate for Technical Leadership and Expertise
- Distinguished Achievement Certificate for Professional Engagement and Service

For either area of recognition, the nominee's strengths will be evaluated against prescribed criteria described in more detail below. As with the *EPS Achievement Certificate*, people interested in receiving the *EPS Distinguished Achievement Certificate* must self-nominate via an online Form. The nominee should first review the specific certificate requirements in each recognition area, and choose which one he/she wants to apply. The nominee should review the certificate requirements to assess themselves against the criteria and to prepare their supporting paperwork.

Distinguished Achievement Certificate for Technical Leadership and Expertise

There are five high-level focus areas for this new certificate. These areas include: (1) being recognized authority of technical expertise in one's field; (2) being a subject matter expert (SME) at conferences, keynotes, webinars, blogs; (3) demonstrating sustained technical contributions to industry; (4) documenting advanced technical recognitions; and, (5) being endorsed strongly by others. Examples of being a recognized authority of technical expertise include being an advanced member of the technical staff at a company (e.g. Fellow, Senior Technical Staff, Distinguished Engineer, etc.), making technical contributions as a Member or Fellow of professional associations/societies related to electronics packaging (e.g., IEEE, IMAPs, SMTA, ASME, etc.), and being an invited speaker at companies, technical conferences, and EPS Chapter meetings. Methods to demonstrate participation as a SME include abstracts accepted and papers presented at conferences, giving keynote lectures at conferences or professional society meetings, presenting webinars for EPS and other IEEE Societies, and serving on technical panels at conferences and other venues. Example approaches to demonstrate sustained technical contributions to industry include publishing well-cited technical papers at conferences and in journals, book chapters, and patents; serving as an editor of a journal or reference book; and being a leader or participant in industry blogs, focus groups, technical roadmaps, newsletters, and forums. Methods to document technical recognitions include receiving technical awards from a company, institute, professional society, or academic institution; being the acknowledged inventor of a seminal technology or process important to industry; serving as the point person for global high-level task force activity; and being elected to be a Member of an organization such as the US National Academy of Engineering, Royal Academy of Engineering, Chinese Academy of Engineering, IBM Academy of Technology, etc.

Distinguished Achievement Certificate for Professional Engagement and Service

There are four high-level areas of focus for this new certificate. These areas include: (1) demonstrating leadership in the electronics packaging field; (2) illustrating broad impact/influence in the electronics packaging field, (3) providing extensive service and "give back" to the profession and/or industry; and (4) being endorsed strongly by others. Leadership and broad impact activities in electronics packaging can be documented from outstanding accomplishments during industry employment or for notable volunteer contributions to the profession and society. Examples of significant professional service include serving as an officer in a technical society at the international, national, or local chapter level; participating in packaging related technical committees, councils, or affinity groups; contributing to technology roadmaps such as the Heterogeneous Integration Roadmap (HIR); and receiving a professional society or industry award based on service contributions. Documentation of "give-back" to one's technical community can be accomplished via demonstrations of coaching and mentoring of co-workers, young professionals, and students.

More details on the Certificate Program are available on the EPS website at https://eps.ieee.org/education/eps-certificate-program.html. The EPS Certificate Program is sponsored by the IEEE EPS VP Education and is offered only to EPS members. For questions, please contact Jeff Suhling (jsuhling@auburn.edu).

EPS Achievement Certificate

Congratulations to these EPS Members on receiving the IEEE Achievement Certificate from the IEEE Electronics Packaging Society and completing the required number of professional development hours.

Shaw Fong Wong, Intel Corporation
Jeffrey C. Suhling, Auburn Unviersity
Siddharth Ravichandran, Georgia Institute of Technology
Agneta Elisabet Ljungbro, Ericsson AB
Omkar Gupte, Georgia Institute of Technology
Joseph Soucy, Charles Stark Draper Laboratory
Chandrasekharan Nair, Intel Corporation
Chintan Buch, Applied Materials Inc.
Atom Watanabe, Georgia Institute of Technology
Vidya Jayaram, Intel Corporation
Chris Bailey, University of Greenwich
Anil B. Lingambudi, IBM
Shuye Zhang, Harbin Institute of Technology
Ralph Remsburg, University of Hertfordshire

EPS Resource Center

The IEEE EPS Resource Centers contains valuable, technical content from reputable experts to enhance research or industry work, implement trainings, or earn CEU/PDH credits--all of which are universally available on demand.

IEEE EPS Resource Centers benefits include:

- Access to valuable technical community content
- Access to content 24 hours a day, 7 days a week through an easy-to-use global portal
- Available at no cost for EPS members
- Opportunities to earn CEUs and PDHs

Top webinars:

- The Evolution of Lead-Free Solder Alloy
- Heterogeneous Integration Roadmap (HIR) Chapter 20 Thermal Management
- Heterogeneous Integration Roadmap (HIR) Chapter 10 Integrated Power Electronics
- Heterogeneous Integration Roadmap (HIR) Chapter 6 Aerospace & Defense
- Heterogeneous Integration Roadmap (HIR) Chapter 9 Integrated Photonics

https://resourcecenter.eps.ieee.org/

EPS Distinguished Lecturer Program

EPS Distinguished Lecturers are selected from among EPS Fellows, Award winners, and Society leaders, who are members of the technical community and experts in their field. They are available to present lectures and/or courses at EPS events—Chapters, Conferences, Workshops or Symposia; as well as IEEE Student Chapter events.

The EPS Distinguished Lecturer Program (DLP) aims at serving communities interested in the scientific, engineering, and production aspects of materials, component parts, modules, hybrids and micro-electronic systems for all electronic applications.

The Program strives to support EPS Chapters worldwide by helping them to invite leading researchers in their respective fields and IEEE Student Chapters to encourage students to pursue EPS related fields and to join the EPS society. The DLP talk is a major event in the life of the inviting Chapter.

EPS Distinguished Lecturers

Ramachandra Achar, Ph.D. (7/1/2020–6/30/2024)
Department of Electronics, Carleton University
Ottawa, Ontario, CANADA
Topics: CAD tools and methodologies for interconnects, packages, and systems with an emphasis on signal, power and EMI integrity

Mudasir Ahmad, (6/2021–12/2021)
Cisco Systems, Inc.
San Jose, CA USA
Topics: Internet of Things (IoT), Advanced Packaging, 2.5D, Heterogeneous Silicon Photonics, Advanced Reliability (Thermomechanical, Mechanical Shock), Numerical Modeling, Advanced Thermal Solutions, Stochastic Analysis, Bayesian Inference, Machine Learning, Artificial Intelligence

Kemal Aygün, Ph.D. (7/1/2020–6/30/2024)
Intel Corporation
Chandler, AZ USA
Topics: Package/socket/board/interconnect technologies, electrical simulation methodology and lab metrologies

Muhannad Bakir, Ph.D. (1/2020–1/2024)
School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, GA USA
Topics: Emerging interconnection architectures and technologies; heterogeneous system design and integration

W. Dale Becker, Ph.D. (7/1/2020–6/30/2024)
IBM
Poughkeepsie, NY USA
Topics: Electronic Package design and integration, system design, electrical modeling tools

Wendem Beyene, Ph.D. (7/1/2020– 6/30/2024)
Intel Corporation
San Jose, CA
Topics: Electrical modeling and simulation techniques for analysis of interconnects, packages, and systems. Machine learning techniques

Karlheinz Bock, Ph.D. (7/2020–7/2024)
Technische Universität Dresden
Dresden, Germany
Topics: Multifunctionality & heterosystemintegration & additive manufacturing (IoT, Industry 4.0, tactile internet), packaging for mechanical, digital and power co-integration (automotive, machines, robots..),2.5D and 3D electro-optical-RF interposer and board (high performance), heterointegration for flexible, bio, organic and large area electronics (open form factor)

Bill Bottoms, Ph.D. (6/2021–6/2025)
Third Millennium Test Solutions
Santa Clara, CA USA
Topics: Heterogeneous Integration, Semiconductor test technology, Emerging research materials, Packaging of electronic components and systems, the global network and its future requirements, the internet of things and Smart manufacturing

Chris Bower, Ph.D. (6/2021–6/2025)
X-Celeprint Inc.
North Carolina, USA
Topics: novel assembly methods, elastomer stamp micro-transfer-printing, heterogeneous integration, three-dimensional integration, manufacturing of micro-assembled displays and other large-format electronics.

William T. Chen, Ph.D. (1/2020–1/2024)
ASE (U.S.) INC
Santa Clara, CA USA
Topics: Semiconductor and Electronics Industry Trends and Roadmap

Xuejun Fan, Ph.D. (1/2020–1/2024)
Department of Mechanical Engineering
Lamar University
Beaumont TX USA
Topics: Design, modeling and reliability in micro-/nano- electronic packaging and microsystems

Philip Garrou, Ph.D. (1/2020–1/2024)
Microelectronic Consultants of North Carolina
Research Triangle Park, NC USA
Topics: Thin film technology; IC packaging and interconnect; Microelectronic materials; 3D-IC integration

Madhu Iyengar, Ph.D. (7/1/2020–6/30/2024)
Google
Mountain View, CA
Topics: Thermal component and system design for packages, servers, and data centers.

Subu Iyer, Ph.D. (6/2021–6/2025)
University of California, Los Angeles
Los Angeles, CA USA
Topics: Heterogeneous Integration; Flexible hybrid electronics; 3D interposer, and wafer scale integration and stacking\

Beth Keser, Ph.D. (1/2020–1/2024)
Intel San Diego, CA USA
Topics: Fan-Out Wafer Level Packaging and Wafer Level Packaging structures; processes, materials, tools, design rules and roadmaps; photoimageable liquid polymer films

Pradeep Lall, Ph.D. (1/2020–1/2024)
Auburn University
Auburn, AL, USA
Topics: Semiconductor Packaging, Modeling and Simulation, Reliability in Harsh Environments, Shock/Drop/Vibration, Cu Wirebonding, Flexible Hybrid Electronics, Additive Manufacturing, Prognostics and Health Management, LEDs, Micro CT Measurements

John H. Lau, Ph.D. (1/2020–1/2024)
ASM Pacific Technology
Hong Kong
Topics: Electronics and Photonics 2D and 3D packaging and manufacturing

Ravi Mahajan, Ph.D. (7/2020–7/2024)
Intel Corporation
Arizona, USA
Topics: Advanced Packaging Architectures, Assembly Processes and Thermal Management

James E. Morris, Ph.D. (1/2020–1/2024)
Department of Electrical and Computer Engineering
Portland State University
Portland, Oregon USA
Topics: Electrically conductive adhesives; Electronics packaging; Nanotechnologies

Mervi Paulasto-Kröckel, Ph.D. (7/2020–7/2024)
Aalto University
Helsinki, Finland
Topics: MEMS, electronics reliability, automotive components and packaging, implantable electronics, dissimilar materials & interfaces

Eric D. Perfecto, (1/2020–1/2024)
IBM Research
Poughkeepsie, NY USA
Topics: Fine pitch interconnect, chip to chip and chip to laminate connection, UBM and solder selection, chip package interaction and 2.5D fabrication

Mark Poliks, Ph.D. (1/2020–1/2024)
Binghamton University (SUNY)
Binghamton, NY USA
Topics: Materials and Processes, Advanced Manufacturing, Flexible Hybrid Electronics, High Speed and Additive

Jose Schutt-Aine, Ph.D. (1/2020–1/2024)
University of Illinois
Champaign, IL, USA

Topics: High-Frequency Measurements, Mixed-Signal Design, High-Performance Computing, electromagnetic Modeling, Signal Integrity, CAD Tools for Interconnects and Packages, Machine Learning for High-Speed System Modeling

Nihal Sinnadurai, (1/2020–1/2024)
Suffolk IP11 9RZ UK
Topics: Accelerated Ageing for Reliability Assurance -theory and practical methods - including HAST (my invention originally); The use of encapsulation and plastic packaging and reliability evaluation method; PCB & Hybrid technologies; Thermal management and design

Ephraim Suhir, Ph.D. (1/2020–1/2024)
Los Altos, CA 94024 USA
Topics: Accelerated life testing; Probabilistic physical design for reliability; Bonded assemblies; Thermal stress; Predictive modeling; Fiber optics structures: design for reliability; Dynamic response to shocks and vibrations

Chuan Seng Tan, Ph.D. (6/2019–6/2023)
Nanyang Technologica University
Singapore
Topics: 3D Integration and packaging, Fine Pitch Cu-Cu Bonding Through Silicon Vias (TSVs), Group IV Semiconductors: Material Growth, Engineered Substrates, and Device Applications

Rao Tummala, Ph.D. (1/2020–1/2024)
Microsystems Packaging Research Center (PRC)
Georgia Institute of Technology
Atlanta, GA USA
Topics: Electronics Packaging

E. Jan Vardaman, (1/2020–1/2024)
TechSearch International, Inc.
Austin, TX USA
Topics: International developments in semiconductor packaging, manufacturing and assembly; SiP: Business and technology Trends; drivers in advanced packaging; Flip chip and wafer level packaging

Paul Wesling, (1/2020–1/2024)
Saratoga, CA USA
Topics: Origins of Silicon Valley and the Electronics Packaging Society; the IEEE/SEMI/ASME Heterogeneous Integration Roadmap and how to use it (as editor for the 2019 Roadmap).

C.P. Wong, Ph.D. (1/2020–1/2024)
Georgia Institute of Technology
Atlanta, GA, USA
Topics: Materials

Jie Xue, Ph.D. (1/2020–1/2024)
Cisco Systems, Inc
San Jose, CA, USA
Topics: Advanced Packaging for Networking Application; Impact of Internet of Everything (IoE) to Semiconductor Industry eco-system; High performance substrate technologies; Trends and challenges of Silicon Photonics for datacenter and networking applications

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President's Column

(*Continued from page 1*)

to our activities on the HIR, our Technical Committees, or our chapters. If you have any questions or wish to share your assessment of our efforts with me, please do not hesitate to contact me at c.bailey@gre.ac.uk.

Finally, I look forward to working with the EPS Board of Governors, Staff, and our volunteers throughout 2021 to deliver our strategic goals and continue to provide the unique service that IEEE EPS can offer you, our members, and our industry. I hope you enjoy reading this edition of the newsletter and find time to relax and enjoy the summer holidays. Please stay safe and well, and I look forward to meeting you again in person at one of our future events.

Chris Bailey

The 71th ECTC Virtual Conference—Amazing Online Participation from the Community

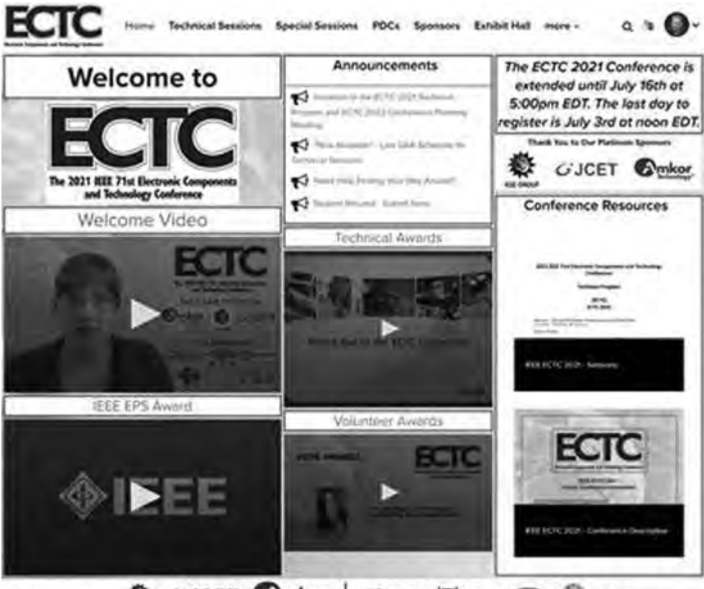
Submitted by
Florian Herrault, Assistant Program Chair, IEEE ECTC 2022

This year's IEEE Electronic Components and Technology Conference (ECTC) was held virtually from June 1 to July 16, 2021. The conference brought together over 1,300 industry professionals, academics, and students in attendance from 23 countries.

The virtual conference format gave us a unique opportunity to provide not one but two amazing keynote sessions, and a series of special sessions and panels that had a pre-recorded and a live component. The ECTC ExCom team worked closely with IEEE MCE to organize the conference on the Engagez virtual platform. The events were first live broadcasted using pre-recorded segments from the participants, and followed by a live Question & Answer portion. ECTC attendees were able to submit their questions during the live broadcast of the pre-recorded segments and the live Q/A segment. Most live Q/A sessions were held between June 21 and July 1st. The entire event (pre-recorded and live Q/A segments) was then made available for on-demand viewing until the end of the conference.

The conference included 346 papers in 46 oral sessions. There were 14 special sessions. The Heterogeneous Integration Roadmap workshop was integrated into the ECTC platform, providing a similar experience to the in-person conference. The professional development courses drew 251 attendees for 14 sessions. 43 sponsors supported the conference. This year's Technology Corner Exhibit featured 61 exhibits.

Preparations for the 71st ECTC started last October, when the Executive Committee announced ahead of the abstract submission deadline that the conference would be held virtually. Our professional volunteers serving in the technical sub-committees reviewed 489 submitted abstracts with a near even split between submissions from academic and industry. The number of submitted abstracts was on par with our in-person conferences. Ultimately, 71% of the submitted abstracts were accepted, leading to 347 presentations at the conference. In a testimony to the diversity of the industry and the conference, abstracts were received from 24 countries with the Unites States, Taiwan, and South Korea leading the way in number of abstract submissions.



71st ECTC Virtual Platform

Building upon last year's successful virtual conference, and based on the limited information we had at the time, the ECTC executive committee took an early decision in October 2020 to host the 2021 ECTC on a virtual platform. Making the decision early allowed the team to deliver a best-in-class virtual conference experience to our loyal community. The conference program came together at the virtual Technical Program Committee's annual planning meeting on November 20, 2020. The technical subcommittee chairs and session chairs did an excellent job developing interesting sessions and communicating with their session authors, which enabled all the manuscripts to be publication-ready well before the start of the virtual conference. The session chairs reviewed the submitted manuscripts prior to final acceptance. ECTC again used the IEEE Computer Society Conference Publishing Services to receive and process manuscripts. As in previous years, the IEEE CrossCheck system was used to ensure that all of the ECTC manuscripts maintain a high level of original content.

During the first day of the conference (on June 1st), attendees were able to tune in for any of the on-demand 346 presentations and browse the exhibit corner. They were also able to enjoy an excellent keynote presentation from Sam Naffziger, AMD Senior Vice President, Corporate Fellow, and Product Technology Architect. The presentation focused on the impact of chiplet-based SOC architectures and manufacturing from a packaging perspective for computing applications. Over 500 attendees watched Sam's presentation.

From June 2 through June 9, we had the pleasure to attend a series of special sessions, special panels, and plenary presentations. Following up on Sam's keynote presentation, Kanad Ghose—Binghamton University, Dale Becker—IBM, invited a panel of experts to discuss the opportunities and challenges of the chiplet designs and applications. The panel discussed both technical and business challenges (deployment, sourcing, security, trade-offs between thermal, warpage and electrical performance).

Rozalia Beica—AT&S and Ed Sperling—Semiconductor Engineering—hosted a special panel on the evening of June 2nd to evaluate the market terends and geopolitical and economic outlook in the semiconductor industry. The business centric panel discussion was very informative with an emphasis on geopolitical uncertainties, and impact on the global supply chain in microelectronics packaging.

On June 3rd, Jan Vardaman—TechSearch International, Inc., Mark D. Poliks—Binghamton University, and Kimberly Yess—Brewer Science, Inc. hosted a Plenary session with a panel of 7 experts on the transformation of the electronics industry in a Post-COVID world. As was pointed out during the discussion,

the electronics industry continues to experience growth, driven by society changes resulting from the global pandemic. Growth in datacenters, the use of artificial intelligence, and increased use of telemedicine has been accelerated by the pandemic and with changing lifestyles this growth may continue. Out-of-season demand for game consoles, commercial and educational laptops and tablets, monitors, and other electronics has been driven directly by the pandemic. Supply chains and material availability have also been disrupted and with renewed growth for vehicles sales, automotive electronics has entered a new phase. This panel discussed the continued transformation of the industry and expectations that will drive packaging developments in the future.

To finish our first week of events, Dave Armstrong—Advantest, and Robert Patti—Nhanced Semiconductors, chaired an excellent ECTC Special Session on June 4th, on the topic of test challenges in the area of heterogeneous integration, mentioning that this topic has not gathered the attention it deserved in the past, despite being a key element of making heterogeneous integration mainstream.

On June 7, Chris Bailey—EPS President, University of Greenwich, and Sam Karikalan—EPS VP Conferences, Broadcom, hosted the EPS President's Panel to provide industry perspective on the future vision of electronics packaging. Panelists from AMD, Facebook, Intel, and Marvell Semiconductor gave the attendees insights into the semiconductor industry's position, particularly from companies that use advanced electronics packaging in their products. These are exciting times for the electronics packaging community where advanced packaging and heterogeneous integration technologies are seen as key product differentiators. This panel session will hear from several leading companies who will discuss their future vision for advanced electronics packaging.

Later in the day, Kevin Byrd—Intel and Keith Newman—AMD chaired a ECTC Special Session on Low Temperature Solder (LTS) and the packaging challenges of next-generation SMT interconnects. Low temperature solder (LTS) systems, previously considered as a Pb-free replacement for PbSn, have now been introduced in select production applications due to different factors: sub-200˚C processing temperatures create opportunities for significant reductions in component warpage, thermal stress of substrates, and thermal impact to device reliability. This session highlighted LTS research areas most critical to component suppliers to improve compatibility with surface mount technology (SMT) LTS processing and to enhance solder joint reliability. Topics presented during this session focused on plating surfaces, heterogeneous vs. homogeneous solder joint construction, and solder materials design, amongst others.

On June 8, Karsten Meier—TU Dresden, and Przemyslaw Gromala—Robert Bosch GmbH, chaired a ECTC Special Session on Materials and Technologies for Advanced Packaging (5G, RF, Power, Harsh Environment) with an expert panel from Europe and USA. The thermal challenges associated with heterogeneous integration and tightly-packed microelectronic components was one of the key takeaways of this inspiring session.

On June 9, Kotlanka Rama Krishna—Analog Devices and Ahyeon Koh—Binghamton University hosted a panel of experts for an ECTC Special Session focusing on the home-use medical devices and packaging in wearable technologies. This session focused on some of the challenges associated with packaging sensors and the electronic signal chain into these emerging, at-home clinical-grade wearables.

On June 10, ECTC welcomed for the first time ever its second keynote speaker, in part due to the month-long virtual conference

ECTC Special Session on Materials and Technologies for Advanced Packaging

format. Pedro Arsuaga, Renewable Energy Business Program Manager, GE Research, gave an inspiring talk on the transition taking place from fossil fuel based power generation to renewable energy based power generation. This energy transition is shaking the foundation of how the grid was created and has been operating for the last century, as both wind and solar technologies connect to the grid using power electronics.

On June 10, the IEEE EPS Seminar, chaired by Yasumitsu Orii—NAGASE and Shigenori Aoki—LINTEC, focused on emerging high-bandwidth optical networks and how latency can impact the system performance.

Chris Bower—X Display Company and Mark Beranek—NAVAIR chaired an ECTC Special Session on Pathogen Detection & Eradication on June 11. The session focused on Photonics and Photonics packaging solutions for safely detecting and eradicating pathogens on surfaces and spaces. This session was particularly impactful considering the positive impact that pathogen detection sensors and eradication components can have on public health. A path-forward plan aimed at initiating future research in the areas of photonics and photonics packaging for pathogen detection and eradication was given by 6 expert panelists.

ECTC also hosted the Heterogeneous Integration Roadmap Workshop on-demand. Bill Chen (ASE) and Bill Bottoms (3MTS) hosted the event which was divided into 4 sessions consisting of 23 technical groups: Session 1: High Performance Computing & Data Centers; 2D-3D & Interconnect; Thermal Management; Integrated Photonics; Test & Cyber Security. Session 2 Automotive; MEMS & Sensors Integration; SiP & Module; Supply Chain; Integrated Power Electronics. Session 3: 5G & Future Communications; WLP (Fan-in & Fan Out); Aerospace & Defense; Mobile; Materials & Emerging Research Materials; IOT; and Session 4: Medical, Health & Wearables; Emerging Research Devices; Single Chip and Multi Chip Integration; Co-Design; Modeling & Simulation; Reliability. The half-day pre-recorded event was followed by live feedback.

The 2021 ECTC Professional Development Courses provided a good representation of topics of interests for Electronic Packaging Technologists. Each of the courses were presented by world-class experts, enabling participants to broaden their technical knowledge base. As in previous years there were 14 courses, each 2.5 hours long. Each PDC occurred within the 1st two weeks of the conference, and were made available on demand for the PDC registrants until the end of the presentation. As in the past CEU/PDH credit were provided at no expense to the attendee upon request.

71st ECTC Keynote Session #2 – Perdo Arsuaga from GE Research at the start of his virtual presentation

Awards for best and outstanding papers from last year's 2020 ECTC, both in oral presentation sessions and interactive sessions, were presented by the ECTC 2021 ECTC Vice General Chair, Rozalia Beica, and posted on the frontpage of the ECTC virtual platform. Also presented was the Intel Best Student Paper Award for ECTC 2020.

1) Best Session Paper
InFO_SoW (System-on-Wafer) for High Performance Computing
Shu-Rong Chun, Tin-Hao Kuo, Hao-Yi Tsai, Chung-Shi Liu, Chuei-Tang Wang, Jeng-Shien Hsieh, Tsung-Shu Lin, Terry Ku, Douglas Yu—Taiwan Semiconductor Manufacturing

2) Best Interactive Presentation Paper
Embedded 3D-IPD Technology based on Conformal 3D-RDL: Application for Design and Fabrication of Compact, High-Performance Diplexer and Ultra-Wide Band
Ayad Ghannam, Alessandro Magnani, David Bourrier, Thierry Parra—3DiS Technologies

3) Outstanding Session Paper
10 and 7 µm Pitch Thermo-Compression Solder Joint, Using a Novel Solder Pillar and Metal Spacer Process
Jaber Derakhshandek, Giovanni Capuz, Vladimir Cherman, Funnihiro Inoue, Inge De Preter, Lin Hou, Pieter Bex, Carine Gerets, Fabrice Duval, Thomas Webers, Julien Bertheau, Stefaan Van Huylenbroeck, Alain Phommahaxay, Ehsan Shafahian, Geert Van der Plas, Eric Beyne, Andy Miller, Gerald Beyer—IMEC

4) Outstanding Interactive Presentation Paper
Processing Glass Substrate for Advanced Packaging Using Laser Induced Deep Etching
Rafael Santos, Jean-Pol Delrue, Norbert Ambrosius, Roman Ostholt, Stephan Schmidt—LPKF Laser & Electronics AG

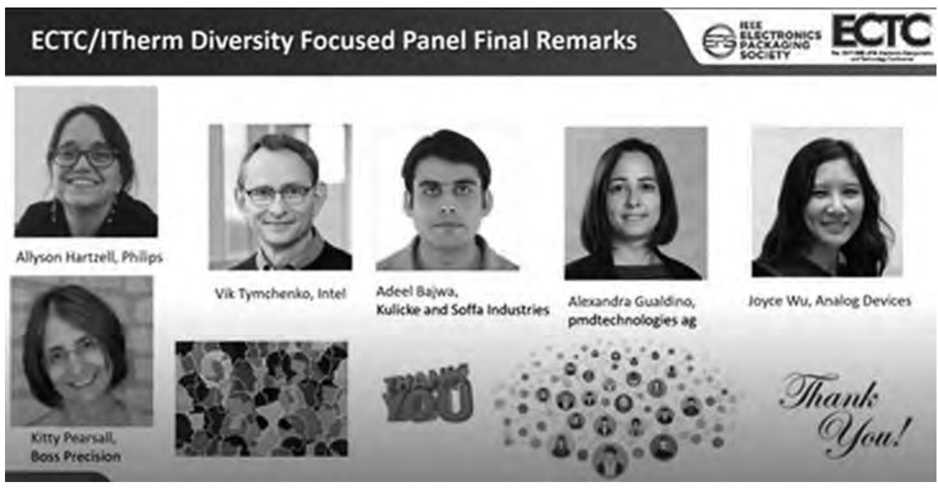
5) Intel Best Student Session Paper
A Comprehensive Study of Electromigration in Lead-free Solder Joint
Jiefeng Xu, Chongyang Cai, Vanlai Pham, Ke Pan, Huayan Wang, Seungbae Park—Binghamton University

2020 ECTC Best Paper Awards

The Technology Corner exhibit area was accessible virtually with 61 exhibitors. Exhibitors had multiple resources available within their virtual booth, offering virtual introductions, brochure materials, staff contact information, and an opportunity to submit inquiries and discuss directly with exhibit members.

The 71st ECTC had 61 exhibitor booths at the Virtual Technology Corner.

We hosted three amazing events to support diversity, women in engineering and science, and young professionals. On June 9, co-sponsored with iTHERM, Allyson Hartzell from Philips and Kitty Pearsall from Boss Precision, Inc. hosted the Diversity Panel. The panel was composed of Joyce Wu, Analog Devices, Viktor Tymchenko, Intel, Alezandra Gualdino, PMD Technologies and Adeel Bajwa, Kulicke and Soffa Industries, Inc.. The panel focused on how gender equality trends, ethnic and cultural diversity can boost business performance.



The diversity session panel during ECTC 2021

On June 10, Jean Trewhella, Globalfoundries, Sr. Past President of EPS and 2010 ECTC General Chair, and Tanja Braun, Fraunhofer IZM, EPS BOG Member and Women in Engineering (WIE) Delegate, held a virtual Women's Luncheon Table event.

On June 11, Yan Liu, Medtronic, and Adeel Bajwa, Kulicke and Soffa, hosted the ECTC Young Professionals Meetup event with panel contributions from Kitty Pearsall and Prof. Subramanian Iyer from UCLA. In this active event, students interacted with senior EPS members and professionals through a series of active and engaging activities, having opportunities to learn more about packaging-related topics, ask career questions, and meet some professional colleagues.

Prof. Subramanian Iyer talking to a group of students during the Young Professionals Meetup

Overall, the 71st ECTC was a unique experience but really showed how strong the packaging community is. Despite the virtual format, we had a very strong exhibitor presence, excellent sponsorship, and number of high-quality technical presentations and excellent presentation attendance. The ECTC Executive Committee sincerely thanks all the attendees, exhibitors, and conference sponsors for their support as well as all the committee members and chairs who are volunteering their time to help organize the sessions and make ECTC such a success every year. Special thanks also to our event management team and to MCE for developing our virtual platform.

The 72nd ECTC will be held at Sheraton San Diego Hotel & Marina, San Diego, California, May 31–June 3, 2022. Rozalia Beica from AT&S will be the General Chair of this conference. The Call for Papers and PDC Proposals will be available at www.ectc.net, and the abstract submission will close on October 4, 2021. So get those abstracts ready and submit them as soon as abstract submission opens online.

We are looking forward to see you all in San Diego in 2021, and restart our in-person sessions, speaker breakfasts, our gala and networking events, and other opportunities to interact with our colleagues from the Packaging community!

Top Conference Papers Based on Usage

2020 IEEE 70th Electronic Components and Technology Conference (ECTC)

(June 3–30, 2020)

InFO_SoW (System-on-Wafer) for High Performance Computing
Shu-Rong Chun; Tin-Hao Kuo; Hao-Yi Tsai; Chung-Shi Liu; Chuei-Tang Wang; Jeng-Shien Hsieh; Tsung-Shu Lin; Terry Ku; Douglas Yu

Die to Wafer Stacking with Low Temperature Hybrid Bonding
Guilian Gao; Thomas Workman; Cyprian Uzoh; K. M. Bang; Laura Mirkarimi; Jeremy Theil; Dominik Suwito; Rajesh Katkar; Gill Fountain; Gabe Guevara; Bongsub Lee

Magnetic Inductor Arrays for Intel® Fully Integrated Voltage Regulator (FIVR) on 10th generation Intel® Core™ SoCs
Malavarayan Sankarasubramanian; Kaladhar Radhakrishnan; Yongki Min; William Lambert; Michael J Hill; Ashay Dani; Ryan Mesch; Leigh Wojewoda; Jose Chavarria; Anne Augustine

Scalable Chiplet Package Using Fan-Out Embedded Bridge
Joe Lin; C. Key Chung; C. F. Lin; Ally Liao; Ying Ju Lu; Jia Shuang Chen; Daniel Ng

Ultra High Density SoIC with Sub-micron Bond Pitch
Y. H. Chen; C. A. Yang; C. C. Kuo; M. F. Chen; C. H. Tung; W. C. Chiou; Douglas Yu

2020 19th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)

(July 21–23, 2020)

Embedded Microchannel Cooling for High Power-Density GaN-on-Si Power Integrated Circuits
Remco van Erp; Georgios Kampitsis; Luca Nela; Reza Soleimanzadeh Ardebili; Elison Matioli

3D Wafer-to-Wafer Bonding Thermal Resistance Comparison: Hybrid Cu/dielectric Bonding versus Dielectric via-last Bonding
Herman Oprins; Vladimir Cherman; Tomas Webers; Soon-Wook Kim; Joeri de Vos; Geert Van der Plas; Eric Beyne

Coupled Electro-Thermal Analysis of Permanent Magnet Synchronous Motor for Electric Vehicles
Amitav Tikadar; Nitish Kumar; Yogendra Joshi; Satish Kumar

Additively Manufacturing Nitinol as a Solid-State Phase Change Material
Darin J. Sharar; Adam A. Wilson; Asher Leff; Andrew Smith; K. Can Atli; Alaa Elwany; Raymundo Arroyave; Ibrahim Karaman

Topology Optimization of Manifold Microchannel Heat Sinks
Yuqing Zhou; Tsuyoshi Nomura; Ercan M. Dede

2020 8th Electronic System-Integration Technology Conference (ESTC)

(September 15–18, 2020)

Manufacturing of High Frequency Substrates as Software Programmable Metasurfaces on PCBs with Integrated Controller Nodes
D. Manessis; M. Seckel; L. Fu; O. Tsilipakos; A. Pitilakis; A. Tasolamprou; K. Kossifos; G. Varnava; C. Liaskos; M. Kafesaki; C. M. Soukoulis; S. Tretyakov; J. Georgiou; A. Ostmann; R. Aschenbrenner; M. Schneider-Ramelow; K-D. Lang

Reliability Testing of FCCSP Packages for Automotive Applications
Karsten Meier; Laura Wambera; Bjoern Boehme; Christian Goetze; Simone Capecchi; Jens Paul; Marcel Wieland; Karlheinz Bock

Thermal Evaluation of Metalized Ceramic Substrates for use in Next-Generation Power Modules Toward International Standardization
Naoki Wakasugi; Chuantong Chen; Kiyoshi Hirao; Shijo Nagao; Katsuaki Suganuma

Cu Pillar Based Advanced Packaging, for Large Area & Fine Pitch Heterogeneous Devices
Abdenacer AIT MANI; Nohora CAICEDO; Nadia MILOUD-ALI;François LEVY; Fréderic BERGER; Thierry MOURIER; Tarik CHAIRA; Natacha R APHOZ; Alexis BEDOIN; Patrick PERAY; Mireille FRANCOU; Alain GUEUGNOT; Laura BOUTAFA; David HENRY

Interconnections of Low-Temperature Solder and Metallizations
YiWun Wang; C. Robert Kao

2020 IEEE 22nd Electronics Packaging Technology Conference (EPTC)

(December 2–4, 2020)

Wafer Level Back to Back Hybrid Bonding for Multiple Wafer Stacking
H. Y. Li; M. Kawano; L Ji; H. M. Ji; C. S. Lim

Wafer Level Fine-Pitch Hybrid Bonding: Challenges and Remedies
Vivek Chidambaram; Yew Wing Leong; Qin Ren

Lidless and Lidded Flip Chip Packages for Advanced Applications
Gamal Refai-Ahmed; Huayan Wang; Suresh Ramalingam; Nagadeven Karunakaran; Ke Pan; SB Park; Alegesen Soundarajan; Sreedharan Kelappen Kanaran; C. Key Chung; Yu Lung Huang

Impact of Process Variations on the Capacitance and Electrical Resistance down to 1.44 µm Hybrid Bonding Interconnects
B. Ayoub; S. Lhostis; S. Moreau; E. Leon Perez; J. Jourdon; P. Lamontagne; E. Deloffre; S. Mermoz; C. de Buttet; V. Balan; C. Euvard; Y. Exbrayat; H. Frémont

An Automatic Chip-Package Co-Design Flow for Multi-core Neuromorphic Computing SiPs
Jingjing Lan; Vishnu P. Nambiar; Rheeshaalaen Sabapathy; Rahul Dutta; Chai Tai Chong; Mihai Dragos Rotaru; Kuang Kuo Lin; Surya Bhattacharya; Kevin Tshun Chuan Chai; Anh Tuan Do

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2021 Conferences Status

With the health and safety of our members and participants being our first priority, please know that our thoughts are with those affected by the COVID-19 outbreak.

We are closely monitoring the developments related to this pandemic and working diligently with the IEEE and our conference organizing committees worldwide, on our preparedness.

The following is the current status of the EPS sponsored conferences for the remainder of 2021. As the situation keeps changing dynamically, please reference the EPS Conference webpage for weekly updates

Conferences financially sponsored/co-sponsored by the EPS:	
IEMT	Canceled
ESTC	Not held in 2021
ICEPT	In-person Event Xiamen, China Aug 11–14, 2021
IWIPP	Biennial—Postponed to Aug 24–26, 2022
DTIP	Virtual Event Aug 25-27, 2021
EMPC	Virtual Event, Sept 13–16, 2021
THERMINIC	In-person Event Berlin, Germany Sept 22–24, 2021
EOS/ESD Symposium	In-person Event Tuscon, AZ Sept 26–Oct 1, 2021
EPEPS	Virtual Event Austin, TX Oct 17–20, 2021
QCE	Virtual Event Oct 18–22, 2021
IMPACT	In-person Event Taipei, Taiwan Oct 20–22, 2021
HOLM	In-person Event San Antonio TX Oct 24–27, 2021
COMCAS	In-person Event Tel Aviv, Israel Nov 1–3, 2021
ICSJ	Hybrid Event Kyoto, Japan Nov 10–12, 2021
3DIC	Hybrid Event Raleigh, NC Nov 15–18, 2021
SSLChina: IFWS	In-person Event Shenzhen, China Nov 28–30, 2021
EPTC	Virtual Event Dec 1–3, 2021
EDAPS	Virtual Event Urbana, IL Dec 13–15, 2021

Research and Development on Reliability in Europe—status and next steps

High Level Introduction About R&D on Future of Micro- Nano-Electronics Reliability (an European perspective)

In Europe, reliability is seen as a major driver for CO_2 reduction and as key enabler of a greener society. Many of the new concepts can only be turned into saleable products if their electronics components and systems have outstanding reliability performance. Autonomous driving, cooperative industrial and service robots as well as smart grid solutions with multimodal energy generation from regenerative sources such as solar, wind, geo-thermal or hydropower and the energy transport within the bidirectional multi-level network are just a few examples. Here, power electronics, sensor technology, signal processing and communication electronics are heterogeneously integrated into very complex systems for highly safety-relevant functions.

In order to tackle these challenges, industry, research institutes and academia collaborate closely in pre-competitive R&D projects on all levels, European, transnational, national and regional. On European level, funding is provided by the European Commission via work programs like on ICT (Information and Communication Technologies), NMBP (Nanotechnologies, Advanced Materials, Biotechnology and Advanced Manufacturing and Processing), and Transport (Smart, green and integrated transport) as well as with within the large JTI ECSEL (Joint Technology Initiative Electronics Components and Systems.

On the transnational level, the Eureka clusters PENTA, Euripides, and ITEA are complementary funding schemes, which are supported further by a large variety of programs on national and even regional levels). Additionally in 2017, a first Important Project of Common European Interest (IPCEI) on Microelectronics was launched. In all these R&D projects, improving the reliability according to the requirements of the respective application domains have always been a major objective. Technical and training sessions during EuroSimE 2020 and 2021 demonstrated the importance of modelling and simulations in respect to reliability to a broad audience.

All these funding schemes are guided by the ECS SRIA (Electronic Components and Systems Research and Innovation Agenda). This roadmap document has been created in 2017 by the three European associations of the electronics industry AENEAS, Artemis-IA and EPoSS and is now updated every year. In its chapter on ‘Quality, Reliability Safety, and Security’, the research and innovation priorities in the field of reliability methodologies including physics of failure, data driven, and hybrid approaches for EoL (end of life) as well was for RUL (remaining useful live) assessments are defined.

Physics-of-failure approaches are used by most industrial companies where the smaller ones, SMEs, are supported by the research institutes (Imec, Fraunhofer, LETI, SINTEF, RISE). Large central consortia like CALCE (www.calce.umd.edu) and CAVE³ (cave.auburn.edu) do not exist in Europe.

Reliability of devices has strong culture in Europe. Historically there exists close pre-competitive research between academy and industry. Funded programs in Europe typically support reliability research of test devices that are defined by the industry or SME’s (Small and Medium Sized Enterprises). Due to this, possible failure modes are investigated and understood early in basic research. This results in a strong understanding for the reliability performance of innovative devices, even on system level.

From a European perspective, there are three major challenges to be investigated from a reliability point of view:

1) Model based approaches including AI/ML (Artificial Intelligence/Machine Learning): Virtual prototyping techniques are well established in Europe, but further co-ordination along the value chain needs attention. With a huge amount of data generated, AI and/or ML concepts are needed. Special funding schemes on both national and European level are being initiated.
2) Condition-based monitoring, in order to:
   a) Determine actual mission profiles of systems;
   b) Perform prognostics and health management of the systems using physics-of-degradation concepts;
   c) Predict remaining useful life for devices.
3) Software and Hardware reliability: Software reliability can be captured with growth models, hardware with physics-of-failure approaches. But the main question is: how can we combine these approaches, which act on different time scales.

Major Reliability Challenges Based on On-Going Publicly Funded Reliability Projects

In the table below we have compiled ongoing publicly funded projects, its website reference and listed challenges considered in these projects. These are large consortia are dealing with DfR In addition there exist a multitude of smaller national and international consortia.

Acronym	Challenges
iRel4.0 **www.irel40.eu** iReλ 4.0 intelligent Reliability 4.0	In the ECSEL JU funded project iRel40 75 partners from 13 countries are collaborating along the value chain from wafer production to system integration and combine their strength to enhance reliability along the value chain.
smartSTAR **www.elektronikforschung.de/projekte/smartstar** smart STAR	In the SmartSTAR project, the concept of an automotive integrated health management ECU is being developed for the first time. This will permanently monitor important electronic components and indicate signs of materials wear-out as early as possible. For this purpose, miniaturized sensors are being integrated directly into the ASIC. In addition, AI/ML based algorithms and methods are developed for in-situ degradation monitoring.

HiPer www.penta-eureka.eu/project-overview/penta-call-3/hiper/	In Hiper, we improve High Performance Vehicle Computer (HPVC) thermo-mechanical reliability in harsh automotive environments, achieving a lifetime of 50,000 hours in contrast to the current 8,800 hours. This will include: the development of an innovative mold underfill technology; the application of new accelerated testing and qualification methods; prognostics and health management (PHM); new design for reliability (DfR) simulations; and reliability concepts.
Power2Power www.infineon.com/cms/en/product/promopages/power2power/	Develop silicon-based power semiconductors with increased power density and energy efficiency. The partners along the value chain (wafer-, semiconductor-, package-, system- and application-manufacturers) will establish pan-European pilot lines with advanced industry 4.0 aspects to develop innovative power electronics that are fit for the future.
NextGaN www.ganext-project.com	Remove barriers for GaN adoption and demonstrate the higher efficiency and power density of GaN-based system in a range of applications. The heart of the project is the development of an intelligent GaN power module where the controller, drivers and protection circuits are co-packaged with the power devices.
Compass www.itea3.org/project/compas.html	Develop novel, compact models and ultra-compact digital twins. The compact models capture nonlinear, transient and coupled (i.e. multiphysics) situations. The digital twins can self-sufficiently cast decisions (ultimately in real time) for prognostic health management.

Getting SMEs on board

We may safely say that in Europe, the leading large industrial companies play into the "Champion's league" with respect to reliability assessment, virtual engineering and PHM. But we must not forget that there is a multitude of SMEs ???small and medium sized companies designing high end electronics in niche markets. This also includes the many start-ups in growing fields such as IoT, AI edge computing etc. Thanks to their minimum overhead, hands-on approaches, and short communication channels, they can realize products in a rather short time. With respect to design for reliability (DfR), they do often not have the expertise, or simulation tools to perform the analysis for new products. Quite regularly, start-ups fail due to reliability issues with their products during qualification or in the field. Some of these failures could be identified and corrected in design phase but are not captured due to the lack of expertise. An historical example was the mounting of two BGAs with moderate heating on both sides of the PCB (for electrical performance reasons) which led to a local overheating of the system. Consequently, the start-up failed as time and cost for redesign was not available anymore.

Thanks to the strong encouragement of local governments and EU funding agencies to incorporate SMEs into R&D projects, it gives them a fast-learning insight in DfR processes, expertise, and tools within product development for these leading companies.

Ideally, every new electronic design should get a reliability risk assessment, for example using the FMEA (Failure Mode and Effects Analysis) technique. This can be a qualitative assessment done by reliability experts and when some risks are identified, a quantitative reliability assessment should be done.

Strength Fast product development	**Weakness** Lack of reliability expertise, tools and DfR within product development
Opportunity Make DfR part of new design using tools, and external expertise	**Threat** Redesign due to electronics failing in qualification phase or in the field

SWOT analysis w.r.t. DfR analysis in SMEs and start-ups

Specific actions are taken towards SMEs to get them on board of the advanced DfR train:

- Networking events: local workshops in different countries provide low barrier access for SMEs
- Concrete guidelines on reliability qualification and quantification, and best practices for DfR
- Incorporation in R&D projects through local brokerage events
- Seminars and on-site hands-on trainings
- Helpdesk for electronic assembly
- Individual consultancy on PBA Design-for-X (**P**rinted **B**oard **A**ssemblies Design for e**X**cellence), development, production, failure-analysis, etc

Several industrial oriented R&D centers provide these services to the local industry.

European Center of Excellence (ECEx)—Education

Reliability of electronic components and smart systems is of major concern. For the new applications, the complexity and heterogeneity as well as the harshness of the service condition and the safety requirements are increasing strongly and at the very same time. Hence, there is an urgent need for strengthening the training on advanced reliability methodologies. An Erasmus Mundus MSc program exists already for Smart Systems Integration technologies. It is to be complemented by dedicated MSc programs on the Reliability of Electronics as well as by widespread training courses for European enterprises, for SME in particular. Currently, research institutes such as RISE, Imec, and Fraunhofer ENAS are working on establishing a European Center of Excellence (ECEx) on DfR methodologies for electronic components and smart systems. The strong involvement of electronics industry is crucial as well as the active participation by leading OEMs as educators. Hence, the ECEx will be developed as a network of experts and not as a separate organization.

The mission of ECEx is to support education and to increase the knowledge base in the field of reliability of electronic packaging and smart systems. Specifically, ECEx will focus on:

- Organization of summer schools
- Webinars that allow experts to reach a wider audience in Europe,
- Make it possible for people from Academia to have a sabbatical year at Industry (supported by EU funding) or Industry representative to work in academia (supported by EU funding).
- a Europe wide course curriculum can be developed, with a Europe-wide exam (MSc in electronics reliability)

First examples are free lectures from leading professors at EU academia during the last EuroSimE conference (www.eurosime.org).

Major Research Institutes

Europe has traditionally two major group of research centers. The first one is based on research institutes, which are partly financed by local government and partly through contracts with industry or European funding schemes. In Germany, Fraunhofer Gesellschaft comprises some 80 institutes across the entire country. Reliability and quality of electronic components and system is a particular focus area of the Fraunhofer institutes ENAS, IISB, IWMS, and IZM.

Belgium, Imec is the main research institute that cooperates with the electronics industry. In its headquarter in Leuven and associated labs in Gent, Antwerp, Hasselt and Brussels, there is also a strong collaboration with all universities.

In Sweden, RISE is present in several locations. Focus is on quality and reliability of components and systems.

Besides the institute with a particular focus on reliability mentioned above, research organizations from other European countries contribute as well. In Norway, there is SINTEF and in Finland, there is VTT. For France, CEA LETI is the leading research institute. In the Netherlands, TNO with its 14 institutes spread over the country fill this position.

As the second group, there is a number of European universities, which have strong reliability programs in their portfolio as well. Usually, they are located in close vicinity to the major European electronic companies and have intensive cooperation with them.

In Germany, TU Chemnitz, TU Dresden and IMTEK at Freiburg University have particularly strong reliability programs for electronics. In addition, Jade University located in north Germany has a very specific focus on compact and reduce order modeling with an application in semiconductor and electronics.

In the Netherlands, there are two major scientific centers located close to the engineering industrial leaders:

- TU Delft focuses on micro- and nano-electronic reliability.
- TU Eindhoven besides reliability and technology focus is specializing in compact modeling.

Other European universities with a strong reliability programs include:

- Greenwich University (UK)
- Aalto University (Finland)
- Bordeaux (France)
- University of Wroclaw (Poland)

European Reliability Conferences

The EU Reliability society is concentrated around the following conferences and workshops:

- **EuroSimE**—International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems. Main focus: The conference addresses the results of fundamental research and industrial applications for vibrational, thermal, mechanical and multiphysics simulation and experiments of micro/nano-electronics and microsystems. More information can be found here: https://www.eurosime.org/
- **ESREF**—European Symposium on Reliability of Electron Devices, Failure Physics and Analysis. https://esref2021.sciencesconf.org/resource/page/id/43
- **EuWoRel**—European expert workshop on reliability of electronics and smart systems organized by EPoSS (https://www.smart-systems-integration.org/).
- **European Safety and Reliability Conference** (**ESREL**) is an international conference under the auspices of the European Safety and Reliability Association (**ESRA**).
- **ESTC**—Electronic System-Integration Technology Conference. ESTC is the premier venue for academics and industry to present and discuss the latest developments in electronics packaging.: https://www.estc-conference.net/home
- **EMPC**—European Microelectronic and Packaging Conference & Exhibition (https://empc2021.org/)
- **Therminic**—Thermal investigations of ICs and Systems. Therminic is the major European Workshop related to thermal issues in electronic components & systems (https://therminic2021.eu/)
- **European conference of the PHM society**—The Prognostics and Health Management Society (PHM Society) is a non-profit organization dedicated to the advancement of PHM as an engineering discipline. It serves industry, academia, and government leaders in this international community. https://phm-europe.org/

Przemyslaw Gromala, Robert Bosch GmbH
Willem van Driel, Signify / TU Delft
Sven Rzepka, Fraunhofer ENAS
Dag Anderson, RISE
Bart Vandevelde, Imec
Klaus Pressel, Infineon Technologies AG

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Here are a few examples of available books in pdf format: (more added every year)

1. *Lead-Free Electronics: iNEMI Projects Lead to Successful Manufacturing* by E. Bradley, C. Handwerker, J. Bath, R. Parker and R. Gedney; Publication Date: 2007
2. *Magnetic Actuators and Sensors* by J. Brauer; Publication Date: 2006
3. *Multigrid Finite Element Methods for Electromagnetic Field Modeling* by Y. Zhu and A. Cangellaris; Publication Date: 2006
4. Silicon *Germanium: Technology, Modeling, and Design* by R. Singh, H. Oprysko and D. Harame; Publication Date: 2004
5. *Integrated Passive Component Technology* by R. Ulrich and L. Schaper; Publication Date: 2010

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