EPTC 2021

23nd Electronics Packaging Technology Conference
1st-3rd Dec 2021, Singapore

IEEE EPS Flagship Conference
in Asia Pacific Region

Call for Registration

ABOUT EPTC

The 23rd IEEE Electronics Packaging Technology Conference (EPTC2021) is an international event organized by the IEEE RS/EPS/EDS Singapore Chapter and co-sponsored by IEEE Electronics Packaging Society (EPS). It aims to provide a platform for the dissemination of innovations and new developments in semiconductor packaging and component technology, from design to manufacturing. Since its inauguration in 1997, EPTC has been established as a highly reputed electronics packaging conference and is the EPS flagship conference in the Asia-Pacific Region 10. It covers diverse areas of electronics packaging technology including modules, components, materials, equipment technology, assembly, reliability, interconnect design, device and systems packaging, heterogeneous integration, wafer-level packaging, flexible electronics, LED, IoT, 5G, autonomous vehicles, photonics, emerging technologies, 2.5D/3D integration, and smart manufacturing. EPTC2021 features keynotes, technology talks, invited presentations, technical presentations, sponsorship & exhibition corners, and virtual networking activities.

The EPTC technical program committee which consists of more than 100 experts from diverse technology areas in the semiconductor packaging industry, is committed to creating an engaging technical program for the packaging community. Last year, the 22nd EPTC was conducted on a virtual platform due to the pandemic. More than 680 attendees attended from 30 countries worldwide, with 140 video presentations across the 26 technical sessions. Additionally, technology talks from industry and academic experts have been introduced. The technical program and technology talks will be supplemented by an exhibitionwhere companies exhibit their latest technologies and products for the packaging community.

Considering the current prevailing pandemic situation, the EPTC organizing committee has decided to hold the 23rd EPTC conference proceedings in a virtual mode with both live presentations (Dec 1-3, 2021) and on-demand presentations (December 1-31, 2021). EPTC 2021 will feature live presentations of Keynotes, Technology Talks, Panel Discussions and a HIR Workshop, and on-demand presentationsof recorded live presentations, conference invited presentations, regular technical presentations, and professional development courses.

Registration details for EPCT2021 can be found here and EPTC 2021 Advance program can be found here .

Upon successful registration, you will receive the instructions to access EPTC2021 presentations.

The program highlights are as follows:

KEYNOTES

Advanced Package FAB Solutions for Next-Generation Devices *by* **Seung Wook Yoon**, PhD, MBA

Dr YOON is currently the Corporate VP and Head of Team of Package Technology Strategy and Planning, Samsung Electronics. Before joining Samsung, he was director of group technology strategy, STATS ChipPAC, JCET Group. He also worked as a deputy lab director at the Institute of Microelectronics, A*STAR, Singapore. ”Yoon” received a Ph.D degree in Materials Science and Engineering from KAIST, Korea. He also holds an MBA degree from Nanyang Business School, Singapore. He has over 300 journal papers, conference papers, trade journal papers, and over 20 US patents on microelectronic materials and electronics packaging. He has served as a technical committee member of various international packaging technology conferences, EPTC, ESTC, iMAPS, IWLPC and SEMI.

Future Directions for 3D Integration Technologies, Enabling Further Electronic System-Level Scaling Benefits *by* **Eric Beyne,** PhD.

Dr Eric Beyne is Senior Fellow, VP R&D and Program Director 3D System Integration Program, IMEC. Eric obtained a degree in electrical engineering in 1983 and a PhD in Applied Sciences in 1990, both from the Katholieke Universiteit Leuven, Belgium. Since 1986 he has been with IMEC in Leuven, Belgium, where he has worked on advanced packaging and interconnect technologies.

TECHNOLOGY TALKS

A Roadmap Based on a Holistic Understanding of Thermo-mechanical Challenges from Package to System to Maximize Silicon Performance *by* **Gamal Refai-Ahmed**, PhD, LFASME, FIEEE, FCAE, FEIC, Xilinx Fellow.

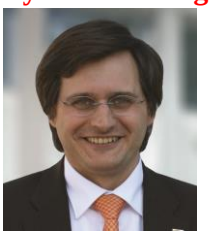
Dr Gamal Refai-Ahmed, Life Fellow ASME, Fellow IEEE, Fellow Canadian Academy of Engineering, is Xilinx Fellow and Chief Thermo-Mechanical Architect. He obtained the Ph.D. degree in Mechanical Engineering from the University of Waterloo. He has been recognized as one of the global technology leaders of thermal management through his numerous publications (more than 100 publications) and patents & patents pending US (more than 60) and International (more than 120). His contributions are seen in several generations of both GPU and FPGA products.

State University of New York, Binghamton University awarded him the Innovation Partner Award for his industrial role with Binghamton University. Gamal is the recipient of the 2008 excellent thermal management award, 2010 Calvin Lecture and 2013 K16- Clock award in recognition for his scientific contributions and leadership of promoting the best electronics packaging engineering practice. In 2014, Gamal received the IEEE Canada R. H. Tanner Industry Leadership for sustained product development and industrial innovation leadership. In 2016, ASME awarded Gamal the ASME Service Award. In continuation to Dr Refai’s contributions to the best engineering practice, the State University of New York at Binghamton awarded him the Presidential University medal in 2019, the university’s highest recognition honour. In 2020, Gamal was elected to IEEE Fellow for 2021.

Packaging Materials as a Key Enabler for Future Megatrends *by* **Klemens Brunner,** PhD.

Since March 2018, Klemens Brunner serves as President of Heraeus Electronics, a leading packaging materials supplier in the electronics industry headquartered in Hanau, Germany. Before that, he was head of the Marketing & Sales department of Heraeus Electronics. He began his career at Philips Research in the Netherlands, where he worked on LEDs technology development and Philips business group Automotive Lighting in product marketing. He joined Lumileds (formerly a division of Philips) in San Jose, USA as general manager of the business unit Automotive LED and general manager Automotive Lighting Asia Pacific, where he was based in Hong Kong. Klemens Brunner has a PhD in physical chemistry from the University of Vienna.

Hybrid Bonding – State-of-the-Art and Upcoming Requirements *by* **Paul Lindner,** PhD**.**



Paul Lindner heads the R&D, product and project management, quality management, business development and process technology departments. Lindner joined the company in 1988 as a mechanical design engineer and has since pioneered various semiconductor and MEMS processing systems, which have set industry standards. His responsibilities included designing semiconductor processing systems and tooling for custom applications, including innovative system designs pioneered in the first commercially available wafer bonders, silicon-on-insulator (SOI) bonding systems, and precision alignment systems for 3D interconnect applications. Prior to his appointment as executive technology director, Lindner established a product management department at EV Group. During that time, he was involved in marketing, sales, manufacturing and on-site process support.

Innovative Copper Electrodeposition Solutions for High-Density Fanout Package Technology *by* **Bryan Buckalew,** PhD, Technical Director, Lam Research Corporation, USA

Technology talk (title TBD) *by* **Jinho An**, PhD, Technology Director, Applied Materials, USA

Technology talk (title TBD) *by* **Emilie Jolivet**

Emilie Jolivet is Director of the Semiconductor & Software Division at Yole Développement (Yole), part of Yole Group of Companies. Emilie manages the expansion of the technical and market expertise of her team. In addition, Emilie's mission focuses on managing business relationships with semiconductor leaders and developing market research and strategy consulting activities. With its previous collaborations at Freescale and EV Group, Emilie developed core expertise dedicated to package & assembly, semiconductor manufacturing, memory and software & computing.

Emilie Jolivet holds a Master's degree in Applied Physics specializing in Microelectronics from INSA (Toulouse, France) and graduated with an MBA from IAE (Lyon, France).

PANEL

Supply Chain Ecosystem Challenges Impacting Global Electronic Packaging

This Panel will cover supply chain trends (e.g. convergence, mergers, and acquisitions), material shortages, equipment limitations, manufacturing capacity, and disruptions (e.g., geopolitical, natural & human resources, regulatory & Environmental Health and Safety). Each of these factors must be taken into consideration when making technical and business decisions. Exacerbating these challenges is the COVID pandemic.

The Panel will be chaired by Dr Kitty Pearsall and panellists include C. P. Hung (ASE), Chun Ho (Nelson) Fan (ASM PT), Jan Vardenman (TechSearch International) and TBD (GlobalFoundries). Details of the Panel at EPTC 2021 will be finalized soon.

WORKSHOP

Heterogeneous Integration Roadmap (HIR)

The Heterogeneous Integration Roadmap (HIR), released in October 2019, is a roadmap to the future of electronics packaging, identifying technology requirements and potential solutions. The primary objective is to stimulate pre-competitive collaboration between industry, academia, and government to accelerate progress. The roadmap offers professionals, industry, academia, and research institutes a comprehensive, strategic technology forecast over the next 15 years. The HIR also delivers a 25-year projection for heterogeneous integration of Emerging Research Devices and Emerging Research Materials with more comprehensive research and development timelines.
Details of the HIR Workshop at EPTC 2021 will be finalized soon

PROFESSIONAL DEVELOPMENT COURSES (PDC)

Antenna-in-Package (AiP) Technology for Millimeter-Wave Applications; INSTRUCTOR: Y. P. ZHANG, FIEEE , NANYANG TECHNOLOGICAL UNIVERSITY, SINGAPORE

Prof.Yueping ZHANG is a full Professor with the School of Electrical and Electronic Engineering at Nanyang Technological University, Singapore, a Distinguished Lecturer of the IEEE Antennas and Propagation Society (IEEE AP-S), a Member of the IEEE AP-S Paper Award Committee, and a Fellow of IEEE. Prof Zhang has published numerous papers, including two invited and one regular paper in the Proceedings of the IEEE and one invited paper in the IEEE Transactions on Antennas and Propagation. He is the Chinese radio scientist who has published a historical article in an English learned journal such as the IEEE Antennas and Propagation Magazine. He received the 2012 IEEE AP-S Sergei A. Schelkunoff Prize Paper Award.
Prof Zhang delivered the plenary, keynote, and invited speeches at the flagship conferences organized by IEEE, CIE, EurAAP, and IEICE. He received the Best Paper Award from the 2nd IEEE/IET International Symposium on Communication Systems, Networks and Digital Signal Processing, July 18–20, 2000, Bournemouth, UK, the Best Paper Prize from the 3rd IEEE International Workshop on Antenna Technology, March 21–23, 2007, Cambridge, U.K., and the Best Paper Award from the 10th IEEE Global Symposium on Millimetre-Waves, May 24–26, 2017, Hong Kong, China.

Packaging and Heterogeneous Integration for Automotive Electronics, and Advanced Characterization of EMCs; INSTRUCTOR: PRZEMYSLAW GROMALA, ROBERT BOSCH GMBH, GERMANY

Dr.Przemyslaw Gromala is a simulation senior expert at Robert Bosch GmbH, Automotive Electronics in Reutlingen. He is currently leading an international simulation team and FEM verification lab focusing on implementing simulation-driven design for electronic control modules and multi-chip power packaging for hybrid drives. His research activities focus on virtual pre-qualification techniques for the development of electronic control modules and multi-chip power packaging. His technical expertise includes material characterization and modelling, multi-domain and multi-scale simulation incl. Fracture mechanics, verification techniques, prognostics and health management for safety-related electronic smart systems.

Prior to joining Bosch Mr. Gromala worked at the Delphi development center in Krakow, as well as at Infineon research and development center in Dresden. He is an active committee member of the IEEE conferences: ECTC, EuroSimE, ICEPT; ASME: InterPACK. Active committee member of EPoSS – defining R&D and innovation needs as well as policy requirements related to Smart Systems Integration and integrated Micro- and Nanosystems. He holds a PhD in mechanical engineering from the Cracow University of Technology in Poland

Fan-out, Chiplets and Hybrid Bonding; INSTRUCTOR: JOHN H LAU, UNIMICRON TECHNOLOGY CORPORATION

Dr.John H Lau , with more than 40 years of R&D and manufacturing experience in semiconductor packaging, John has published more than 500 peer-reviewed papers, 30 issued and pending US patents, and 22 textbooks on, e.g., Advanced MEMS Packaging (McGraw-Hill, 2010), Reliability of 2D and 3D IC Interconnects (McGraw-Hill, 2011), TSV for 3D Integration, (McGraw-Hill, 2013), 3D IC Integration and Packaging (McGraw-Hill, 2016), Fan-out Wafer-Level Packaging (Springer, 2018), Heterogeneous Integrations (Springer, 2019), Assembly and Reliability of Lead-Free Solder Joints (Springer, 2020), and Semiconductor Advanced Packaging (Springer, 2021). John is an elected ASME Fellow, IEEE Fellow, and IMAPS Fellow.

Flip Chip Interconnect Technologies; INSTRUCTOR: ERIC PERFECTO, IBM CORPORATION AND SHENGMIN WEN, SYNAPTICS INC.

Dr Shengmin Wen is the Principal Package Architect at Synaptics Inc., has more than 20 years of semiconductor industry experience in the areas of Si fabrication technology, advanced packaging and assembly process development, Si and packaging co-design, semiconductor device failure analysis, reliability and qualification, product engineering, testing, and volume production business management. In recent years, he focused on the chip-scale package (CSP), including wire bond, flip chip, wafer-level Fan-In and Fan-out, and panel-level packaging development. In particular, he has extensive and unique experiences in flip-chip assembly technologies that uses fine pitch Cu Pillar bump with both mass reflow and thermal compression processes. He is an expert in package warpage control, substrate technologies, advanced fine pitch flip-chip assembly process, and reliability.

He previously worked at Amkor Technology, where he was a director of the 3D CSP Product Group. Dr Wen received his PhD from Northwestern University, Evanston, IL, USA, researching on fatigue and reliability of electronic materials, where he created and published a science-based fatigue theory. Dr Wen has been actively participating and contributing to industry technical conferences to learn, share, and contribute.

Eric Perfecto has over 39 years of experience working in developing and implementing C4 and advanced Si packages at IBM and GLOBALFOUNDRIES. Responsibilities included UBM and Pb-free solder definition for C4 and u-Pillar interconnect and yield improvements in C4 and 3D wafer finishing. He is currently working at the IBM Nanotech Center. He holds an MS in Chemical Engineering from the University of Illinois and an MS in Operations Research from Union College. Eric has published over 75 external papers, including two best Conference Paper Awards (2006 ESTC and 2008 ICEPT-HDP) and the 1994 Prize Paper Award from CMPT Trans. on Adv. Packaging. He holds 55 US patents and has been honoured with two IBM Outstanding Technical Achievement Awards and an IBM Outstanding Contribution Award for the development of the 3D wafer finishing Process (2014). Eric was the 57th ECTC General Chair in Reno, NV, and the Program Chair at the 55th ECTC. Eric is an IEEE Fellow and has achieved senior member status from IMAPS and the Society of Plastic Engineers. He is an EPS Distinguish Lecturer, the Awards Program Director and elected board member of the Electronics Packaging Society of IEEE.

ESD Impact and Risk on IC Package Technology Development and MEMs Devices; INSTRUCTOR: CHARVAKA DUVVURY, ESD CONSULTANT, IEEE DISTINGUISHED LECTURER

Dr Duvvury received his PhD in Engineering Science from the University of Toledo and has worked for Texas Instruments for 35 years in semiconductor device physics with development work in ESD design. He was elected as TI Fellow in 1997 and as IEEE Fellow in 2008. He has contributed to the industry by offering tutorials at various IEEE sponsored conferences and participating in the EDS DL Program. He served as an editor for TDMR (2001-2011) and is currently serving as the editor for TED. After retiring from TI, he has been working as a technical consultant on ESD design. He is a recipient of the IEEE Electron Devices Society's Education Award (2013), Outstanding Contributions Award from the EOS/ESD Symposium (1990), and Outstanding Industry Mentor Award from the Semiconductor Research Council (1994 and 2012). From 2004-2006 he served on the IEDM CMOS Reliability Sub-committee. He has published over 150 papers in technical journals and conferences and holds US 75 patents. He co-authored and contributed to 5 books. Charvaka has been serving on the Board of Directors of the ESD Association (ESDA) since 1997, promoting ESD education and research at academic institutes. He served twice as General Chairman of the ESD Symposium. He has been co-founder and co-chair of the Industry Council on ESD since 2006. In 2015, he co-founded iT2 Technologies that utilizes an intelligent software engine for rapid ESD data analysis.

CONFERENCE TOPICS

There are altogether **150 technical presentations** covering important aspects of electronics packaging listed below.

- Advanced Packaging
- TSV/Wafer Level Packaging
- Interconnection Technologies
- Emerging Technologies
- Materials and Processing
- Assembly and Manufacturing Technology
- Electrical Simulation & Characterization
- Mechanical Simulation & Characterization
- Thermal Characterization & Cooling Solutions
- Quality, Reliability & Failure Analysis
- Advanced Optoelectronics and Displays.
- Smart Manufacturing and Equipment Technology

We are particularly grateful for the continued and strong support from our sponsors. Your support have enabled us to carry on with the cause to provide a platform for timely dissemination of the latest technical knowledge to the electronics packaging community.

EPTC2021 Conference Sponsors

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MESSAGE

On behalf of the EPTC 2021 organizing committee, I would like to extend our sincere gratitude to all sponsors, exhibitors, media partners, technical committee members for providing their continued generous support despite the current uncertainties and challenging circumstances. I trust everyone is coping well despite the disruptions caused by the pandemic. We are all affected in one way or another, and it is more important than ever to support one another. We also quickly learn that digital transformation has a key role to play, becoming more significant than before. I hope that you will find this EPTC 2021 online experience an enriching one. I am sure we will emerge stronger from this pandemic, and I hope to meet everyone in person in 2022.

Most sincerely,

Gongyue Tang, PhD
Institute of Microelectronics, Singapore

General Chair
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