Update on the CHIPS and Science Act

Jan Vardaman, Nancy Stoffel, Benson Chan

Abstract

The 2022 CHIPS and Science Act is the largest investment into the microelectronics industry made by the US government in history. The intent of this legislation is to strengthen the competitiveness of domestic manufacturers and suppliers for microelectronics assemblies. The sweeping vision from the signing brief stated that with this legislation, the US is "making historic investments that will poise U.S. workers, communities, and businesses to win the race for the 21st century. It will strengthen American manufacturing, supply chains, and national security. The Act provides money for investment in research and development, science and technology, and the workforce of the future to keep the United States the leader in the industries of tomorrow, including nanotechnology, clean energy, quantum computing, and artificial intelligence. The CHIPs and Science Act makes the smart investments so that American to compete in and win the future."1

What is the CHIPS and Science Act?

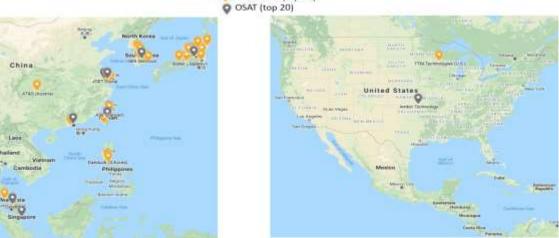
The CHIPS and Science Act seeks to do the following:

- Increase capacity in domestic manufacturing and emerging technologies
- Promote critical supply chain resilience •
- Strengthen the national capacity for manufacturing innovation, and expands workforce development efforts
- Deliver important measurement and technology to semiconductor R&D needs

The U.S.Department of Commerce (DoC) will manage both the incentive and R&D programs and support industry at large. The incentives program is \$39 billion and is focused on increasing domestic semiconductor and packaging capacity and capability. Direct funding and loans will be offered to support these goals. Additionally, there are 25% tax credits available for advanced manufacturing investments as well as loans designed to increase capacity. New advanced fabs have received the most attention, but legacy fabs and packaging will also be funded.

DoC has appointed a Special Advisor to help setup the CHIP Act program office and a team is in place to support DoC semiconductor initiatives. The DoC has actively solicited input from the electronics community. DoC and National Institute of Standards and Technology (NIST) have received over 200 unique responses to a CHIP Act RFI issues from the ecosystem. Workshops were held to define metrology needs for the next 5 to 10 years. NIST issued reports including the Strategic Opportunities for U.S. Semiconductor Manufacturing in August 2022.

Department of Commerce and NIST appointed leaders from industry, academia, and national labs to a newly established Industrial Advisory Committee. \$52.7 Billion investment in infrastructure and R& D will be managed by the DoC. There is an additional \$2 Billion investment in prototyping and lab to fab transition called the Microelectronics Commons that will be run by the Department of Defense (DoD).



Where is Semiconductor Packaging? Where is the innovation ecosystem?

Substrates (top 15)

Figure 1 Source NIST

The R&D part of the program has four components, and the funding breakout is shown in Table 1.

The outlined programs will be run out of NIST leveraging the organizations' history in grant management and technology expertise. Figure 2 shows the relationship between the new

The NSTC program described in the 9906 legislation has the following focus areas:

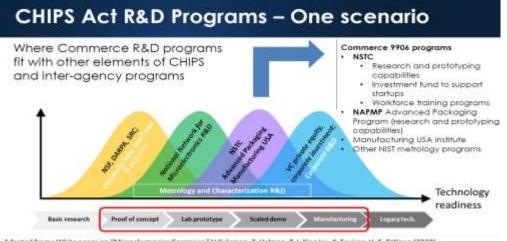
• To conduct semiconductor advanced test, assembly, and packaging capability in the domestic ecosystem."

Table 1: Appropriated Funds for CHIPS andScience Act (\$ in Billions) Source: DoC	FY 2022	FY 2023	FY 2024	FY 2025	FY 2026
Section 9902 Semiconductor Incentives					
Incentives Program	19	5	5	5	5
Section 9906					
National Semiconductor Technology Center	2	2	1.3	1.1	1.6
Nat. Adv Packaging Manufacturing Program	2.5				
Microelectronics Research at NIST	0.5				
Manufacturing USA Institutes	0.5				

investments managed by the Department of Commerce, and existing programs

The National Semiconductor Technology Center (NSTC) will be the focal point of the R&D investments. Its mission will be to advance semiconductor technology throughout the semiconductor ecosystem, and seed new industries, based on the availability of advanced semiconductor devices. The NSTC will focus on fab level integrated circuit developments with \$2 billion in the first

- Materials characterization, instrumentation and testing for next generation microelectronics.
- Virtualization and automaton of maintenance of semiconductor machinery.
- Metrology for security and supply chain verification.
- training programs and apprenticeships, in advanced microelectronics design, research, fabrication, and packaging capabilities,"



Adapted from : White paper on "Microelectronics Commons," V. Coleman, Z. Holman, T.-J. King Liu, K. Squires, H.-S. P. Wong (2020)

Figure 2: CHIPS and Science Act investments to support semiconductor and packaging development

year and continuing investments over the next 5 years. NIST solicited input across the industry on the needs and structure of the proposed NSTC and they received over 250 responses on their questions on the scope of the NSTC. They have also hosted 36 workshops and solicited input through other advisory bodies. NIST will publish a whitepaper in the first quarter of 2023 that will summarize the results of the landscape analysis, governing structure, and financial models. The CHIPS Act is not just about the chips but rather recognizes the critical role that packaging plays in the electronicsmanufacturing ecosystem. Without parallel advances in substrate, test and assembly capabilities, the supply chain issues will not be solved. The National Advanced Packaging Manufacturing Program is the largest R&D program investment with a \$2.5 billion budget. The focus is to strengthen semiconductor advanced test, assembly, and packaging capability in the domestic ecosystem. Additional critical R & D investment designed to move developments through the transition from lab to fab, is the Microelectronics Commons. The \$2 Billion investment in prototyping capabilities will be run by DoD.

There are also funds set aside for microelectronics Research at NIST which will include a focus on metrology needs for the industry. Additionally further investment into the Manufacturing USA Institutes will be funded at \$0.5 billion in the first year with additional funding over the next four years. The intent is to utilize the strengths of the existing 16 manufacturing institutes. These institutes and their focus areas are shown in Figure 3. Additionally, the bill specifies that up to 3 new manufacturing institutes (NMI) focus may include

- Research to support the virtualization and automation of maintenance of semiconductor machinery.
- Development of new advanced test, assembly, and packaging capabilities.
- "...Developing and deploying educational and skills training curricula needed to support the industry sector and ensure the U.S. can build and maintain a trusted and predictable talent pipeline,"

customers. The institutes require cost-match to federal investment. The current list of existing MII are: shown in Figure 3.

The next MII focus areas are under development and input will be sought through an RFI.

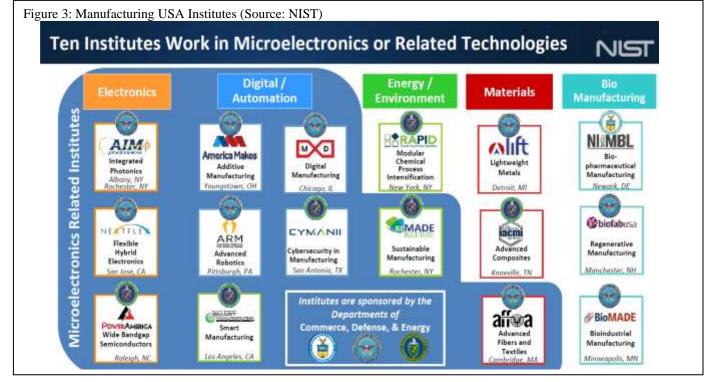
The Global share of the US in packaging manufacturing is only 3% (See Figure 4). However, the US has major strengths in

Figure 4: North Amerian electronics manufcturing capabilities (source: US DoD and IPC)

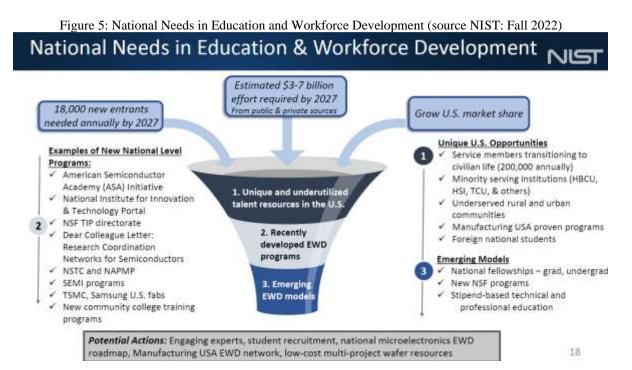


packaging research both academic and industrial. With investment, these strengths can be converted into new domestic manufacturing capabilities focused on advanced packaging.

Advanced packaging is an enabler. Combining heterogeneous devices together in a package creates compact and capable systems critical to new applications, DOD, and industrial uses. Packaging incorporates communications capabilities such as 5G and 6G, Bluetooth, and RF, Video drivers, Low-cost combo of cutting-edge chips with legacy chips, Photonics, Compound



The current common institute features are that they are focused on identified target manufacturing approaches. These Department of Defense Manufacturing Innovation Institutes (MII) are public-private consortia, with strong participation from industry, academia, and government semiconductor for extending batter life, GPS, stacked memory, and chiplets. Other novel concepts include flexible hybrid electronics. Moore's Law alone is not going to be the enabler of products. New approaches to cost and performance challenges involve shifting from monolithic chip design to modular



concepts. The future includes 3D manufacturing methods and structures. The CHIPS investments will support the development lifecycle from proof of concept through commercialization as shown in Figure 2.

Workforce development is critical for all the CHIPS Act investments as the demand for skilled workers will increase substantially. "Whoever wins workforce, wins microelectronics. Period." The CHIPS Act has substantial goals to create a new and diversified workforce to meet the workforce needs that will arise with the growth of high-tech manufacturing. At this moment in time, the U.S. has unique opportunities to create a new workforce with the needed skillsets. Figure 5 outlines the needs and initial and emerging programs to address these needs.

Specific communities that may match the opportunity include returning service members transitioning to civilian life (200,000 annually), underserved rural and urban communities. Institutions that have demonstrated success with workforce training will be engaged. These institutions include minority serving institutions (HBCU, HIS, TCU, & others), Manufacturing USA proven programs. An additional resource that can meet the emerging technology skill gap are foreign national students. Half of engineering students are foreign nationals. Retraining of the current workforce will also be critical. Emerging models to increase the engineering and science graduates include national fellowships for graduate and undergraduates, new NSF programs, and stipend-based technical and professional education.

For more information go to:

1. https://Chips.gov

- <u>https://www.whitehouse.gov/briefing-</u> <u>room/statements-releases/2022/08/09/fact-</u> <u>sheet-chips-and-science-act-will-lower-costs-</u> <u>create-jobs-strengthen-supply-chains-and-</u> counter-china/
- 3. <u>https://www.mckinsey.com/industries/public-and-social-sector/our-insights/the-chips-and-science-act-heres-whats-in-it</u>
- <u>https://nstxl.org/opportunity/microelectronics-me-</u> commons/
- 5. <u>https://www.manufacturingusa.com/news/manufactur</u> <u>ing-usa-releases-2022-highlights-report</u>

Acknowledgement

The authors would like to acknowledge Frank Gayle, Robert Rudnitsky and David Seiler for presenting their keynote titled "NIST, Semiconductors and the CHIPS and Science Act" at the 33rd Electronics Packaging Symposium held at Binghamton University, September 7, 2022.

Authors



E. Jan Vardaman is president and founder of TechSearch International, Inc., which has provided market research and technology trend analysis in semiconductor packaging since 1987. She is the author of numerous publications on emerging trends in semiconductor packaging and assembly. She is a senior member of IEEE EPS and is an IEEE EPS Distinguished Lecturer. She received the IMAPS GBC Partnership award in 2012, the Daniel C. Hughes, Jr. Memorial Award in 2018, the Sidney J. Stein International Award in 2019, and she is an IMAPS Fellow.



Nancy Stoffel Nancy holds a PhD in Materials Science from Cornell University. Her career has focused on materials, process development and reliability for electronics integration. Currently Nancy works for GE Research and specializes in design and manufacturing of printed electronic systems and electronics

packaging. Nancy is active in the IEEE Electronics Packaging Society and is on the executive board of ECTC.



Benson Chan is the Associate Director for the Integrated Electronics Engineering Center at Binghamton University, a NY State Center for Advanced Technology with a mission to help companies to understand their use of electronics to improve their business by understanding the design, reliability

and failures of their products. He holds 53 patents and numerous papers in electronics packaging. He is an iMAPS fellow and IEEE EPS TC Chair for Emerging Technologies and on the IEEE EPS Board of Governors