Emerging Technology; Smart Manufacturing of Computer Systems and Assemblies

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Abstract—This paper details several current examples of Industry 4.0 **[10]** activity involving application of emerging technologies used for the Smart Manufacture of computer systems and affiliated electronics. Highlights include Smart Manufacturing methods in development and in current production, where the use of artificial intelligence and machine learning is leveraged to improve quality, yield, and reliability at a reduced overall manufacturing cost.

I. INTRODUCTION

The fourth wave of the industrial revolution (known as Industry 4.0), incorporates a proliferation of digital technology, including an enhanced interconnectivity of devices, and related tools brought into the cloud to enable ease of data access and real time analysis. Included in this array of digital technologies are Artificial Intelligence (AI) and Machine Learning (ML) operations designed to provide for decision making and self-improvement. When AI and ML are incorporated into specific assembly or process sequences, so called "Smart Manufacturing" operations are created that allow us to work with machines used in manufacturing process operations in new, and highly productive ways. Moreover, because Smart Manufacturing technology typically enables real time manufacturing feedback such as defect detection, and capability for on-the-fly corrective action and process optimization, the potential for more efficient, consistent, high quality, high reliability end products are realized at an overall reduced manufacturing cost.

In this article we showcase a few examples of smart manufacturing and emerging manufacturing technologies in development or in current use for the assembly and integration of computer systems and related electronics, and convey how these operations will affect manufacturing systems in the coming years.

II. IMPLEMENTATION OF COBOT IN IBM

In recent years, IBM has developed and deployed multiple tools across various sectors of card and system hardware integration for the manufacturing of computer servers to ensure high quality, defect free assembly, with improved manufacturing throughput. At the forefront of these smart assembly efforts are the use of customized Collaborative Robot (COBOT) tools coupled with cameras and integrated software programs that provide defect detection and user feedback loops that guarantee proper assembly. Several specific applications leverage use of these combined techniques, including the integration of large processor modules into land grid array (LGA) sockets, DIMM card installations into system level computer chassis, and the assembly of information secure card hardware.

In general, the use of COBOT methods allows for hands free assembly of delicate, and possibly contamination sensitive hardware that have small assembly process windows to guarantee defect free assembly. As an example, consider LGA sockets comprised of large arrays of thousands of contacts made from 60 micron (μm) thick noble metal plated copper alloy micro-springs. See Figure 1. These micro-spring contacts are sensitive to contamination and are easily damaged from process handling steps spanning socket assembly onto card electronics, and multiple plugging and unplugging of modules into socket sites to support computer system test and build operations. Furthermore, as module pin counts, module sizes, and socket sizes continue to increase to meet systems performance demands, an appreciable potential for contact damage becomes readily apparent if an exact and coplanar alignment of modules into socket housings is not realized.

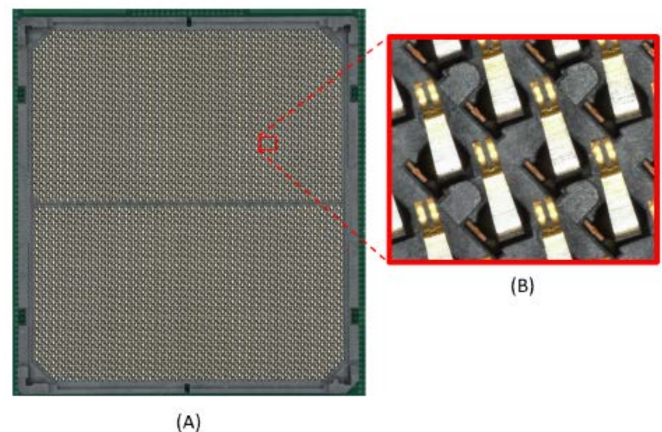

Figure 1. Example Hybrid Land Grid Array Connector (A) and close-up of Contact (B)

To address these sensitivities and damage concerns, an enclosed COBOT, vision system, and affiliated vision recognition process that identifies socket contact and possible socket related defects has been developed and integrated into system manufacturing lines by the IBM Guadalajara Mexico Industry 4.0 manufacturing team. Specifically, a server chassis with socket sites on a motherboard is fed into an

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enclosed COBOT system that is like drawings depicted Figure 2. The COBOT tool, with its specialized handling arms and heads, is first used to remove protective socket covers on the motherboard assembly within the system chassis to proceed with automated socket inspection using a 20 MP camera and custom written computer software.

If socket defects are found prior to placement of modules, the tool auto-records and highlights specific defect areas, enabling quick turn defect mapping, failure analysis, and root cause problem resolution. An example of socket inspection images taken by the COBOT imaging system that highlight good (green) suspect (yellow) and damaged (red) pins is illustrated in Figure 3.

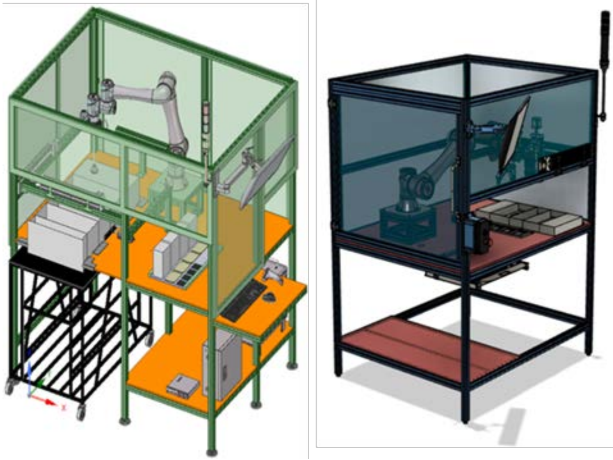


Figure 3. Example Illustrations of Enclosed COBOT Tools Used for Systems Assembly Integration

If no defects are found upon inspection, the vision recognition system and COBOT arm and head assemblies are used to inspect, pick up, and place modules with pre-applied thermal interface pads into system socket sites. This pick and place operation provides a coplanar and accurate X-Y placement of modules into socket housings to an X-Y alignment precision of approximately 50 microns. An image of the COBOT module placement operation is shown in Figure 4. Once modules have been precision placed and seated into socket housings, the COBOT and vision system inspects, picks and places heat removal devices onto the module-socket assembly stack. A load is then applied to the hardware stack to secure the module and actuate the LGA micro-springs to provide stable electrical interconnects. This load is provided by an integrated load screw and spring latch assembly present on the heatsink and card surface, where the load screw is actuated by the COBOT to a fixed stop and torque value.

Note that disassembly steps involving removal of modules for test, upgrade or replacement purposes are also provided using the same COBOT and vision systems tools.

Similar process flows have also been developed for integration of new DIMM card technology that must be aligned and integrated into systems chassis frames affixed to processor card assemblies, while future systems may use COBOT and corresponding vision systems configurations to ensure accurate and reliable plugging and unplugging of large arrays of high-speed cable networks within computer systems chassis as well.

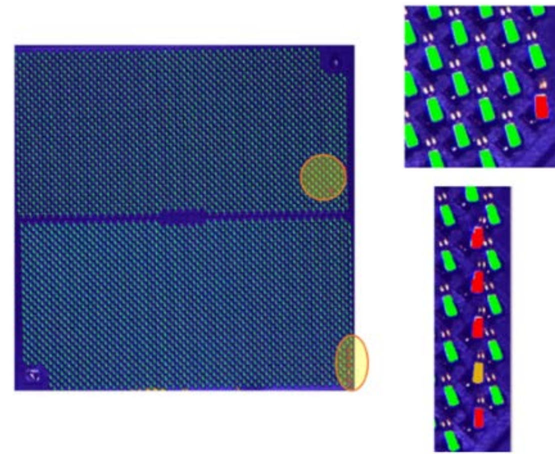


Figure 2. Example COBOT Inspection System Images of Good and Defective LGA Socket Contacts

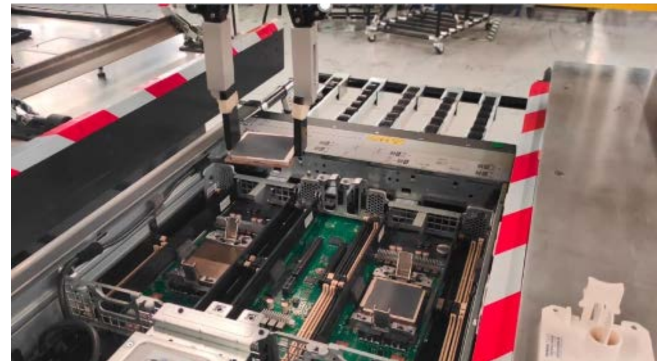


Figure 4. COBOT LGA Processor Module Installation

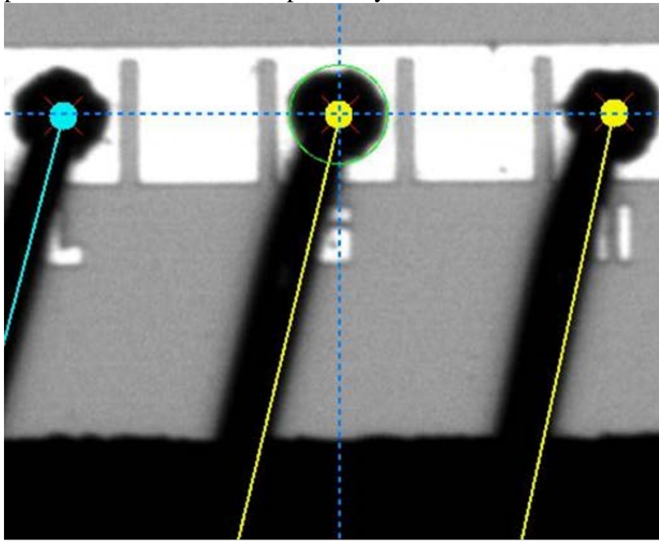
III. Wire bonder smart manufacturing and industry 4.0 improvements at Kulicke&Soffa

The recent development in smart factory and Industry 4.0 (I4.0) initiatives help improve wire bonding quality assurance, operational efficiency and time to market. New machine functionalities have been added to meet the desire for factory automation, real-time monitoring, closed-loop optimization and traceability. Some of the smart functionalities in today's state of art wire bonders include:

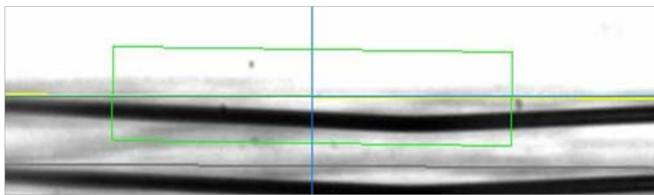
- On bonder automatic setup and calibration solutions to enhance portability and tool matching
- Auto recovery features to improve bonder up time and reduce need for operator assist
- FDC (Fault Detection and Classification) using machine vision, electrical and servo system: PBI (Post bond inspection), automatic loop height, wire sway measurement.
- Digital twins to simulate wire bonding loops in offline CAD programs (as shown in Figure 7).

Figure 5 shows two examples of using wire bonder vision system to detect issues during wire bonding. In the first example (a), wire bonder vision system measures the ball diameter and ball placement. When ball diameter or placement is outside the set limit, machine will stop or warn the operator for corrective action. For ball placement, automatic correction function can be used to correct the placement of the balls based on the actual

measurements to assure machine accuracy. In the second example (b), wire straightness is measured, alarm can be set to detect and prevent wire sway. Excessive wire sway may cause wire short and yield loss. Early FDC can help correct production issues fast and prevent yield loss and field failures.



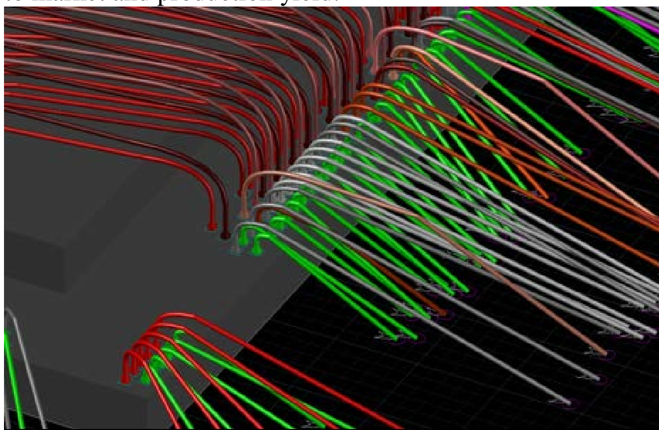
a) On Bonder ball diameter and placement measurement



b) Wire sway measurement

Figure 5. Using wire bonder vision system for defect detection and improve yield

Another I4.0 concept being used in wire bonding is the Digital Twin. 3D loop models serve as a digital to the actual wire loops on the bonder. Figure 6 shows the wire bond looping digital twin that can help design the loop shapes, optimize the wire layout and bonding sequence, and perform clearance check for wire to wire spacing and capillary to wire interference. This digital twin can dramatically shorten the time to market and production yield.



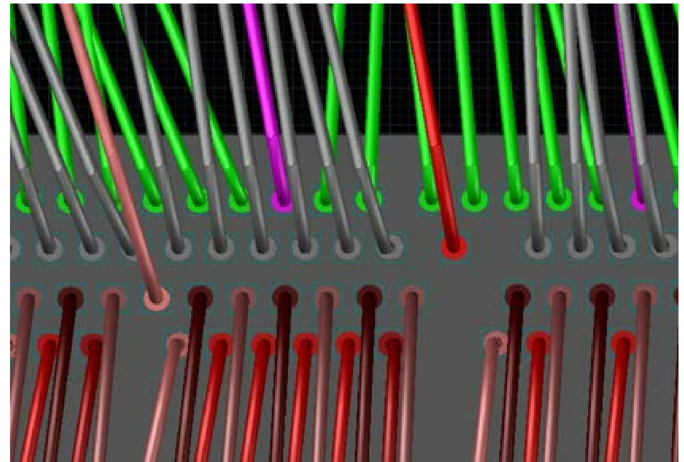


Figure 6. Wire looping model digital twin for offline programming, clearance check to improve time to market and fabrication yield

IV. Smart Factory in Electronics Manufacturing: AI-based Closed-Loop Self-Optimization Platform – At Binghamton University

With the rapid technology development in Industry 4.0, such as artificial intelligence (AI), electronics manufacturing processes can be more intelligent. Smart manufacturing, which adopts real-time decision-making based on operational and inspectional data, can be realized soon [1]. In Surface Mount Assembly (SMA) lines, data-driven solutions can be applied to diagnose abnormal defects and adjust optimal machine parameters in response to unexpected changes/situations during production with the collected data. Collaborating with various industry partners, the State University of New York at Binghamton research team at Binghamton developed a novel framework based on AI-based closed-loop feedback control and parameter optimization to implement an intelligent manufacturing solution in the PCB assembly for yield and throughput improvement. This AI-based framework could provide a potential road map for data-driven process control in SMA.

Each SMA process, including solder printing, pick and place (P&P), and soldering reflow (SRP), has a significant impact on the quality and throughput of the final PCB product. As a result, multiple inspection machines, including solder paste inspection (SPI) and automated optical inspection (AOI) machines, are introduced to monitor the manufacturing process. The Binghamton University Smart Electronics Manufacturing Laboratory (SEML) is fully equipped with two solder paste printers, two chip mounters, and a reflow oven, in addition to

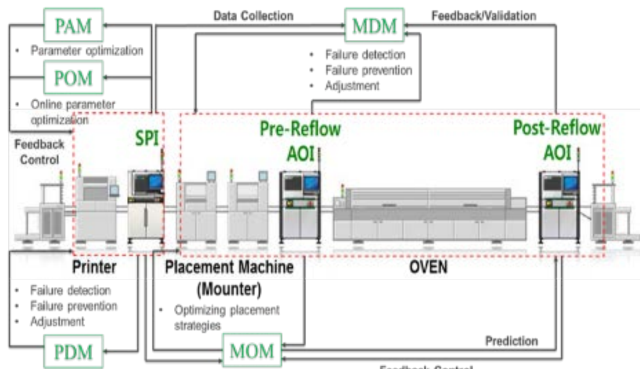


Figure 8. A schematic diagram of the AI-based closed-loop feedback

SPI and AOI machines. At SEML, the research team tested over 10,000 PCBs. The results indicate that numerical methods based solely on physical properties may have practical limitations in explaining the behavioral patterns of small-scale components. However, recent research suggests that methods based on artificial intelligence can improve product quality by up to 35% [2]. It implies that an intelligent SMA process control based on data can advance SMA processes. As a result, the intelligent SMA strives to maintain optimal settings in offline and online environments. Figure 7 depicts the overall schematic of the AI-based closed-loop feedback control framework.

Intelligent SMA Modules

In the solder printing process, four machine intelligence modules are considered: (1) printing advising module (PAM); (2) printing optimization module (POM); (3) printing diagnosis module (PDM); and (4) dynamic stencil cleaning process control (CPC). PAM and POM aim to recommend and adjust the critical printer parameters, such as printing speed, printing pressure, and separation speed, using hybrid machine learning and heuristics optimization techniques offline and online, respectively [3, 4]. The experimental results indicate that by advising and adjusting printing parameters, PAM and POM can improve production quality by more than 60% in the Cpk. PDM identifies potential printing failures to optimize process quality

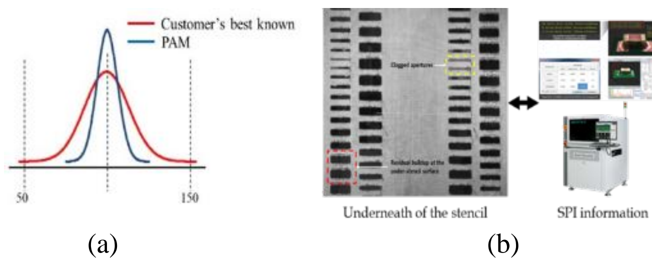


Figure 7.Application of solder printing modules (a) PAM effectiveness (b) Smart residue buildup prediction

and minimize downtime [5]. The experimental results indicate that the PDM is capable of predicting various types of defects with an accuracy of greater than 87 %. The CPC analyzes the SPI data to determine the amount of residue on the stencil undersurface and evaluate the stencil cleaning profile and cycle control [6]. The CPC improves the robustness and quality of the cleaning process by 34% and 10%, respectively, compared to the best-known cleaning parameters. For instance, Figure 8. (a) Illustrates the expected outcome of applying printing modules while showing the AI-based residual prediction.

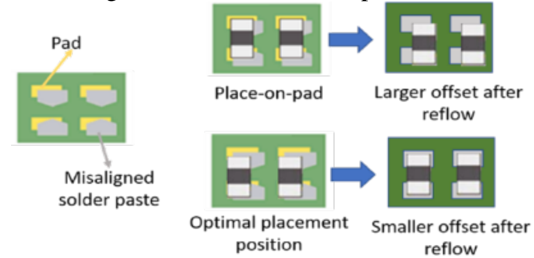


Figure 9. The illustration of the optimal placement position in the MOM

The mounter optimization module (MOM) and the mounter diagnosis module (MDM) can be used during the P&P procedure to optimize the P&P machine's parameters automatically. The final offsets of the components are predicted in the MOM framework using a hybrid AI model based on data collected by SPI, Pre-AOI, and Post-AOI machines. MOM can determine the optimal placement with the least post-reflow misalignment possible. The experimental results indicate that MOM can reduce final misalignments by 18% compared to a conventional placement method (i.e., placing a component on the pad center). Figure 9 represents a visual illustration of the mounter placement optimization. MDM is a preventive and prescriptive maintenance method that utilizes operational and AOI inspection data from P&P machines to determine the root causes of P&P defects and to prevent future failure. MDM can identify the known root causes of certain defects, such as improper nozzle size and nozzle contamination, with an accuracy of 84.5%. It demonstrates that when an abnormality is detected using AI-based diagnosis algorithms, various mounting defects can be detected and classified automatically with higher level of the accuracy.

The goal of the reflow setting optimization process is to determine the best reflow oven temperature settings that ensure the final quality of the PCB products by fine-tuning the actual thermal profile to the manufacturer's target profile.. As a result, the tuning process undertaken by the reflow engineers is time-consuming and costly. We propose an automated recipe optimization model for reflow soldering based on the thermal profile of the printed circuit board and its recipe. First, the initial recipe collects the thermal profile and the recipe and then proposes a simulation model based on the relationship. After that, an AI-based model is used to generate an optimal recipe that minimizes the difference between the simulated and target temperature profiles. The AI-based optimization enables us to achieve 97% fitness in the given target profile within an hour. The AI-based model increases the degree of automation, resulting in time and labor savings. In the future, data from multiple inspection machines will be integrated to improve the reliability of the reflow optimization process.

Summary

Due to the small size of small-scale electronics products, SMA processes have become significantly more complicated to maintain high-quality PCB products. Theoretical interpretations of SMA processes can be complex due to numerous uncertain variables. SMA processes can be

intelligent and adaptable to changing environmental conditions with the help of AI and big data. The quality of the final printed circuit board can be improved while maintaining optimal control parameters throughout the SMA processes. Automated and intelligent systems enable the next level of electronics manufacturing, which accelerates the manufacturing of customized products by leveraging data and information from end-users via edge/cloud computing.

V. Deterministic Directed Micro-assembly Printers – a PARC Example

Large forces are driving systems to be built with many, small, heterogeneous parts. Monolithic semiconductor integration in a single fabrication line is extremely expensive and limited to very few materials and processes, so the dominant approach to building systems is assembly of heterogeneous parts from disparate process lines. Miniaturization drives demand for smaller and smaller components. Parts less than a millimeter, and even down to micrometer scales need to be handled efficiently to enable new systems architectures and performance, optimize use of expensive material and devices, and enable efficient modular design with libraries of chips. The display industry is attempting to integrate millions of LEDs (5um to 150um) into next generation displays from a library of new microLEDs, and possibly driver chips, and is thus poised to be the first million chip system at commercial scale. Photonics, integrated circuits, flexible electronics and large area sensor systems are other sectors which are increasingly leveraging integration of many, small, heterogeneous parts. High throughput is needed to enable future internet of things and large area electronics needs.

Current assembly approaches have challenges scaling to small, heterogeneous parts with high throughput. Mechanical approaches are limited by slow scanning (pick and place, laser, stamp), very special die fabrication (stamp, fluidic assembly, and laser) or are not able to sort chips (traditional fluidic assembly, stamping). Fluidic assembly has particularly low cost and high throughput potential but is traditionally performed with fixed templates, is not deterministic (stochastic), and is not a digital or heterogeneous process. Laser printers use electrostatic trap templates to assemble small toner particles at 10^9 per hour, several orders of magnitude faster than current assembly approaches, showing that electrostatics has strong scaling potential. However, laser printers do not control the orientation or sort, nor have enough yield to address electronics applications.

PARC, a Xerox company, is developing a new assembly method which aims to leverage the scalability of electrostatics while combining deterministic control, to enable a new manufacturing tool for integrating and sorting many small, heterogeneous parts into next generation systems Figure 10, Figure 11. The process starts with pre-fabricated chips which are singulated and placed into solution. An active matrix electrode array, similar to the backplane of a display, is then used to generate dynamic electric force fields which manipulate the chips. The force patterns are designed to sort, orient and assemble the chiplets into programmable patterns. Closed loop control via optical tracking of the parts and a computer-controlled planner dynamically controls the force patterns and thus the chip positions. The process is deterministic as the computer knows each chip's location and determines its target location, and thus has the ability to move some chips away from the target assembly area, such as those which have been marked bad by a previous wafer scale testing step, or are upside down. The process can also do simultaneous heterogeneous assembly, where different chip types are assembled at the same time. This is important because this could reduce the number of transfers needed which is a costly step. After assembly the arrangement of chips can be transferred to a final substrate with a continuous feed process to enable very large substrates, or with a flat stamp transfer for wafer scale applications. Interconnects and other standard post processing can then be applied.

An early stage prototype of the system has been built and used to demonstrate feasibility and future scalability of the new process. Automated computer controlled assembly of 150um silicon chiplets have been assembled from a reservoir of chips and transferred with an intermediate transfer roller to a final rubber substrate to form an array with a continuous feed process Figure 12. Small chips (15um) and heterogeneous chips can be assembled Figure 13. Larger die (200um) have been interconnected after final transfer. Micrometer scale registration has been demonstrated Figure 14. As the approach uniquely moves individual chips laterally with different patterns, close packing of chips for high bandwidth chip to chip communication is possible. Single chip experiments show chip translation speeds of 6 mm/sec and above are possible Figure 15, suggesting the full system could achieve such speeds if the control systems software and electronics are improved. Like a laser printer, the architecture can be stitched to enable wider systems, including replicating control systems where each handles ~10^3-10^4 chips in parallel. This suggests throughputs of 10^6-10^8 per hour could be theoretically achieved if scaled, enabling designers to build future systems with many heterogeneous small chips with the low cost of printing but with the control of pick and place.

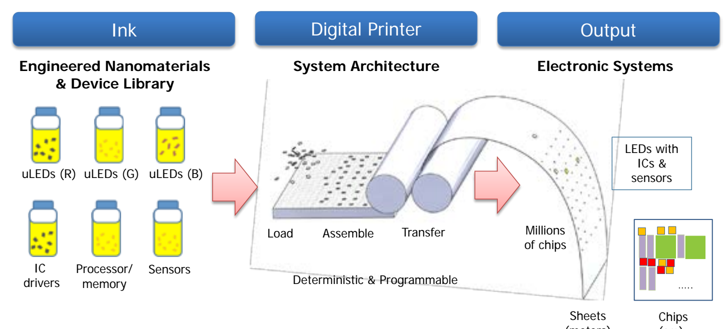


Figure 10. PARC's vision for using a programmable micro-assembly printing process to make heterogeneous, integrated systems such as smart LED displays with circuits and sensors. A general process which can accommodate a wide variety of chips from different foundries are assembled into circuit patterns and then transferred to a final substrate for subsequent interconnects. The transfer process can be continuous feed for large area applications or stamp transfer for smaller, wafer scale applications. Ref: Rupp (SID 2021)

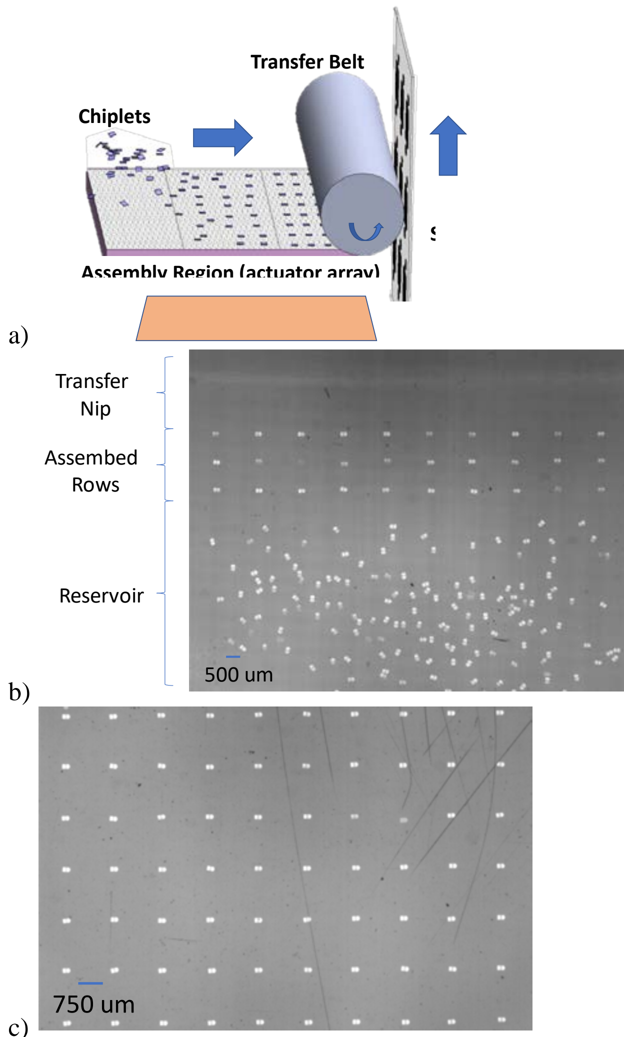


Figure 11. a) Schematic of assembly and transfer system. b) Automated assembly and orientation control of 150 um Si chiplets (made by Sandia National Labs) on a 50um actuator grid (viewed from under the array with the camera in Figure 1a),, showing the reservoir of chip as they are directed along the actuator array to form rows near the transfer nip. c) A 7x10 array at 1.5 mm pitch on a final rubber substrate, after transfer from the intermediate electrostatic transfer belt. (Ref: Rupp (ECTC 2019)

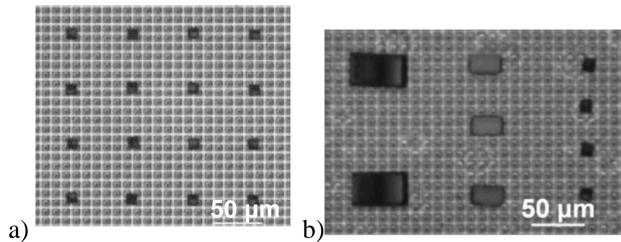
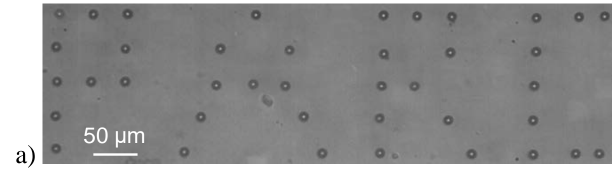


Figure 12. Small chip assemblies on the 10 um pitch electrode array. a) 16 chiplets of 15 um size arranged in an array, and b) heterogeneous assembly of chips of width 15 um, 30um and 50um. c) Larger LEDs (~200um) energized after assembly, transfer and interconnects on a final substrate. Ref: Rupp (ECTC 2019)



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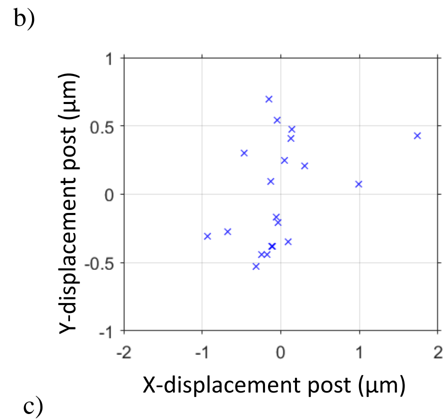

Figure 13. Stamp transfer of a) 10 beads on a PDMS stamp and b) a heterogeneous assembly of metal (dark) and dielectric (light) 10 µm beads after a second transfer from a rubber stamp to a final glass substrate. c) The overall registration error from the intended targets in b) are less than 1 µm. Ref: Plochoweitz (Transducers 2019).

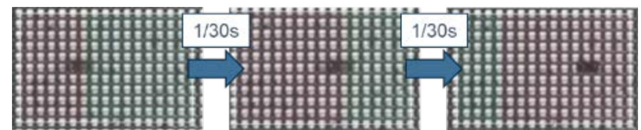

Figure 14. ***Long range particle motion. Particle is measured moving multiple electrodes over a single video frame with an average velocity of 6 mm/s. Chip is 50um x 100um. The actuator grid pitch is 50um. Ref: Rupp (SID 2021)***

VI. Conclusion

As we have shown, there are many ways to use smart manufacturing techniques. The use of data to perform analysis on how the manufacturing processes are drifting has always been used in Cp and Cpk charts to show if a process is in or is not in control. The use of AI and Machine learning techniques to not just see a chart to show where the process is going but to make use of this data and to use it to make the corrections needed to adjust the process in real time. This will ultimately make the products we sell not only less expensive but also to be better quality.

VII. ACKNOWLEDGMENTS

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Professor Park is an expert in Modeling and Simulation for electronics components and systems integration. His contributions have been recognized many international awards and citations. He has contributed in various 2.5D/3D package development, MEMS packaging, reliability assessment of assemblies and systems, and smart electronics manufacturing. He has more than 200 technical publications and holds 4 US patents. Dr. Park served for several technical committees including a member of JEDEC 14-1 Reliability Committee, co-chair of iNEMI Modeling and Simulation TWG, chair of “Electronics Packaging” council in Society of Experimental Mechanics, and an associate editor for ASME Journal of Electronic Packaging. Professor Park has been helping consumer electronics and packaging companies as a consultant.