











Call for Abstracts - Fourth Annual REPP

(Please submit by August 15)

Symposium on Reliability for Electronics and Photonics Packaging

Reliability, Failure Modes and Testing for Integration of Electronics and Photonics (SiPh)

General Chair

Przemyslaw Gromala, Bosch **Technical Program Chair** Tiwei Wei, Purdue University

Program Committee

Haohui Long, Huawei Gnyan Ramakrishna, Cisco Richard Rao, Marvell Tech. Farnood Rezaie, Cisco Eric Ouyang, JCET Global Ranjan Rajoo, GlobalFoundries Ninad Shahane, TI Sanketh Buggaveeti, Infinera Abhijit Dasgupta, U-Maryland Xueren Zhang, AMD

Keynote Speakers

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Xueren Zhang, AMD

Europe Liaisons

Willem van Driel, TU Delft Wilson Maia, Thales

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Hualiang Shi, Meta

Administrative Chair

Paul Wesling, HP (retired)

16-17 November 2023 SEMI World Hdgtrs, Milpitas, CA USA

REPP'23 is planned to be a **hybrid event**, with both in-person and WebEx participation

This symposium will focus on quantified reliability, accelerated testing and probabilistic assessments of the useful lifetime of electronic, photonic, MEMS and MOEMS materials, assemblies, packages and systems in electronics and photonics packaging. This includes failure modes, mechanisms, testing schemes, accelerated testing, stress levels, and environmental stresses.

The intent is to bring together electrical, reliability, materials, mechanical, and computer engineers and applied scientists to address the state-of-the-art in all the interconnected fields of electronic and photonic packaging, with an emphasis on various reliability-related aspects: design-for-reliability, manufacturing, reliability modeling and accelerated testing.

Proposals for presentations in the fields of Reliability for Electronic and Photonic Packaging are solicited, for either in-person or remote presentation, addressing the following technical areas:

At the Component/Sub Component Level

- Lasers, Diodes, Fan-out IC, PLC fabrication challenges and developments
- Multiphysics interactions
- 2.5D/3D/Heterogeneous integration
- On-chip integration of subcomponents
- Wafer scale technology

System Level of Integration

- Integration challenges for electronics and photonics copackaging
- Optical coupling and index matching at the system level
- Thermal management challenges at the system level

Testing for Yield

- Burn-in testing
- Testing methods at subcomponent level
- Testing methods at co-packaging level
- Methods and methodology to track yields
- System level testing and yields at scale

Co-Design and Simulation

- Modeling schemes
- Global optimizations

Up to three travel grants of \$1,000 are available for grad students presenting their work.

Accelerated testing

- Accelerated testing techniques and methodologists for different electronic, photonic and MEMS technologies, designs and applications
- Accelerated testing and how it translates to Field conditions and deployment
- Highly focused and highly cost-effective failure-orientedaccelerated-testing (FOAT) to understand the physics of failure

Failure modes/Failure Mechanisms

- Accelerated models
- Sub-component specific FA modes
- FA techniques
- Material characterization and failure criteria

Abstracts or proposals should include a title and a summary of **200-500 words** with one or two optional figures or diagrams, clearly showing the relationship of the talk to the topics of the Symposium. Acceptance of proposed presentations will be announced by **20 September 2023**. Most presentations will be 30 minutes long, supplemented by keynotes and invited talks. **No formal papers will be due**; however, speakers may submit an extended abstract suitable for use by attendees. Your proposals may be submitted at https://attend.ieee.org/repp

You may also email your proposal to Tiwei Wei, REPP Program Chair, at wei427@purdue.edu

View videos of 30 talks from 2022 REPP: View Videos of 2022 Talks

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