Institute of Electrical and Electronics Engineers, Inc.

Electronics Packaging Society

Strategic Plan

2022 – 2027

Approved 9 November 2019

Contents

Updated June 2023

1) Introduction

Governance and the operations of the society are detailed in its Constitution and Bylaws and its Operations Manual. These two documents can be found at https://eps.ieee.org/about/governance.html.

This document details the societies strategic plan and actions for its implementation for the 5-year period 2019-2024.

2) Mission and Vision

Mission: Electronics Packaging Society core purpose is to support innovation through dissemination, education and convening various forums in electronics packaging for our membership worldwide, the wider engineering community, and for the benefit of humanity.

Vision: The Electronics Packaging Society will continue to be essential to the global electronics community both in academia, research institutes, and industry. Our society will be universally recognised for its contributions to electronics packaging and the impact this has in improving global conditions.

3) Field of Interest

The field of interest of the Society is described in the Societies Constitution, Sec 3 A, and reads as follows:

The EPS field of Interest includes all aspects of packaging and integration of electrical, electronic, optoelectronic, biological, micromechanical and sensing components; addressing signal and power delivery, material aspects, thermal and structural design and reliability. The Society drives science, technology, engineering, test, modeling, simulation, design, manufacturing, interconnection and performance of integrated components. It sponsors and provides electronics packaging education and reports on electronics packaging research worldwide.

4) Electronics Packaging Society Landscape

The society has 2400 members worldwide. It supports 25+ conferences annually and has three regional conferences: ECTC (USA), ESTC (Region 8) and EPTC (Region 10). Technically the society is served by 12 technical committees and it is engaged in 8 IEEE initiatives and 5 joint activities with IEEE councils. Details of these technical committees, activities/initiatives, and our chapters are provided in the appendix.

With over 5000 engineers attending its conferences annually, and over half a million Xplore downloads of its publications each year the society is in a strong position. But given the changes in the electronics industry (see technology landscape below) and the opportunities this provides, it is important that the society plans to align itself with these opportunities. Hence this strategic plan is timely to ensure these opportunities are addressed through the goals, action plans, and timelines for the period 2019-2024.

a) Technology Landscape – where are we now?

Packaging of Electronic Devices
Electronics enabled systems use printed circuit boards (PCB's) to mechanically connect multiple chips (processors, GPU's, memory, FPGA's, etc) together and provide the circuitry

for signal and power transmission. Electronics Packaging is a multi-disciplinary field of science and engineering that designs, fabricates, and tests these packaged chips and the systems they contribute towards. An electronic package must protect the chips from mechanical damage (due to temperature, vibration, etc), ensure devices are connected to the PCB and other devices to enable signal and power delivery and provide the ability to test each device. Figure 1 details a typical package consisting of an epoxy glass PCB, a substrate, a heat sink, and a silicon chip connected to the substrate and the PCB through solder joints.

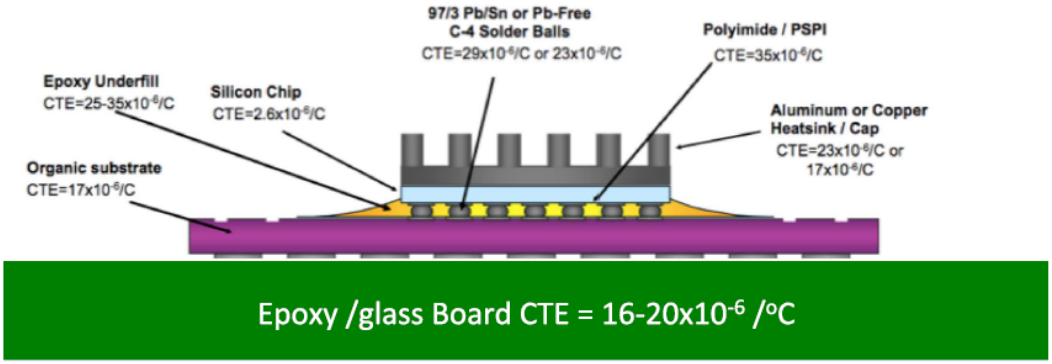


Figure 1: An Electronic Package

Over the last 40+ years, the development of electronics enabled systems with greater function and performance has been driven by Moore's Law (silicon scaling). Figure 2 Details the relative scaling over time for both silicon and packaging features. For example, in 1971 packaging features (e.g. solder bump pitch) and minimum silicon features (transistors) were about 400um and 15 um respectively. Today bump pitch is in the 110-110um range (scaling of 45x) and minimum silicon features are less than 15nm (scaling of 1000x). To bridge this interconnect gap requires technical innovations in electronics packaging.

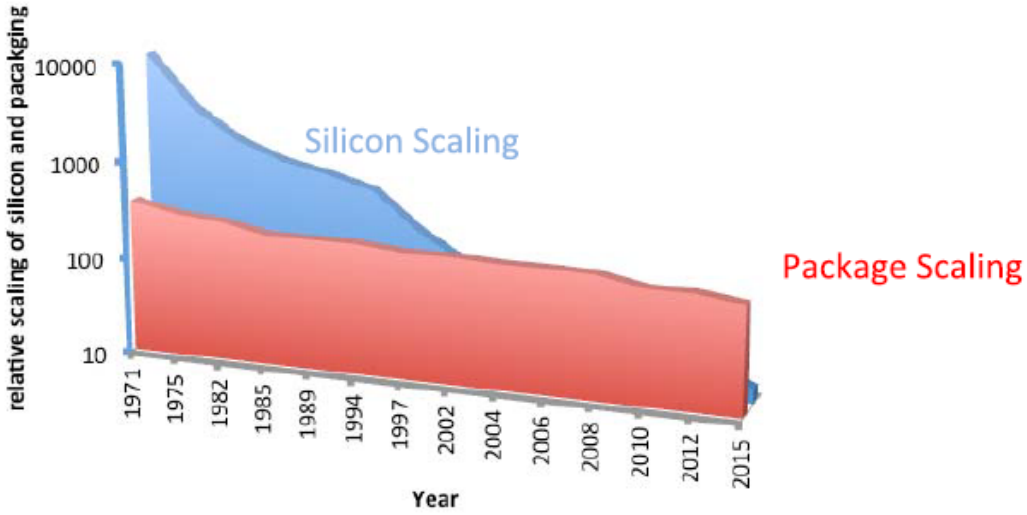


Figure 2 Silicon Scaling vs Package Scaling (1)

Business Considerations – the end of Silicon Scaling

The semiconductor industry has always been controlled by the front end, i.e. IC chip design and fabrication. For much of the 20th century the back end, "Packaging", has been a necessary, but not critical, afterthought. As detailed above, the industry has moved forward

for the past 40 years based on transistor scaling (figure 3) which has provided smaller features and thus more chips per wafer and lower costs.

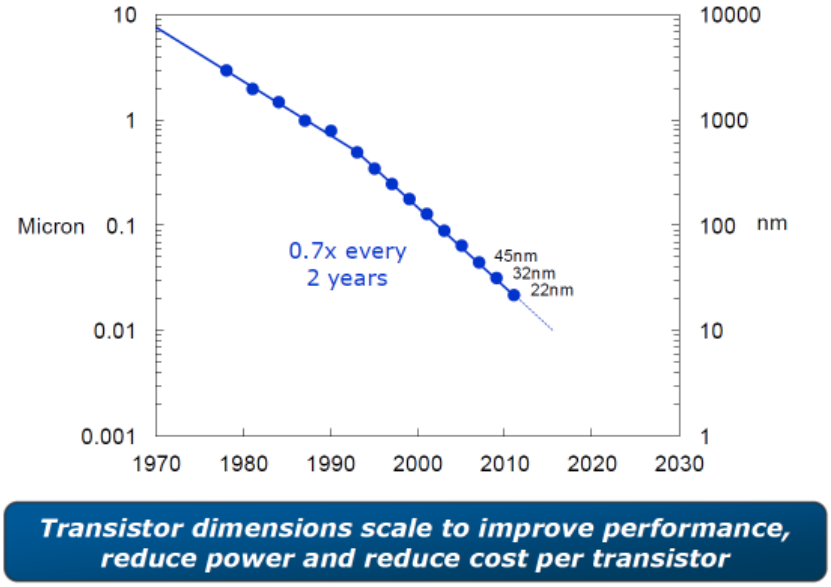


Figure 3: Scaling has Driven our Microelectronics Industry

As we passed 22nm, it has become well accepted that scaling has come to an end for all but a few. Technically a few may still be able to move forward, but financially very few, if any, beyond TSMC, Intel and Samsung, can afford to do so internally, or at fabs where the design and production costs only makes sense for a very few very high-volume products (see figure 4). This has forced more IC companies to go fab light or fabless and move to packaging driven product differentiation.

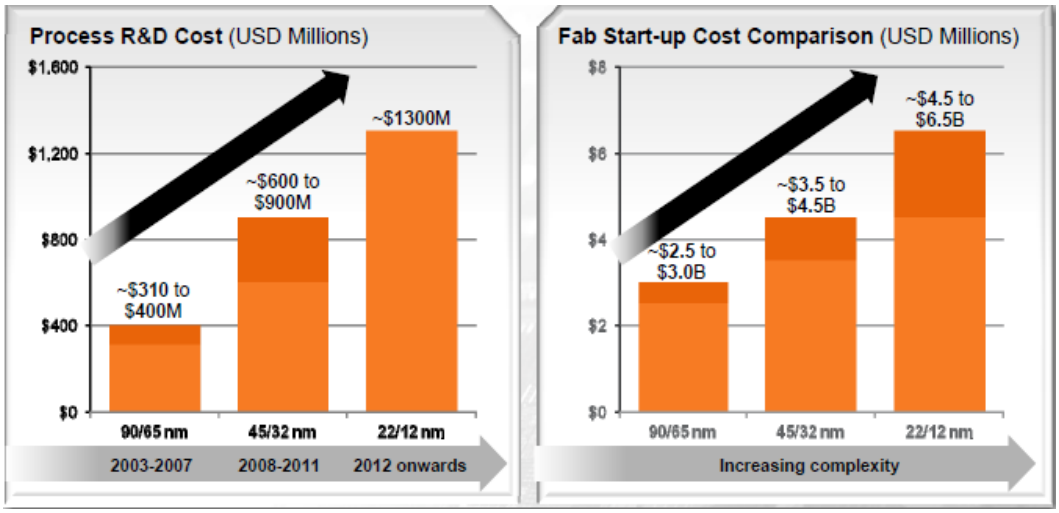


Figure 4: The Cost of Scaling has Become Prohibitive

With an end coming to CMOS scaling something new will be taking its place. It is not clear what that new technology will be, but it is certain that it will take more than a decade to happen. The technology that is chosen to replace CMOS will determine where packaging will go. Until then we will deal with evolutionary changes. For most, customization will come from packaging differentiated solutions NOT the use of the latest node chips. Basically, chips will be put into high density sub modules (in the 1990s these were called multichip

modules and now called SiP (system in package)). If technically and economically viable they will be stacked onto each other (3DIC) and if not, they will be put onto high density interposers getting the shortest interconnect possible between the chips.

Who is Doing the Leading-Edge Work?
In the 1990's the leading-edge packaging work was undertaken at IDMs (Integrated Device Manufacturers) such as IBM, NEC, Fujitsu, DEC etc. because they were the only ones needing advanced packaging for their advanced machines. Post 2000, the torch was passed to IDMs like Intel and OSATS (Outsourced Semiconductor Assembly and Test) suppliers such as ASE, SPIL, Amkor and STATS ChipPAC. As we approach 2020, we are also seeing the leading-edge in packaging move and grow in the the foundries such as Intel,TSMC and Samsung who have come to realize that scaling is ending, and that packaging now has a significant performance contribution to make for their customers.

Recent Technology Changes
Miniaturization has driven microelectronics packaging since the early 1990's. Continued consumer product miniaturization has required high-density packaging & interconnect technologies for many applications (see figure 5).

Figure 5: Miniaturization Drives our Microelectronics Industry

Packaging technology through the decades (see figures 6 & 7) has evolved to meet the requirements of miniaturization while at the same time offering more I/O by moving to area array packages. While early surface mount (SMT) packages were peripheral lead frame-based devices, the later BGAs were based on area array. In a similar fashion, the major Leading-Edge Chip Scale based technologies and wafer level packaging technologies were/are, for the most part, all area array based.

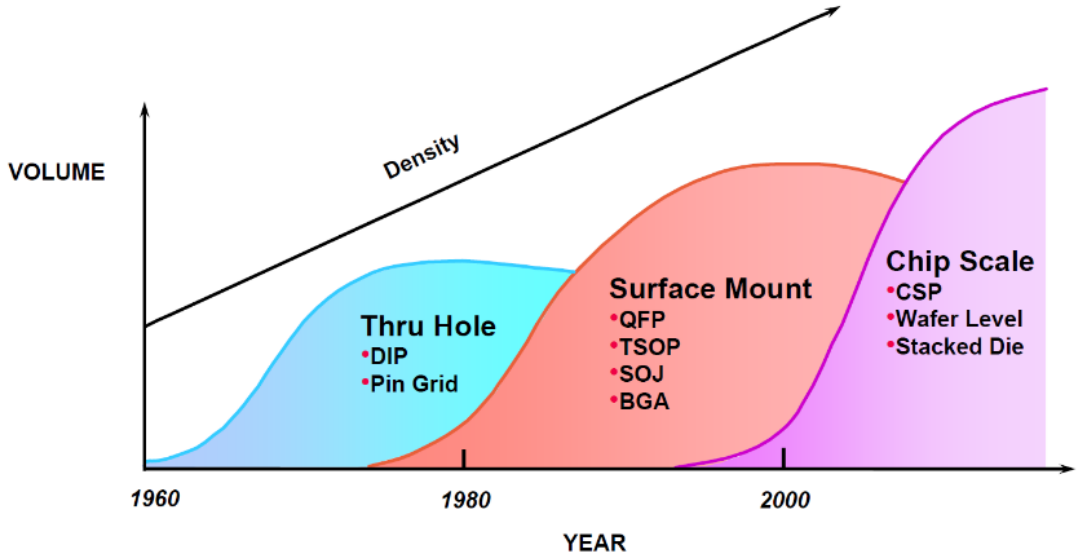


Figure 6: Main Packaging Changes Thru the Decades

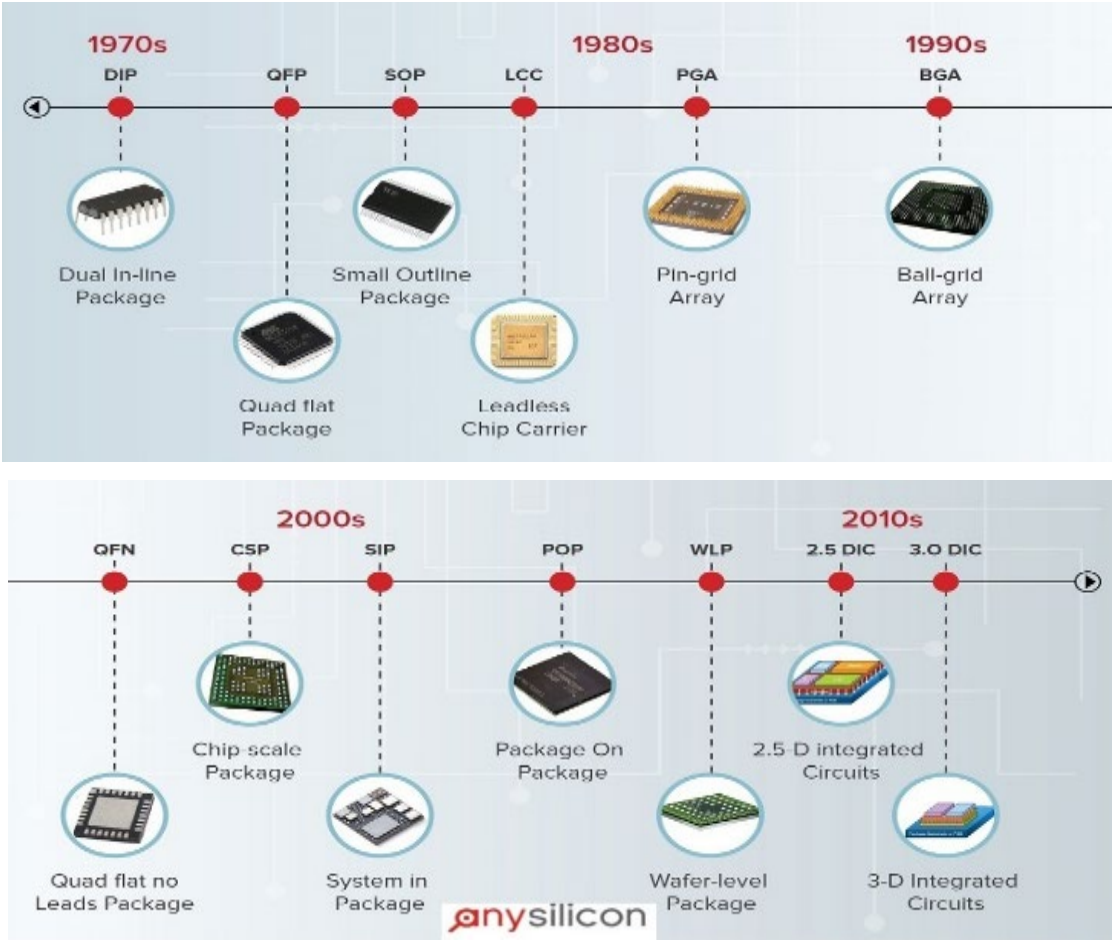


Figure 7: Packaging Options Thru the Decades

Each package type has a “sweet spot” combination of cost, performance, form factor and reliability, driven by:

What to consider in deciding on package type	
Cost	Electrical performance
Power dissipation	Thickness, weight, PCB area consumption
Board level reliability (BLR)	Technical maturity.vs. risk in HVM
Testability	

The original WLP packages of the late 1990’s and early 2000’s was all fan-in based, i.e. all the area array solder ball connections had to be located below the chip and within the dimensions of the chip. As it became clear that this was limiting the technology, the industry developed fan-out solutions that required so-called “re-configuration” by placing known good ICs active face down on a foil and over-molding them. These wafers are then flipped and processed in the wafer fab with redistribution layers (RDL) / ball placement and diced. The first such commercial products were manufactured by Infineon in 2009. Recent advancements are exemplified by TSMC’s InFO technology which produces package interconnects as fine as 2um.

After commercialization of the WLP, further miniaturization had to come from the 3rd dimension as detailed in figure 8.

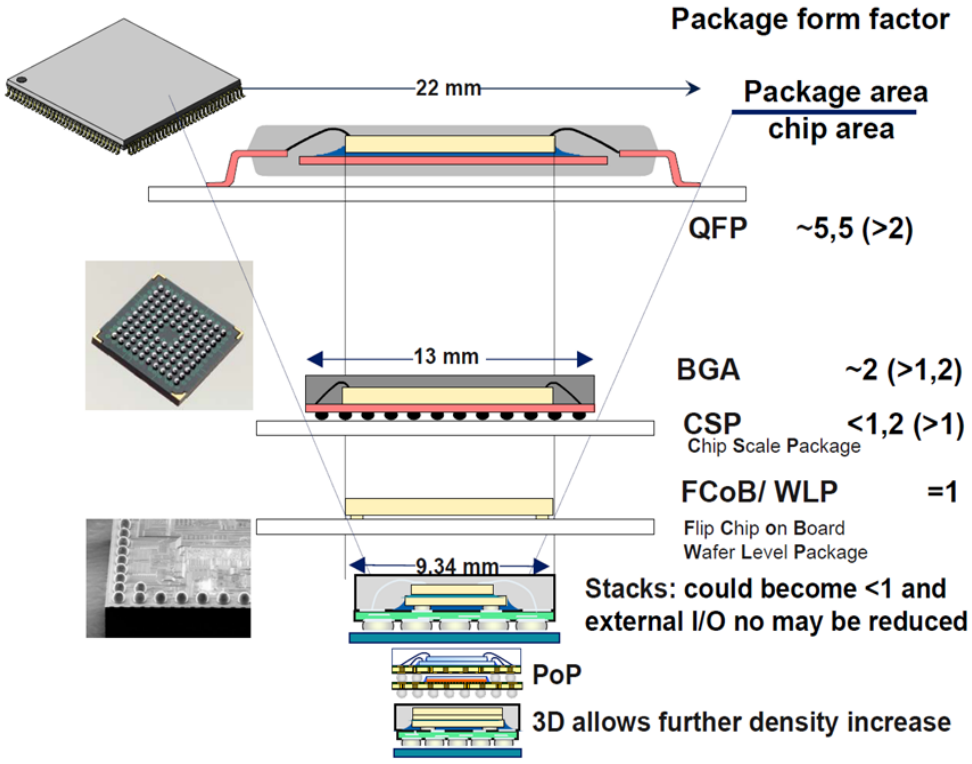


Figure 8: 3D – The Natural Next Step in Miniaturization

In 2017 Sony announced the Industry's First 3-Layer Stacked CMOS Image Sensor (90 nm generation back-illuminated CIS top chip, 30 nm generation DRAM middle chip, and a 40 nm generation image signal processor (ISP) bottom chip for Smartphone cameras as shown in the cross-section below.

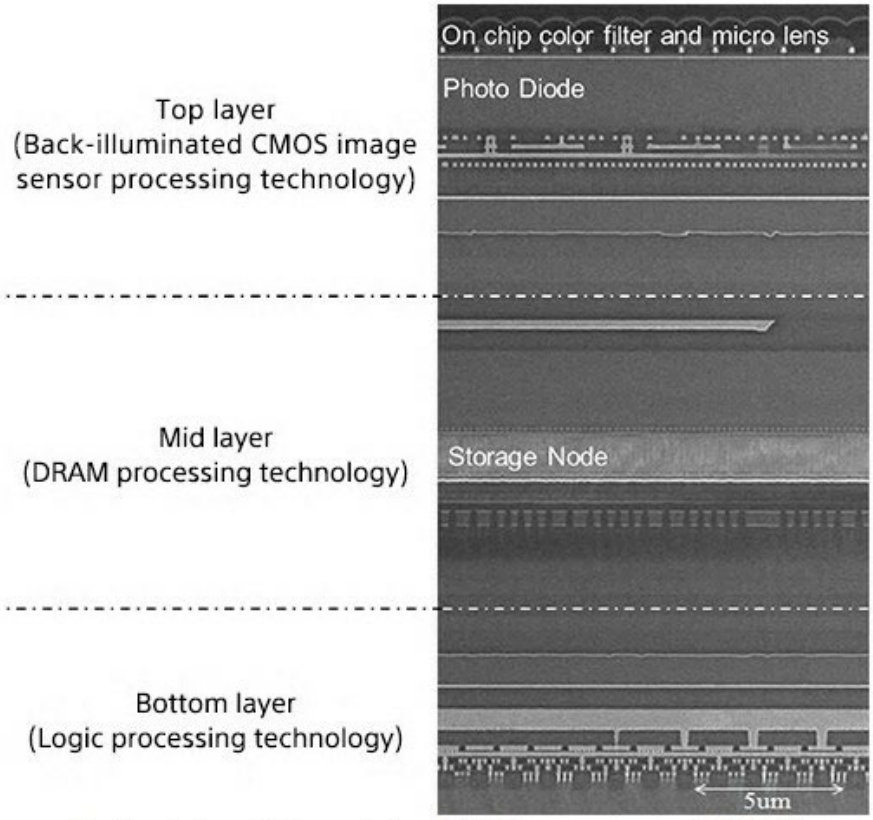


Figure 9: Sony 3 Layer CMOS Image Sensor Technology

After nearly two decades of development and standardization, memory is now being produced by the major memory suppliers in 3DIC format giving product designers high-density low latency memory options such as HBM (high bandwidth memory) which is being produced by both Hynix and Samsung.

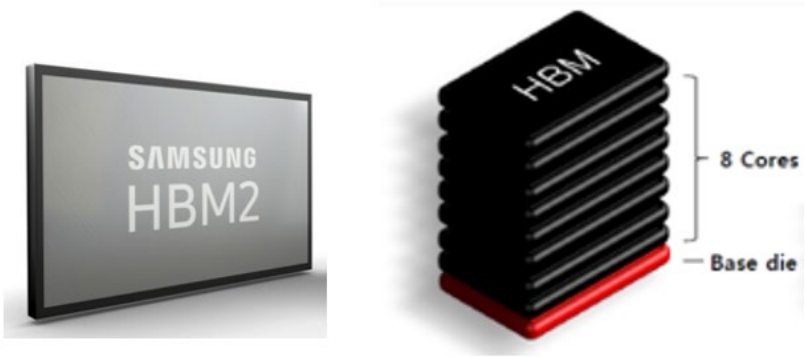


Figure 10: Samsung and Hynix Standardize High Bandwidth Stacked Memory (HBM)

Another packaging trend that we have seen taking hold has been dis-integration. While past decades have been driven by more function being created on-chip, the so-called system on chip (SOC), we now see some reversing of that trend and breaking down the chips into smaller pieces (chiplets) and reassembling on a high-density interposer (figure 11). This was first done in the early 2010's by Xilinx who could no longer yield larger and larger FPGAs.

Figure 11: Dis-Integration for FPGA fabrication

This concept has since been extended to separation of functions, as shown in figure 12. This allows for each function to be fabricated in an appropriate node and allows for optimizing the process for that function; reuse of IP; and significant design speed up. We anticipate significant infrastructure development to enable dis-integration, propelled by programs like the DARPA CHIPS

Figure 12: Is Disintegration the Future of the Chip Industry?

b) Technology Landscape – Where are we going?

Data-centric Era – Next wave market growth engine

Emerging AI and 5G applications, such as intelligent manufacturing, AR/VR, connected devices and smart cars, are generating an explosion of data. This deluge of data is driving the need for an unprecedented amount of computing power, in cloud datacentres and communication infrastructures, to process numerous images, audio, video files, and business analytics workloads. To achieve high-performance and low-latency within system power budgets, wired and wireless infrastructures are expediting the migration to leading-edge technologies at a rate never seen before. Advanced heterogeneous integration technologies will unleash packaging innovations to optimize system and product performances in terms of computing efficiency and bandwidth, at low latency. The following details what we see as the technology landscape in the next 5 years for heterogeneous chiplet integration.

Chiplets Integration – 2D fan-out, interposer, and 3D technologies

Chiplets integration has been commercially realized by interposer technology and wafer level fan-out technology, in datacentre, server, and networking applications. Figure 13 shows chiplet integration of FPGA on a high-routing density interposer through side-by-side 2D interconnects. Min. line/space of 0.4/0.4 μm was used in the interposer for high-density chip-to-chip communication. The reticle size of interposer continues to grow to meet the product needs with more chiplet integration for higher and higher computing power and bandwidth.

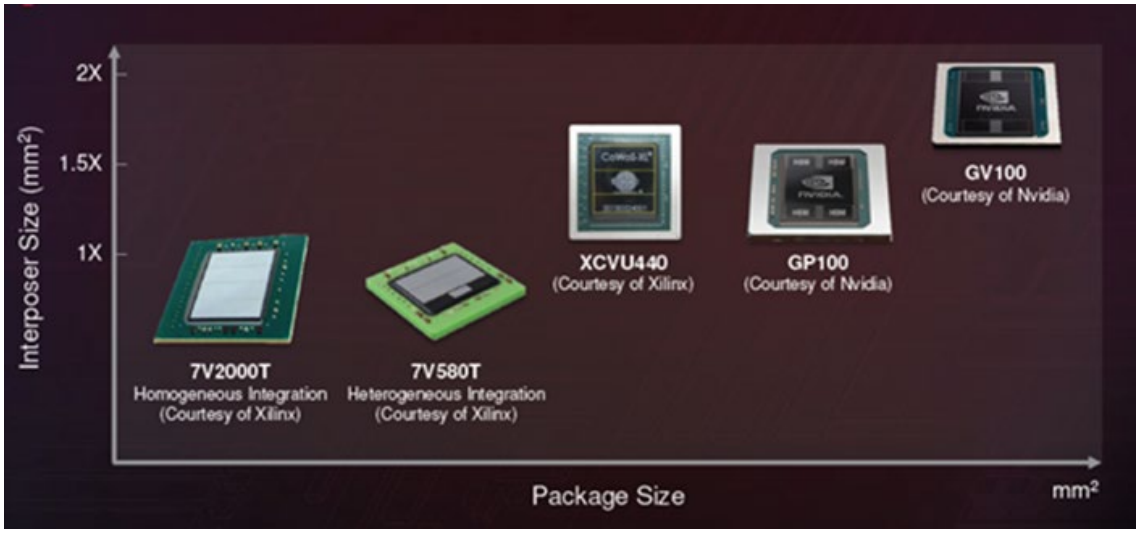


Figure 13. Chiplets integration and heterogeneous functions integration on interposer [2]

Figure 14 shows chiplet integration through 2D InFO fan-out technology for networking applications. The chip-first approach was adopted for the integration. Min. line/space of 2/2 μm was used in the redistribution layer for high density chip-to-chip communication. The reticle size of fan-out continues to grow to meet the product needs with more chiplets integration for higher and higher speed in data processing and data switching.

Figure 14: Chiplets integration through InFO technology for networking

Chiplets integration is not only realized by 2D technologies, but also realized by 3D technologies for improved chip-to-chip interconnect density and data latency in 5G and AI applications. Figure 15 shows an example of 3D chiplets integration of compute logic and I/O chip through a 3DIC interconnects. Through-silicon-via (TSV's) in the bottom I/O chip provides a vertical interconnect communication between the top compute logic chip and the bottom organic substrate. Compute logic stacks on top of the I/O chip are achieved through copper micro-bumps and flip chip assembly.

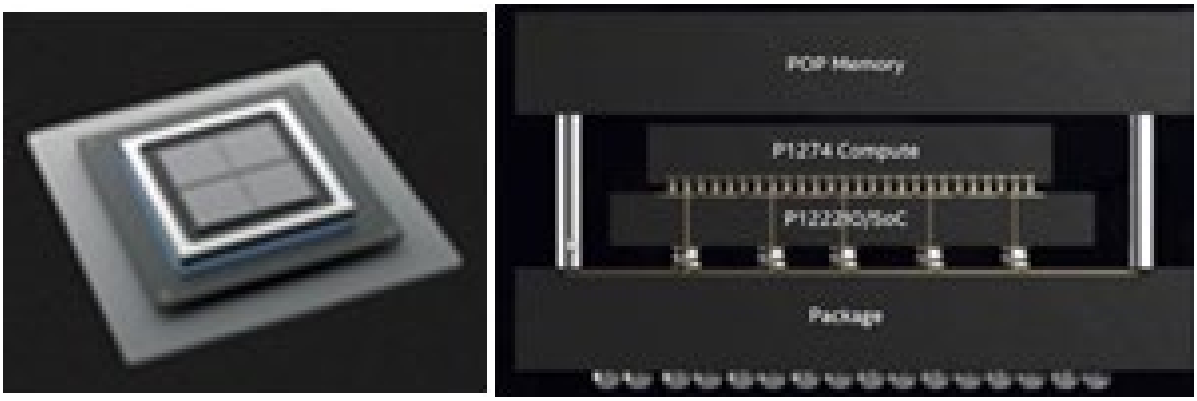


Figure 15: 3D chiplets integration through Foveros technology [3]

Figure 16 shows a 3D chiplets integration through a 3DIC stacking – SoIC (System on Integrated Chips). It provides flexible integration with multiple chip sizes, multiple stacking layers, and multiple functions. Seamless fine pitch chip-to-chip bonding improves performance and minimizes RLC parasitics. To the left is a two chiplets stacking with the same die size. To the right is a three-chiplets stacking with two smaller chiplets stacking on top of a larger chip at the bottom.

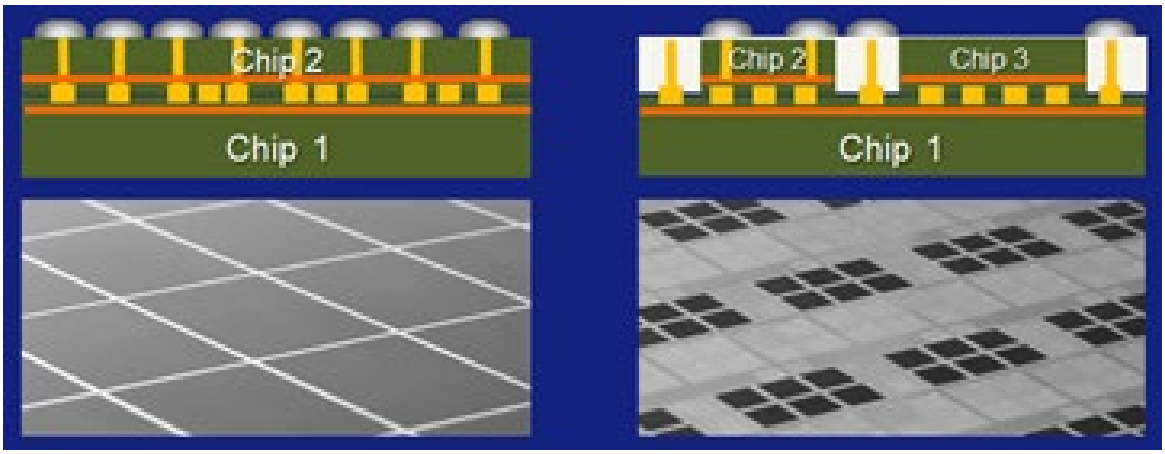


Figure 16: 3D chiplets integration through SoIC technology [4,5]

Heterogeneous Functions Integration – More Than Moore

With the die cost per unit area at single-digit nodes escalating [6], together with yield and die size trade-off, designing for multi-die chiplets becomes a cost-effective solution. Figure 17 details two generations of the AMD EPYC server processors. To the left, the large monolithic System on Chip (SoC) die has been homogeneously split into four tightly coupled die (for better yield) on an organic substrate. To the right, heterogeneous integration of two groups of four 7 nm chiplets on each side of a larger 14 nm I/O die helps optimize overall cost.

Interposer technology not only realizes chiplets integration but also realizes heterogeneous integration of different functional chips or components into a sub-system. As shown in Figure 18, a GPU chip and multiple high bandwidth memory (HBM) stacks are integrated on an interposer, for high performance computing in cloud AI training and datacentre/server applications. The reticle size of the interposer continues to grow to meet the product needs with more compute logics and HBMs integration for higher and higher computing power and bandwidth in future exascale computing.

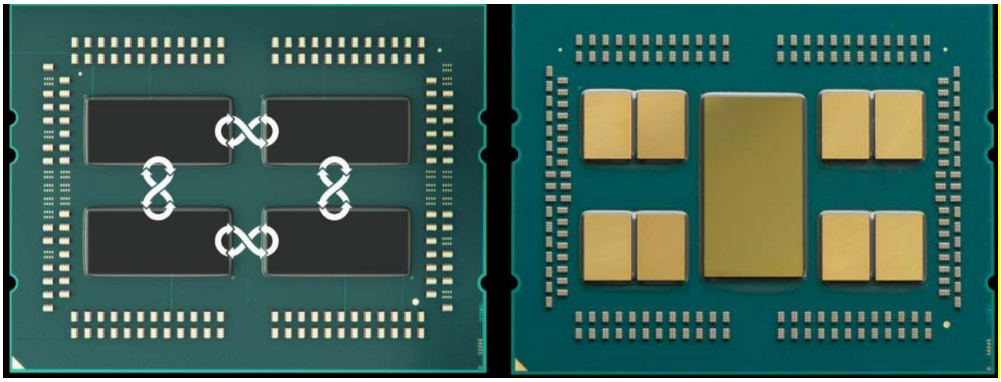


Figure 17: Examples of System Integration - EYPC Server Processors Source AMD

Components of different nodes or from different companies may be heterogeneously integrated together in one system-in-package (SiP), such as implemented in the Intel Kaby Lake G card incorporating an Intel CPU with an AMD GPU linked to 4GB of HBM2 (see figure 18).

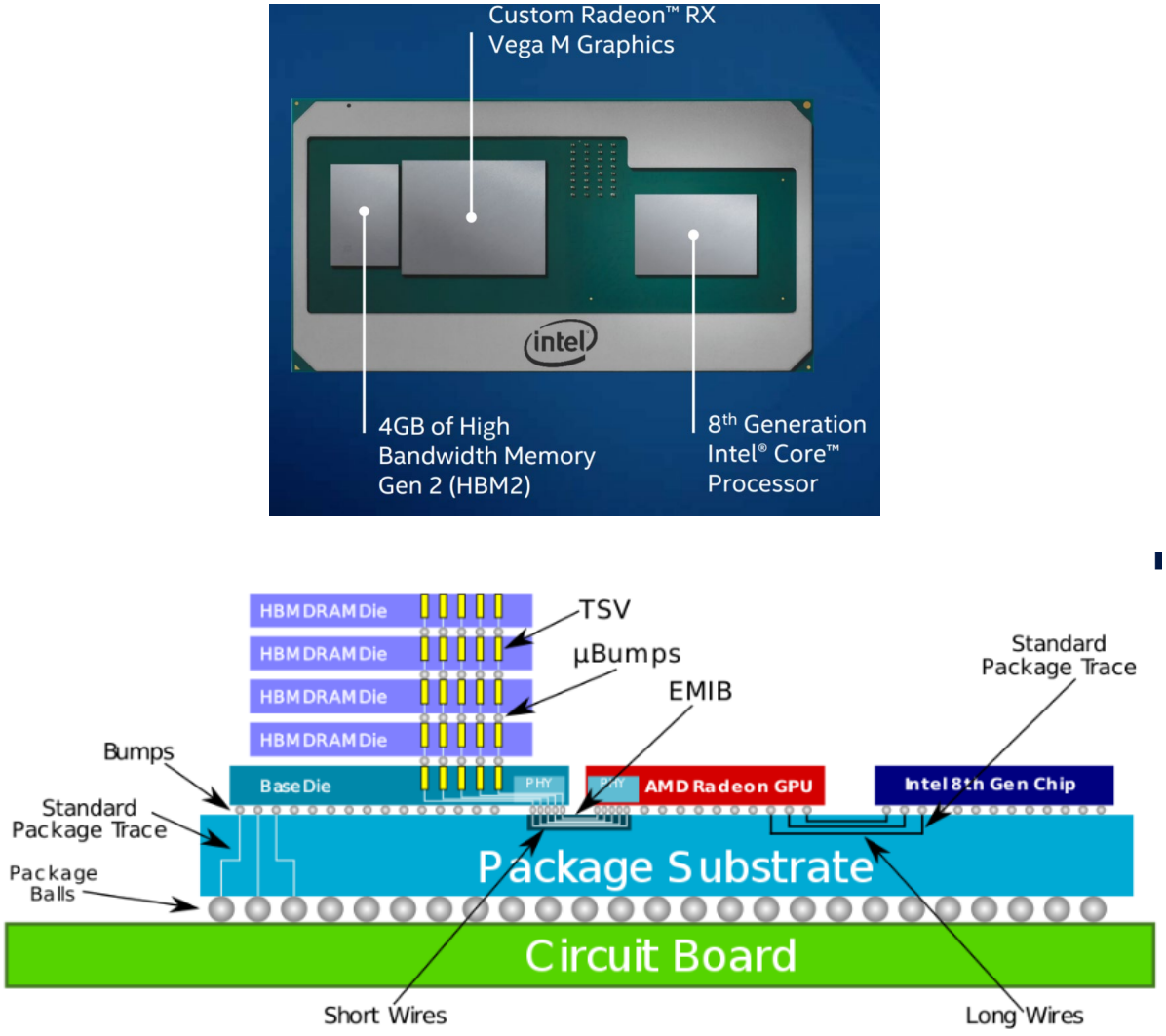


Figure 18 Intel Kaby Lake G (Source Wikichip)

The previous examples demonstrate the growing momentum for SiP in high performance computing taking a new look at system architecture and expanding innovations in our packaging tool-box. We are now seeing the “chiplet initiative” utilizing different packaging technologies for disparate system applications. As the industry goes further into single digit nodes, considerations of cost and time-to-market trading off with high-bandwidth and performance per watt consideration, means that multi-die (chiplets) heterogeneous integration is an important trend going forward [7-13].

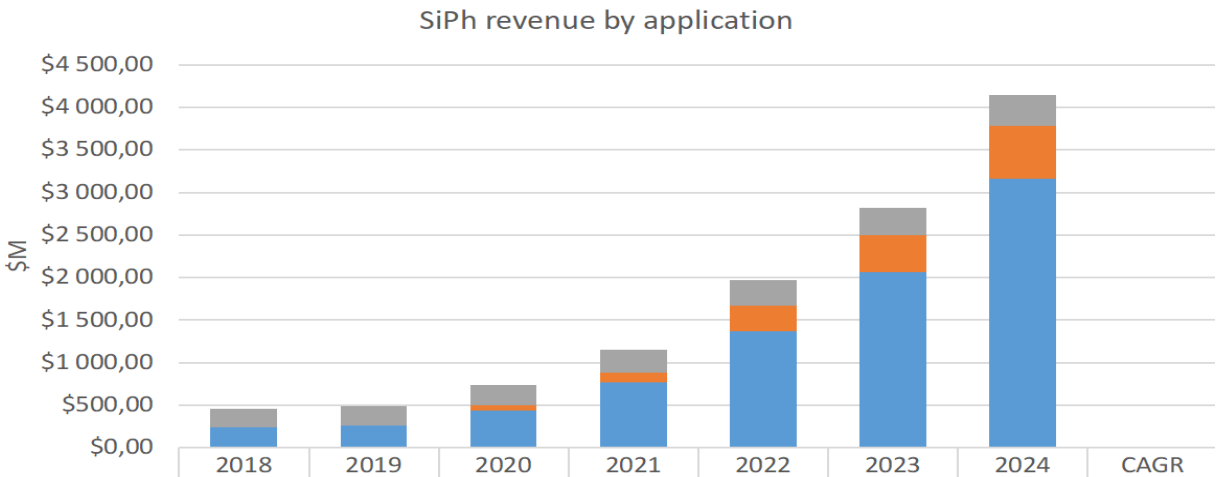
Co-Design, Modelling, Metrology & Standards
Heterogeneous Integration, Advanced Packaging, Chiplets Integration, etc, brings high complexity and challenges to manufacturing, testing, and yield control. Advanced metrology tools become important during the development of 2D/3D chiplets integration technologies. Leveraging AI to assist in defect classification and identification of fine features on topology and at embedding interfaces and interconnects is crucial in fast advancing of chiplets integration technology and manufacturing.

At present, design of the chip, package, board, and system are undertaken separately and independently. Tomorrows electronics enabled systems and packages will require co-design tools that enable chip, package, board, and system designers to work together. In addition to this, electrical design, thermal design, and mechanical design will need to be integrated and supported by multi-physics/scale modelling and simulation tools.

In terms of standards, there is a requirement for standardisation of data interfaces between layout tools and modelling. In addition to ths, heterogeneous integration requires physical standards for example size and weight of panels, etc.

Si Photonics and ASICs Co-Packaging

Si photonics, which is a category of PIC, leverages semiconductor manufacturing infrastructure to combine different photonic functionalities on the same chip. They integrate multiple (at least two) photonic functions, the optical equivalent of electronic ICs and are seeing significant growth.



	2018	2019	2020	2021	2022	2023	2024	CAGR
Long haul	$213,39	$224,06	$246,46	$271,11	$298,22	$328,04	$360,85	9,2%
5G	$0,00	$0,00	$58,00	$118,00	$300,00	$427,00	$620,00	
DCI	$241,43	$260,06	$435,52	$764,98	$1 368,23	$2 067,16	$3 163,06	53,5%

Figure 19 Silicon photonics Revenue by Application source: Yole (14)

There is industry momentum to co-package and couple Si-Photonics devices directly with ASICs on a single package. In March 14, 2019 Microsoft & Facebook jointly announced formation of the Co-Packaged Optics Collaboration (CPO). The goal is the adoption of common design elements and guidance to the suppliers in the design and manufacturing of co-packaged optics [15]. Placing the optics closer to the chip will enable much lower power electrical I/O with potential 30% power reduction at system level crucial in Hyperscale Data Centres today.

All Silicon Technology

Printed Circuit Boards (PCB's) are not an ideal technology. The use of solder joints limits the number of connections that can be achieved between the chip and the PCB. Also, as detailed in figure 1, the CTE miss-match between materials results in thermally driven stress which can impact reliability. These are just two of the issues that packaging engineers face when using PCB's. Extending the concept of the silicon interposer, there is the possibility of replacing the PCB with what is termed silicon interconnect fabric. This fabric will link chips with denser, higher bandwidth connections. It will allow chips to be packed closer together and should provide benefits in heat removal. Figure 20 details an example of this.

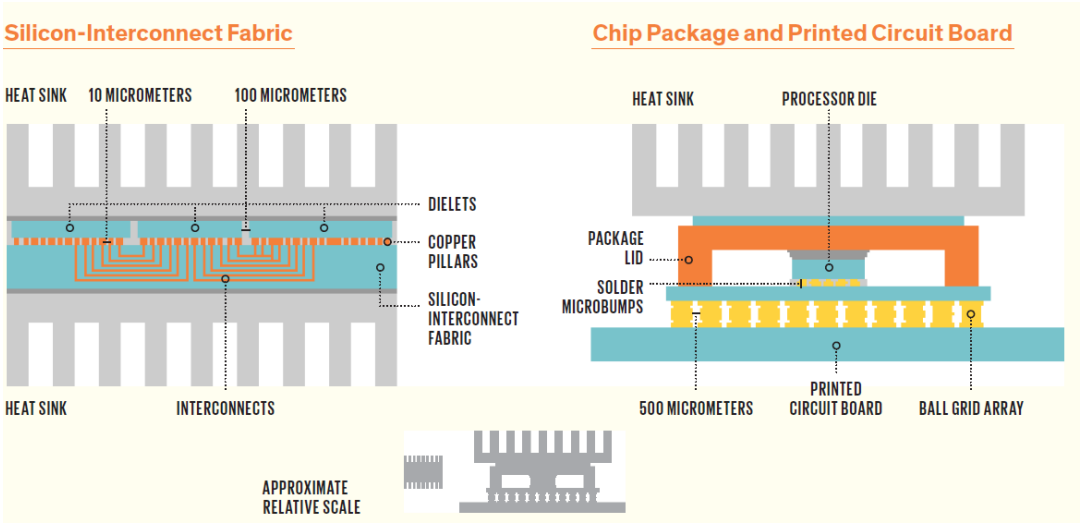


Figure 20: All Silicon Technology vs Traditional PCB based Technology (16)

Heterogeneous Integration Roadmap

The above examples of packaging technology trends provide an insight into the exciting developments and challenges that the electronic packaging community face in the future. To support our community in addressing these opportunities and challenges, the society is leading a roadmap initiative that involves contributions from academics and industry worldwide.

The mission of this Heterogeneous Integration Roadmap (HIR) is to provide guidance to the profession, industry, academia, and government to identify key technical challenges with enough lead time so that they do not become roadblocks preventing the continued progress in electronics packaging. That progress is essential to the future growth of the industry and the realization of the promise of continued positive impact on mankind. The approach is to identify the requirements for heterogeneous integration in the electronics industry through to 2034, determine the difficult challenges that must be overcome to meet these requirements

and, where possible, identify potential solutions. Further details on this roadmap can be found at:

https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html

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5) Key Stakeholders

Stakeholders who will implement this strategic plan include all members of the Board of Governors which includes the following:

Officers	Program Directors	Standing Committee Chairs	Representatives
President President-Elect VP-Conferences VP-Technology VP-Finance VP-Education VP-Membership VP-Publications	Chapter Programs Awards Programs Student Programs Industry programs Regions 1-7 & 9 Programs Region 8 Programs Region 10 Programs	Fellows Evaluation Nominations	Young Professionals Women in Engineering

The Society has Functional Teams in the areas of: (1) Conferences (2) Membership (3) Education (4) Technology and (5) Finance as well as an editorial and publications board for Publications. Each of these are led by their respective VP officer. These teams will be a key component in implementing the strategic plan and its goals and will work with

program directors and members-at -large who are contributing to the membership of each functional team.

Members are the most important people within EPS. EPS members provide much more than financial support for the Society. Through their participation in EPS activities they collectively help to drive our industry and Society forward. EPS members represent some of the most innovative people in electronics packaging, generating new ideas and concepts, as well as collaborating with colleagues around the world. Understanding the motivations for why people become members, remain members, or relinquish membership is important for the future of the Society. The strategic membership goals for EPS are focused on increasing overall membership, with specific focus on growth for under-represented member populations, increasing membership retention, and supporting and growing our local chapters.

Technical Committees (TCs) are a core attribute of EPS. Highly active and performing Technical Committees enable greater technical value to the Society's members through improved conferences, educational offerings, and relevant communications. In addition to this, easily accessible technical communication provides a service to the Society and adds clear value to members and prospective members.

Through its technical committees and initiatives, such as the heterogeneous integration roadmap, EPS has the capability to be the preferred source of strategic packaging information, given our unique combination of broad-based technical expertise and neutral, non-commercial perspective. Our goals for technology will build on the important Heterogeneous Integration Roadmap to enhance EPS stature in strategic packaging technology.

Currently, EPS has a representative to many IEEE Initiatives and Councils. These representatives may or may not be directly linked to other technical teams (e.g. our technical committees). We will increase the benefit of Initiative and Council interactions by first identifying the right interactions to maintain and initiate, and then create explicit links/coordination between the EPS representatives and the TCs.

Outreach and professional development through educational activities are among the major objectives of the EPS. The purpose of these activities is to support the professional development of electronics packaging practitioners, especially young professionals. The traditional educational offerings of the EPS have included online webinars, Professional Development Courses (PDCs) at conferences, and presentations at Chapter Meetings and other venues by the Society's Distinguished Lecturers (DLs). Recently, a Certificate Program was unveiled to allow members to document and receive recognition and credentials for professional development activities related to electronics packaging. The goals below related to education outline our plans to enhance and strengthen existing educational activities, as well as to develop new educational offerings.

EPS supports several conferences worldwide with our US-based flagship conference ECTC is seeing significant growth in attendees and exhibitors. There is potential to build such growth in Europe and Asia through our flagship regional flagship conferences ESTC and EPTC respectively. Our goals related to conferences aim to achieve this as well as promote EPS at all our conferences and identify best practices for the procedures used to make awards at our conferences.

The following details the 23 goals together with their action plans, metrics, and timelines identified by our functional teams and editorial board. These will direct future growth and development of the society during the next five years.

6) List of Strategic Goals for years 2019-2024

Goal	Goal Description	Under Purview
1	Grow EPS membership to 3000	Membership FT
2	Achieve and maintain membership retention rate of 80%	Membership FT
3	Develop new chapters and revitalisation existing chapters	Membership & Education FT's, Regional Directors
4	Increase Membership in Under-Represented EPS Member Populations	Membership & Conferences FT's & EPS conferences
5	Continue to increase the effectiveness of Technical Committees	Technology FT
6	Continue to enhance the quality and depth of technical content to the EPS/Packaging communities	Technology FT
7	Position EPS as a preferred information source of disruptive packaging technology	Technology FT
8	Optimize the value of outreach by TC's to conferences, societies, local chapters, standard activities, in and beyond EPS	Technology FT
9	Reduce turnaround time from paper submission to first decision to 25 days.	Editorial Board
10	Improve Impact Factor of CPMT Journal to 3.0	Editorial Board
11	Improve Reviewer Pool	Publications Board
12	Enhance geographic and gender diversity of Associate Editors	Editorial Board
13	Support the IEEE's strategy to expand its presence in the Open Access	Editorial Board
14	Grow attendance and exhibitor numbers at ESTC by 50%.	Conferences FT & R8 Director
15	To apply conference award best practices given at our Global (ECTC) and Regional Flagship conferences (EPTC, ESTC) that include but are not limited to the type of awards, procedures on how these awards are selected, and the dollar amount of the awards.	Conferences FT & Program Director - Awards
16	EPS to provide Flagship conferences style guideline for logos, brochures and websites including timelines as to readiness.	Conferences FT
17	Meet the IEEE benchmarks in terms of the performance of our conferences.	Conferences FT
18	Enhance EPS continuing education offerings	Education FT
19	Strengthen and expand the EPS certificate program	Education & Technology FT's
20	Develop Guidelines and Templates for Electronic Packaging University Education Programs	Education FT
21	Enhance the EPS Distinguished Lecturer Program	Education FT
22	Develop non curricula educational materials and activities for students and young professionals	All FT's, Director of Student Programs

7) Detailed Descriptions of Goals/Actions and Timelines

Goal 1: Grow EPS Membership to 3000

Goal under the purview of: Membership Functional Team

Actions to Achieve this Goal:

- Engage prospective members in our technical community through expanded social media presence to publicise the benefits of EPS. Launch new video media content to illustrate IEEE EPS and membership benefits.
- Explore ways that membership fees can be bundled with our flagship conference registrations in order to make becoming a member easier for the large number of professionals who attend EPS conferences around the world.
    - Status: Instituted in 2022 and ongoing
- Survey non-members to better understand their reasons for not becoming members of IEEE and EPS and develop region-specific advertising and outreach initiatives to address their concerns.
    - Status: Done yearly as part of post-ECTC attendee survey, expand to include other EPS conferences
- Utilize the Affiliate Membership option as a lower cost option to introduce prospective members to EPS, advertising this more broadly through communications with non-members attending EPS events (e.g. conferences).
    - Status: Instituted with flagship conference membership initiative
- Target membership growth in emerging growth regions for electronics and packaging related industries (e.g. Region 10)
- Promote EPS membership to members of EPS technical committees, including conference technical committees and EPS Technical Committees. Investigate costs associated with providing an initial membership subsidy/discount to committee members who join IEEE and EPS for the first time.
    - Status: Complete
- Analyse attendance data for EPS flagship conferences to evaluate what countries have large numbers of attendees present and cross reference with EPS membership data. In addition, identify flagship conference attendees who are IEEE members but are not EPS members and create an outreach program to encourage them to join EPS.

Metrics and Timeline

- In 2020 (or before), implement a non-member survey through all EPS flagship conferences and databases and analyse data to develop strategies to address obstacles to membership.
- In 2020, Expand cross-promotion of EPS membership with other related societies, with reciprocal cross-promotion to renewing EPS members.
    - Status: Done for a few years with related societies with marginal gains. EPS participating in IEEE-wide society discount program for members joining multiple societies.
- By 2022, implement and wider social media presence through LinkedIn and/or other relevant platforms.
- By 2021, implement a methodology to allow flagship conference (ECTC, EPTC, ESTC) registrants to include IEEE and EPS memberships in their conference registration cost. Consider the use of Affiliate Membership option for this to reduce cost to new members and overall conference/membership total.
    - Status: Complete

- In 2021, analyse attendees from 2020 flagship conferences who are IEEE members and cross reference with EPS membership list to determine IEEE members who are not members of EPS. Create targeted email campaign to reach out to these IEEE members and encourage them to join EPS.
- By 2022, launch a campaign to engage members of EPS Technical Committees and conference technical committees in IEEE and EPS membership. Determine viability of a membership subsidy program for first time members.
    - Status: Done for Technical Commitees and we have encouraged ECTC technical subcommittee members to join in communications during yearly program meetings
- In 2022, review attendance data from 2021 flagship conferences and identify countries with high attendance; develop communication strategy to reach out to attendees in these countries to drive membership and potential chapter growth.
- By 2023, increase Region 10 membership by 10% through host country expansion of EPTC conference.
    - Status: Rotation strategy of EPTC has changed as we reached the other side of the pandemic. Membership statistics at the IEEE level indicate strong growth in Region 10 for the past year +.

Goal 2: Achieve and Maintain a Membership Retention Rate of 80%

Goal under the purview of: Membership Functional Team

Actions to Achieve this Goal:

- Develop and distribute a member survey to be sent to all EPS members in order to learn more about what benefits are most important to them and what EPS can do to provide more value to members.
    - Status: Done in late 2020 with information to membership provided in early 2021
- Outline career and member benefits of being an IEEE EPS member through the creation of 1-2 testimonial videos to be produced and distributed through EPS social media, web, and conference outlets.
    - Status: 2023 focus
- Develop video testimonials of what IEEE membership means for me, with regional, age group, and different industry perspectives.
    - Status: 2023 focus
- Encourage Senior Members to become mentors to student and young professional members so that a society and technical communication path/link is established early with new members.
- Proactively identify Senior Member candidates within Technical groups and Chapters and encourage and support these candidates to pursue Senior Member applications.
    - Status: Recurring senior member encouragement in EPS newsletter, and multiple new SM candidates reached out to BoG members for application support

Metrics and Timeline

- By mid-2020, have completed EPS member survey to analyse present membership demographics and identify key areas for growth and retention of members based on region, age range, and other factors.
    - Status: Complete
- In 2020, develop a framework to support Chapters and Technical groups in identifying Senior Member candidates and proactively engaging and supporting them

in their application process. Led by the Director of Chapter Programs, create supporting documents and materials that describe this process and provide data on potential candidates within the Chapter's region or Technical group's membership.
    - Status: Established communications that were sent to members via email in 2022
- By 2021, have produced and distributed EPS member testimonial videos with viewpoints from members representing various demographic groups. These shall be made available through web and social media outlets.
    - Status: 2023 Focus
- In 2021, develop a members' survey to go out in the Aug-Sept timeframe to understand how member perceptions of EPS are changing over time. Plan to repeat member survey in 2023 during the same Aug-Sept timeframe and compare with 2021 data.
    - Status: Done in 2020, results circulated in 2021
- In 2022, initiate a campaign to contact EPS Senior Members to encourage them to participate in a mentoring program to support student and/or young professional members. The Membership Functional Team will support this initiative to connect mentors and mentees.

Goal 3: Develop New Chapters and Revitalize Existing Chapters

Goal Under the purview of: Membership Functional Team, Educational Functional Team, and the Regional Directors

Actions to Achieve this Goal:

- Establish a Regional Director position for Regions 1-6, 7, and 9, similar to those Director positions for Regions 8 and 10.
    - Status: Completed and instituted in 2020
- With support from the Educational Functional Team, utilize Distinguished Lecturers to support new and underperforming chapters with stimulating speaking engagements on current topics.
    - Status: DL engagements for remote presentations were highly used during pandemic and new DLs are being added
- Establish best practices of active/successful chapters and provide these as documents to all chapters to serve as a blueprint for developing new chapters and invigorating underperforming chapters.
    - Status: Complete
- Establish an EPS-wide chapter awards program for both Student and regular chapters to recognize exemplary performance.
- Implement Student Chapter support programs to promote new student chapters and retain existing ones, providing financial support for student chapter Executive Committee members and chapter faculty advisors.
    - Status: Ongoing
- Develop benefit program for Student Chapter advisors, providing discounted or free IEEE and EPS membership each year the advisor continues in his/her role.
    - Status: Ongoing

Metrics and Timeline

- By mid-2020, identify underperforming and at-risk chapters and implement intervention plans, including Distinguished Lecturer events, membership drives, and other events. Determine opportunities for sister-chapter relationships to be established.

- By 2021, have established Region 1-6, 7, and 9 Regional Director position, through EPS BoG initiative, with revision of bylaws, selection of candidate, and development of roles and responsibilities.
    - Status: Complete
- By 2021, implement and evaluate the Student Chapter Promotion program and assess its effectiveness in encouraging and retaining student membership and advisor engagement.
    - Status: Complete
- In 2021, have developed and implemented the Best EPS Student and Regular Chapter awards program.
    - Status: Complete
- By 2022, have developed and disseminated chapter best practices documents to all chapters to provide a framework for chapter organization, promotion, membership growth, and financial operations. This will be carried out by the Regional Directors with inputs from Directors of Chapter Programs and Student Programs.
    - Status: Complete
- By 2024, have developed and implemented guidelines for student chapter advisors and executive members for developing new student leaders early in their late undergraduate or early graduate careers in order to maintain chapter continuity over time.

Goal 4: Increase Membership in Under-Represented EPS Member Populations

Goal under the purview of: Membership Functional Team, Conference Functional Team, and EPS Conferences

Actions to Achieve this Goal:

- Analyse EPS membership statistics to identify member populations that are under-represented within the Society and determine what criteria will be used to categorize a specific member population as under-represented.
- Once under-represented member populations are defined, develop specific, targeted strategies with actionable plans to support growth of these populations.
- Engage with EPS flagship conferences to establish social events for under-represented member populations. Determine if other EPS conferences/workshops can also support similar events for their attendees.
- Develop EPS specific role model /mentor program for under-represented member populations.

Metrics and Timeline

- By 2022, complete analysis of EPS membership statistics and define at least three member populations that will be focused on for growth.
- By 2023, have established growth plan actions for target member populations, with an emphasis on using Chapters and Conferences as primary providers of events, recruitment, and communication.
- By 2024, work with EPS flagship Conferences (and other major EPS conferences/workshops) to establish events for under-represented member populations.
- By 2024, Establish and promote a list of specific mentors for minority populations in each region.

Goal 5: Continue to increase the effectiveness of Technical Committees

Goal under the purview of: Technology Functional Team

Actions to achieve this goal:

- Initiate regular transitions of Technical Committee Chairs. Ensure leadership transitions occur and new leaders are supported
- Extend scope of Substrates TC beyond ECTC Special Session and increase EM country membership
- Support rebuild of Th&Mech TC
- Develop effective collaboration between Technical Committees (ex: Photonics and Reliability on the REPP Symposium)
- Create an active and cross-functional Test TC

Metrics and timeline:

- Define a recommended term and lead leadership transitions in TCs. Ensure co-chairs are in-place to enable training and transitions.
- Work with each TC Leader to develop Technical Committee specific goals that support our strategy (1:1's). Communicate these goals to the TC Working Group in monthly meetings.

Goal 6: Continue to enhance the quality and depth of technical content to the EPS/Packaging communities

Goal under the purview of: Technology Functional Team

Actions to achieve this goal:

- Continue to increase technical content and depth of monthly EPS Newsletter articles
- Focus on disruptive technologies
- Encourage articles from beyond the TCs (examples: Supply Chain, Standards)
- Look for more opportunities at the interface between technology and (manufacturing)
- Increase frequency of new material on websites (role assignment and expectation coaching)
- Drive web admins as means to enable regulare website updates. Prompt TC Chairs to keep websites up-to-date.
- Increased use of social media

Metrics and actions:

- Each TC is posting material on a regular basis.
- Each TC provides two articles to the EPS newsletter w/in a calendar year.
- Each TC has a web admin

Goal 7: Position EPS as a preferred information source of disruptive packaging technology

Goal under the purview of: Technology Functional Team

Actions to achieve this goal:

- Link appropriate TCs to HIR chapters.
- Define and implement an EPS standards strategy
- Participate in new IEEE Initiatives (ex: Future Networks) and utilize Technical Committee expertise to add to and increase IEEE effectiveness

Metrics and actions:

- Complete review of TC-HIR potential links and formalize representation.
- Participate in HIR Roadmap committees
- Review standards opportunities that align with EPS strategy and define where EPS can participate but not repeat what others do well.

Goal 8: Optimize the value of outreach by TC's to conferences, societies, local chapters, standard activities, in and beyond EPS

Goal under the purview of: Technology Functional Team

Actions to achieve this goal:
- Continued excellent conference and society support by TCs
- Collaboration with Standards Committees on supporting Chiplets standards.
- Increase effectiveness at growing Photonics in ECTC with cross functional help from HIR, Photonics TC, and ECTC Photonics Committee
- Encourage webinars by TC members in their areas of expertise

Metrics and actions:
- Identify Conferences, Chapters, Societies and Standard group to collaborate with.
- Implement liaisons for each selected TC-Chapter/Conference/Soceity/Standard link.

Goal 9: Reduce turnaround time from paper submission to first decision to 25 days.

Goal under the purview of: Editorial Board

Actions to Achieve this Goal:
- Obtain commitment from all Associate Editors to reduced turnaround time without sacrificing the quality of peer reviews.
- Remove "Reject with Major Revisions" option in ScholarOne manuscript system
- Implement Best AE Award to encourage and recognize outstanding performance.
- Empower AE/GEs to make decisions after the first review cycle. SAEs + EIC to help facilitate.
- For papers that need significant revisions, AE/GEs should make greater use of the "Reject and Re-submit".
- Generate & follow-up monthly AE performance reports to gauge & improve performance.

Metrics and Timeline:
- Year end 2020 target turnaround time to 40 days
- Year end 2021 target turnaround time to 35 days
- Year end 2022 target turnaround time to 30 days
- Year end 2023 target turnaround time to 25 days

Goal 10: Improve Impact Factor of CPMT Journal to 3.0

Goal under the purview of: Editorial Board

Actions to Achieve this Goal:
- Reduce turnaround time as noted in Goal 9.
- Improve reviewer pool as noted in Goal 11.
- Conduct an annual competitive analysis to gauge T-CPMT performance against competing journals.

- Identify emerging or new technologies for Special Sections.
- Partner with other Societies/Councils to identify common and relevant topics for Special Sections.
- Publish in-depth critical literature review on current and future topics of interest
- Invite best papers from EPS conferences (ECTC, ITherm & their European and Asian counterparts) to submit revised papers to T-CPMT.

Metrics and Timeline:

- Year end 2020 target Impact Factor 2.00
- Year end 2021 target Impact Factor 2.25
- Year end 2022 target Impact Factor 2.50
- Year end 2023 target Impact Factor 2.75
- Year end 2024 target Impact Factor 3.00

Goal 11: Improve Reviewer pool

Goal under the purview of: Publications Board

Actions to Achieve this Goal:

- Advertise for reviewers at ECTC and other conferences. Tap into population of presenters and recent graduates to generate an active and interested reviewer data base.
- Implement reviewer liaison to target potential reviewers
- Data mine to understand reviewers' performance and use it to refine reviewer pool. Generate monthly reviewer performance reports
- Implement Reviewer Locator in ScholarOne Manuscript system
- Ask reviewers to update profiles in system to identify keywords, areas of expertise and upload CVs
- Ask current reviewers if they are interested in continuing in their role. Revise database based on responses.

Metrics and Timeline:

This is an on-going activity. Plan is to work with T-CPMT Editorial Team and IEEE to implement a continuous improvement plan to refine reviewer pool using review quality and timeliness as refinement criteria

Goal 12: Enhance geographic and gender diversity of Associate Editors

Goal under the purview of: Editorial Board

Actions to Achieve this Goal:

- Invite leaders in Region 8 and 10 to become Guest Editors with the possibility to become Associate Editors
- Enlist female leaders to become Guest Editors with the possibility to become Associate Editors
- Discuss potential candidates during Editorial Board meetings

Metrics and Timeline:

- Ensure Associate Editors have an opportunity to move to the SAE level based on performance.
- Double the geographic and gender diversity from end of 2019 state within 5 years (2024)

Goal 13: Support the IEEE's strategy to expand its presence in the Open Access market

Goal under the review of: the Editorial Board

Actions to Achieve this Goal:

- Offer fully gold Open Access option within IEEE Access. Create Electronics Packaging Society Section.
- Invite selected papers to be Open in T-CPMT twice a year and waive APC fees.
- Track submissions to EPS section within IEEE Access June 2020

Metrics and Timeline:

- Continue marketing efforts in e-newsletter, on website, social media platforms and conferences to advertise section within Access
- Double submissions to EPS section within IEEE Access by June 2022

Goal 14: Grow attendance and exhibitor numbers at ESTC by 50%.

Goal under the purview of: Conference Functional Team, Region 8 Director

Actions to Achieve this Goal:

- Increase sponsorship and exhibitors by standardizing the method of attracting them to the conferences.
- Use EPS' Global Flagship Electronic Components and Technology Conference (ECTC) methodology as the gold standard, which includes having non-rotating organizational committee members who manage the sponsor and exhibitor relationship year-over-year.
- Sponsorship: Compare services and share best practices between conferences.
- ESTC should have a website for sponsors and exhibitors with up to date information including fees and services.
- ESTC should have logos of exhibitors and sponsors posted on the conference website. Rotate best papers from flagship conferences for exposure in different regions.
- EPS rep must present status at Conference Functional Team monthly meeting and actively seek to fulfil requests for keynote, panel, and invited speakers, and PDC instructors. Add EPS President and EPS Rep to ESTC Steering Committees.
- ECTC and ESTC to share IEEE email blast services.

Metrics and timeline

- ESTC to continue to create brochures for sponsorship 6-9 months prior to conference.
- ESTC should have a webpage for sponsors and exhibitors with up to date information including fees and services 6-9 months prior to conference.
- Rotate best papers from flagship conferences for exposure in different regions: Status: Motion approved at BoG November 2019 meeting.
- Appoint an EPS representative to the organizing committee of each conference by end of 2019. (Done)
- Grow conference attendance at EPTC and ESTC by 50% during 2024 conference (use 2018 as baseline).

Goal 15: To apply conference award best practices given at our Global (ECTC) and Regional Flagship conferences (EPTC, ESTC) that include but are not limited to the type of

awards, procedures on how these awards are selected, and the dollar amount of the awards. **(Complete – Guidelines included in EPS Conference Handbook)**

Goal under the purview of: Conference Functional team and the Director of Awards.

Actions to Achieve this Goal:

- Summarize and review the awards given at ESTC, ECTC, and EPTC including how the awards are selected.
- How to analyse data (e.g. categorize paper as Academic vs Industry if there are authors from both).
- Based on the results of the summary and analysis, propose a standard set of best practices.
- Get buy-in from EPS Flagship Conference Organizing Committees.
- Roll-out new awards and award selection processes.

Metrics and timeline

- Summarize and review the awards given at ESTC, ECTC, and EPTC: Sept 2019. (Done)
- How to analyse data (ego categorize paper as Academic vs Industry of there are authors from both) completed. October 2019
- Analyse how the awardees are currently selected. November 2019.
- From the analysis, propose best practices that should be used across all the EPS Flagship Conferences. January 2020
- Get buy-in from EPS Flagship Conference Organizing Committees: March 2020.
- Roll-out new awards and award selection processes: 2020 conferences.

Goal 16: EPS to provide Flagship conferences style guideline for logos, brochures and websites including timelines as to readiness.
IEEE Guidelines on Logo Use: IEEE Policy 6.3.2 and IEEE Policy 10.1.18

Goal under the purview of: Conference Functional team.

Actions to Achieve this Goal:

- Formalize style guidelines with help of Conference FT team.

Metrics and timeline

- Complete at end of 2020 and roll-out to conferences in 2021

Goal 17: Meet the IEEE benchmarks in terms of the performance of our conferences.

Goal under the purview of: Conference Functional team.

Metrics and Timeline

- Metrics: Time to close (6 Months); Net Return (20%); Average time to publish (30 days).

Goal 18: Enhance EPS continuing education offerings

Goal under the purview of: Education Functional Team

Actions to Achieve this Goal:

- Expand EPS webinar catalog and the frequency of new offerings. In particular, develop a robust set of webinar offerings including an electronics packaging education series, a Heterogeneous Integration Roadmap (HIR) series, and a career development series; as well as the traditional mix of relevant and timely technical topics, including webinars that appeal and can be shared across multiple IEEE societies.
- Make EPS webinars available to non-members and the general public through the EPS Resource Center and IEEE Learning Network (ILN).
- Expand the availability of CEU certificates for attending PDCs at EPS conferences. In particular, offer CEU certificates to PDC attendees at all EPS flagship conferences, and gradually expand the CEU certificate program to include the PDC courses offered at all other EPS technically-sponsored conferences.
- Develop a resource guide for EPS-sponsored conference organizers that includes guidelines for organizing PDC courses and implementing CEU certificates.
- Develop system for attendees at DL presentations to receive CEU credits that can count towards the EPS certificate program.

Metrics and Timeline

- In 2020, initiate HIR webinar series including an updated roadmap overview webinar, and selected roadmap chapter presentations from the Technical Working Groups (TWGs).
    - Status: Complete
- In 2021-2024, update HIR webinars as appropriate.
- In 2022-2023, develop plan for implementing an electronics packaging education webinar series.
- In 2023-2024, release electronics packaging education webinars at the rate of 2 per year.
- In 2020-2024, implement initial career development webinars at the rate if 1-2 per year.
- In 2020, develop methodology and pricing structure for EPS webinars made available to non-members and the general public through the EPS Resource Center.
    - Status: Complete
- In 2021-2024, review webinar sales through EPS Resource Center and modify approach if needed.
- In 2020-2024, offer CEU certificates to PDC attendees at ECTC, ESTC, and EPTC (EPS flagship conferences). Work with ESTC and EPTC organizers to initiate and standardize this process at their conferences. As a part of that effort, develop a draft resource guide for EPS conference organizers that includes guidelines for organizing PDC courses and implementing CEU certificates
    - Status: Complete
- In 2022, offer CEU certificates to PDC attendees at EuroSimE.
    - Status: Complete
- In 2022, update resource guide for EPS conference organizers to include information on Professional Development Courses.
- In 2023-2024, with the conference organizers using the resource guide, add availability of PDC CEU certificates to additional EPS-sponsored conferences.
- In 2022, develop online form for attendees at DL presentations to report their attendance, and request associated CEU credits that can count towards the EPS certificate program.

Goal 19: Strengthen and expand the EPS certificate program

Goal under the purview of: Education Functional Team, Technology Functional Team

Actions to Achieve this Goal:

- Better publicize the availability of our EPS continuing education opportunities, and improve the attractiveness of being recognized through the EPS certificate program. In addition, work to develop certificates that are universally recognized in other countries and societies.
- Develop and implement a second level EPS certificate to recognize advanced career and professional development achievements including technical accomplishments, professional society activities, leadership, coaching, mentoring, volunteering, etc.
- Work with EPS Technical Committees to develop topical certificates recognizing achievements in specific EPS technical areas.

Metrics and Timeline

- In 2020, develop and implement plan to publicize EPS continuing education opportunities.
    - Status: Complete
- In 2020, develop guidelines for a second level EPS certificate to recognize advanced career and professional development achievements. Obtain BoG approval for proposed certificate.
    - Status: Complete
- In 2021, implement second level EPS certificate.
    - Status: Complete
- In 2022-2024, evaluate success of EPS certificate program and modify as necessary.
- In 2020-2024, meet with active EPS technical committees to gauge interest in developing topical certificates recognizing achievements in specific EPS technical areas. The goal will be to develop at least one topical certificate in coordination with appropriate Technical Committee.

Goal 20: Develop Guidelines and Templates for Electronic Packaging University Education Programs

Goal under the purview of: Education Functional Team

Actions to Achieve this Goal:

- Develop recommended curricula and course syllabi for electronics packaging educational programs including undergraduate/graduate survey and special topic courses, professional master's degree programs, and research oriented Ph.D. programs.
- Establish and lead a new committee of educators and other interested parties to coordinate this effort.
- Coordinate education workshops at EPS flagship conferences to seek broad input from the educators and the electronics packaging technical community.

Metrics and Timeline

- In 2022-2023, develop database of existing electronics packaging oriented faculty and existing electronics packaging courses and education programs.
- In 2022-2024, hold "Electronics Packaging Education" at ECTC, ESTC, and EPTC to recruit participation from educators and industry, as well as to generate interest.
- In 2023-2024, develop recommended syllabus contents for undergraduate/graduate survey and special topic courses
- In 2023-2024, develop recommended curricula and course syllabi for professional master's degree programs related to electronic packaging.

Goal 21: Enhance the EPS Distinguished Lecturer Program

Goal under the purview of: Education Functional Team

Actions to Achieve this Goal:

- Develop standard approaches for robust recruitment and retention of DLs including application, approval, renewal, and recognition processes.
- Implement DL annual reporting.
- Develop improved system to advertise DL availability and technical expertise areas to Chapters, Student Branch Chapters, conferences, etc.
- Develop system for attendees at DL presentations to receive credit towards the EPS certificate program (see also Goal #1).

Metrics and Timeline

- In 2020, develop standard approaches for robust recruitment and retention of DLs including application, approval, renewal, and recognition processes. Modify DL guidelines document and seek BoG approval where necessary.
- In 2022, initiate DL annual reporting.
- In 2020-2024, develop and implement annual procedure to advertise DL availability and technical expertise areas to Chapters, Student Branch Chapters, conferences
- In 2022, develop online form for attendees at DL presentations to report their attendance, and request associated CEU credits that can count towards the EPS certificate program.

Goal 22: Develop non curricula educational materials and activities for students and young professionals

Goal under the purview of: Education Functional Team, Director of Student Programs, Membership Functional Team, Technology Functional Team, Conference Functional Team

Actions to Achieve this Goal:

- Develop online resources (e.g. papers, presentations, etc.) on various electronics packaging topics to serve as resources to students and young professionals
- Develop a compendium of weblinks to other online public domain electronics packaging educational resources.
- Improve and expand EPS-sponsored annual competition programs for individuals and teams related to electronics packaging that engage and excite students and young professionals. The annual competitions would culminate in featured events held as a part of EPS conferences.

Metrics and Timeline

- In 2022, update existing electronics packaging overview presentation available on EPS website.
- In 2023, develop initial online compendium of weblinks to other online public domain electronics packaging educational resources.
- In 2023-2024, develop plan to expand online educational resources available for students and young professionals.
- In 2020, generate database of individual and team-based student competitions that are directly sponsored by EPS or held at EPS technically-sponsored conferences. Advertise the programs actively.
- In 2020, offer second annual Additively Manufactured Heat Sink competition for university student teams. Hold final round of competition at ITherm 2020.

- In 2021, initiate first year of EPS-sponsored Overclocking competition for university student teams.
- In 2022-2024, continue to sponsor team competitions for students and young professionals, with at least two competitions per year culminating at one or more of the EPS flagship conferences.

8) Conclusion

Electronics Packaging Society goals and their corresponding Operations Plan for their achievement have been presented above. The plan is feasible because the leadership of the Society and various Committees oversee each goal in a coordinated effort to improve the service that the society provides its members and community worldwide. The financial resources of the Society allow the completion of this plan.

Appendix

Technical Committees	Activities/Initiatives	Councils
- Materials & processes - High Density Substrates/Boards - Electrical Design, Modelling & Simulation - Thermal & Mechanical - Emerging Technology - Nanotechnology - Power & Energy - RF & TZ Technologies - Green Electronics - Photonics - 3D/TSV - Reliability	- Heterogeneous Integration Roadmap - Young Professionals - Women in Engineering - IoT - IEEE Quantum - Rebooting Computing - 5G - Hardware Technology Roadmaps	- Sensors - RFID - Nanotechnology - EDA - Superconductivity

The society is also served by 40 chapters worldwide supporting our technical meetings, workshops and conferences.

Region 1-7	Region 8	Region 10
1) Binghamton 2) Central Indiana 3) Dallas 4) Eastern NC 5) Mid Hudson 6) Montreal 7) Orange County 8) Oregon 9) Ottawa 10) Northern VA/Washington 11) Philadelphia 12) Phoenix 13) Pittsburgh 14) San-Diego 15) Santa Clara Valley – Photovoltaics 16) Santa Clara Valley 17) Toronto 18) Vancouver	19) Benelux 20) Bulgaria 21) France 22) Germany 23) Hungary/Romania 24) Israel 25) Nordic 26) Poland 27) Russia 28) Switzerland 29) Ukraine -Kiev 30) Ukraine West 31) UK & Ireland	32) Bangalore 33) Beijing 34) Hong Kong 35) Korea Council 36) Malaysia 37) Shanghai 38) Singapore 39) Taipei 40) Tokyo

Society also 28 student branch chapters, 2 of these being in region 9 (Brazil).

Region 1-7	Region 8	Region 9	Region 10
Florida International University Georgia Institute of Technology	Addis Ababa University Budapest University of Technology & Economics	Universidade Estadual Paulista Universidade Federal do ABC	Central South University Fudan University Harbin Institute of Technology-Main Campus

San Jose State State University of NY at Binghamton UCLA (ED) University of Florida University of Maryland - College Park University of Waterloo	Enugu State University of Science & Technology Gh Asachi Iasi Technical University Institute of Management & Technology Enugu Politechnica Univ of Bucharest Politehnica University of Timisoara Technical University of Cluj Napoca Trident Academy of Technology University Lucian Blaga Sibiu University of Ruse		Seoul National University of Science and Technology Singapore University of Technology & Design Tsinghua University Wuhan University

Society also sponsors 14 IEEE publications with other societies.