Interconnects for 2D and 3D Architectures

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Merged the Interconnects Chapter w/ the 2D-3D Chapter

Chair: Ravi Mahajan, Fellow, Intel Corporation

Ravi is responsible for multi-chip package pathfinding programs for the latest Intel process technologies. He has led efforts to define package architecture, technologies and assembly processes for 90nm, 65nm, 45nm, 32nm, 22nm and 7nm silicon. He holds 40+ patents, including the original patent for a silicon bridge which is the foundation for Intel's Embedded Multi-Die Interconnect Bridge technology. He is currently VP of Publications & Managing Editor-in-Chief of the IEEE Transactions of the CPMT. Additionally he has been long associated with ASME's InterPACK conference and was Conference Co-Chair of the 2017 Conference. Ravi is a Fellow of ASME and IEEE. He was named an Intel Fellow in 2017.

Co- Chair: Raja Swaminathan, Package Architect

Raja is a package architect whose expertise is on delivering integrated HVM friendly package architectures with optimized electrical, mechanical, thermal solutions. He is an IEEE, ITRS and iNEMI roadmap author on packaging and design. He has also served on IEEE micro-electronics and magnetics technical committees. He has 28 patents and 26 peer-reviewed publications. He holds a Ph.D. in Materials Science and Engineering from Carnegie Mellon University.

Interconnect Chapter Lead

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Prof. Subramanian S. Iyer is the Distinguished Chancellor's Professor & Charles P. Reames Endowed Chair in UCLA's Electrical and Computer Engineering Department. His research and teaching interests include System Scaling Technology, Advanced Packaging and 3D integration, technologies and techniques for the memory subsystem integration and neuromorphic computing.

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The Package as a Heterogeneous Integration Platform

- Challenges for On-Package Integration
  - Deliver power-efficient, high bandwidth on-package IO links that support standardized communication protocol(s)
  - Enable a diversity of off-package IO protocols
  - Deliver noise isolation for single ended and differential signals
  - Manage increasing cooling demands
  - Support complex power delivery architectures
  - Meet diverse application functionality ranging from high performance servers to flexible, wearable electronics
  - Meet a broad spectrum of reliability requirements for different market segments and applications
  - Provide cost effective, high precision quick turn assembly

TWG Objectives

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- Define and proliferate a new standardized nomenclature for package architectures covering and clearly demarcating, both 2D and 3D constructions.
- Define and proliferate key metrics driving the evolution of the physical interconnects in these architectures. This chapter lists their current values and projections for the next generations
- The chapter is organized into 4 primary areas:
  - Converged Nomenclature Framework for 2D and 3D Architectures
  - Key Metrics:
    - Design Attributes
    - Electrical Attributes including Signaling and Power Delivery
  - Difficult Challenges
  - Discussion

Converged Nomenclature Framework for 2D & 3D Architectures

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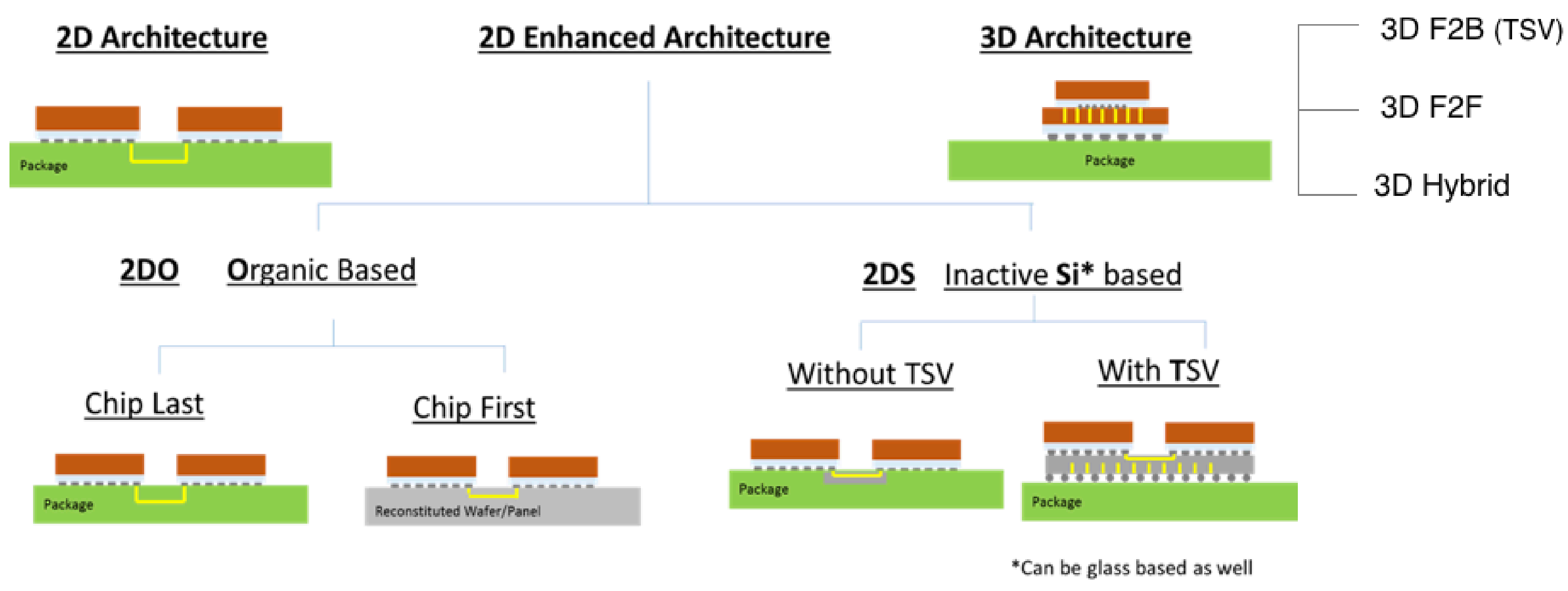

- A 2D architecture is defined as an architecture where two or more active silicon devices are placed side-by-side on a package and are interconnected on the package. If the interconnect is “enhanced” i.e. has higher interconnect density than mainstream organic packages, and accomplished using an organic medium, the architecture is further sub-categorized as a 2DO (2D Organic) architecture and similarly, if the enhanced architecture uses an inorganic medium (e.g. a silicon/glass/ceramic interposer or bridge) the architecture is further sub-categorized as a 2DS architecture.
- A 3D architecture is defined as an architecture where two or more active silicon devices are stacked and interconnected **without** the agency of the package

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Interconnect Nomenclature

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- **Die-Die Interconnects:** Interconnects between stacked die that enable vertical interconnects between multiple die in a 3-D stack *Covered in this chapter*
- **On-package Die-Die Interconnects** i.e. 2D and Enhanced 2D Interconnects: Interconnects between die within the package that enable lateral connections *Covered in this chapter*
- **Die-to-Package Interconnects:** Interconnects between the die and the package (Figure 2), typically known as the first level interconnect (FLI) *Covered in this chapter*
- **Within Package Interconnects:** Interconnects within the package that enable lateral connections *Covered in the Substrate Chapter (Cross-calibration in Progress)*
- **Package to Board Interconnects:** Interconnects between the package and the next level, which is typically the motherboard, referred to as the second level interconnect (SLI) *Covered in this chapter*
- **Package on Package Interconnects** *Covered in this chapter*

Interconnect Design Attributes

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- Peripheral Interconnects for Solder Based 2D and enhanced 2D Architectures

Generations		1	2	3	4	5
Raw Bandwidth Density (GBps/mm)		125	250	500	1000	2000
Package Technology	Minimum Bump Pitch (µm)	55	50	40	35	30
	IO/mm	500	667	1000	1500	2000
	IO/mm^2	331	400	625	816	1111
Signaling Speed (Gbps)		2	3	4	5.33	8

- No universal understanding of the required gap between generations. WG judgement is that it will be a minimum of 2 years and from a planning perspective we recommend a maximum of 3 years to ensure that the interconnect roadmap is competitive
- Starting value of 125GBps is estimated raw bandwidth possible in an AIB style implementation
- Representative example showing how the BW goals are reached. These speeds are not unique.

- Peripheral Interconnects for 2D and enhanced 2D Architectures with Aggressive pitch Scaling

Generations		1	2	3	4	5
Raw Bandwidth Density (GBps/mm)		125	250	500	1000	2000
Package Technology	Minimum Bump Pitch (µm)	55	40	30	20	10
	IO/mm	500	667	1000	1500	2000
	IO/mm^2	331	625	1111	2500	10000
Signaling Speed (Gbps)		2	3	4	5.33	8

- Starting value of 55µm is based on the most common current implementation i.e. HBM

Interconnect Design Attributes

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- Area Interconnects for 3D Architectures

Generations		1	2	3	4	5
Raw Bandwidth Density (Gbps/mm^2)		125	250	500	1000	2000
Package Technology	Minimum Bump Pitch (µm)	40	30	20	15	10
	IO/mm^2	625	1111	2500	4444	10000
Signaling Speed (Gbps)		1.6	1.8	1.6	1.8	1.6

- Starting value of 40µm bump pitch based on known implementations in HBM and WIO2 .

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Package to Board Interconnects

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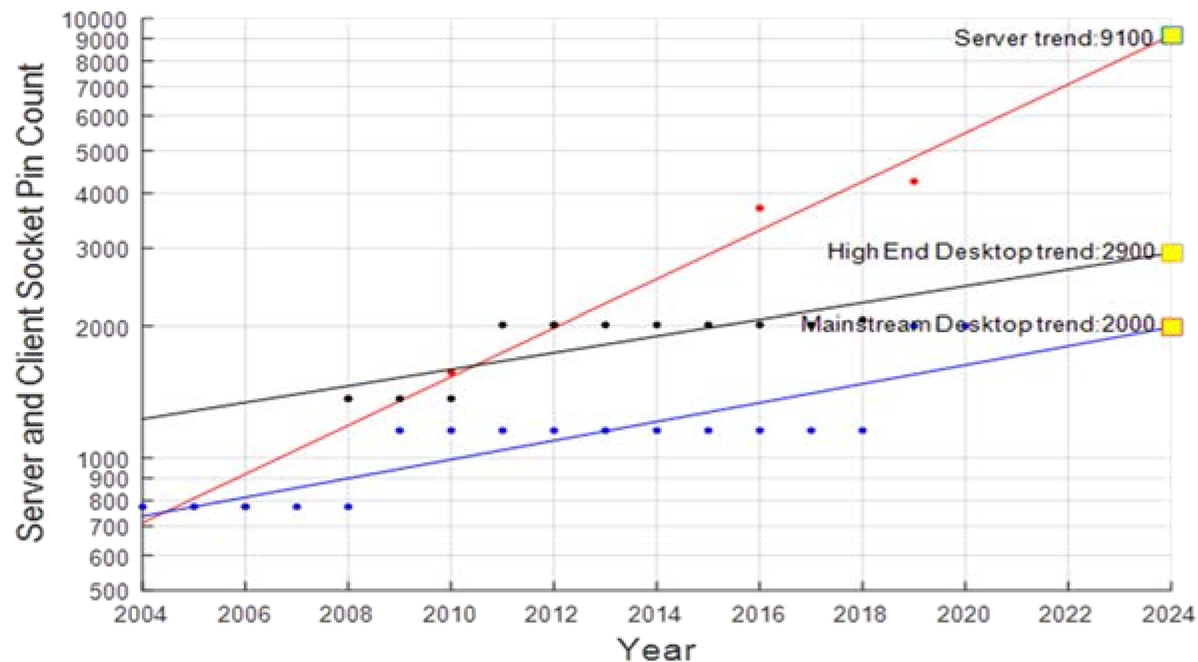
- Either socketed or BGA.
  - The 2015 ITRS Projections for Sockets are reasonable for the cost performance segment
  - For the high performance segments, the socket pin count projections look reasonable till ~2021 but seem to be under projecting significantly after. Updated projections included
  - 2015 ITRS projections for BGA pitch continue to be valid.



	2019	2020	2021	2022	2025	2028	2031	2034
Cost performance	3200	3300	3400	3500	3800	4100	4400	4700
High performance	5125	5694	6302	6946	9105	11601	14434	17604

Table 2b: Updated projections for the Cost-Performance and High Performance segments

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POP Interconnects

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POP Architectures	VI Pitch ** (mm)	Maximum Bottom Package Height (mm)
Bare Die PoP	0.5	0.75
Bare Die PoP with 2-Step solder resist (SR) + solder on pad (SOP)	0.4	0.75
TMV PoP	0.4	0.78
Exposed Die TMV PoP	0.35 → 0.27	0.69
Interposer PoP	0.27 → 0.20	0.67
FOWLP PoP	0.30 → 0.20	0.50 → 0.30

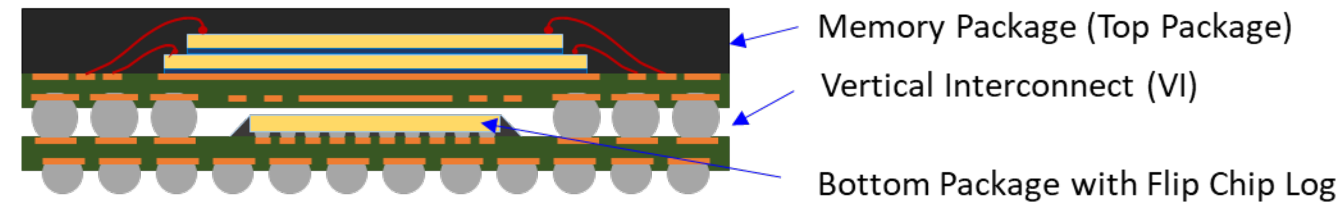

Table 3: State of the Art Pitches and Package Heights and their projected targets for POP Architectures

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The Chapter also covers…..

- Signaling Attributes
- Power Delivery Attributes

Next Revision of the Chapter will …..

- Enhance the POP Interconnect Roadmap i.e. determine if it is possible to develop one …….

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Summary

- Merged the 2D/3D chapter w/ the Interconnects Chapter. Chapter in review (1 complete, one in progress)
- Proposed a new nomenclature for 2D/ 2D-Enhanced and 3D packaging architectures – Feedback to date has not identified any gaps in the nomenclature
- Key metrics to describe 2D and 3D packaging architectures defined and roadmap described