HETEROGENEOUS INTEGRATION ROADMAP

Heterogeneous Integration Roadmap for Aerospace and Defense (HIR-AD)

Aerospace-Defense TWG Co-Chairs:
Tim Lee (Boeing)
Jeff Demmin (Booz Allen Hamilton)

05/28/2019

IEEE Region 6 Director-Elect
IEEE FNI Co-Chair,
IEEE HIR, A-D & AMS TWG Co-Chair
Past President, IEEE MTT-S

Timothy Lee, currently a Boeing Technical Fellow, is responsible for the development of RF and digital electronics for advanced communications networks and sensor systems. In the IEEE, Tim is promoting the use of technology to benefit humanity.

Mission Statement for HIR – Aerospace – Defense (A-D)

- The mission of **Heterogeneous Integration Roadmap for Aerospace and Defense** is to provide guidance and recommend solutions to the profession, industry, academia and government to identify key technical challenges with sufficient lead time that they do not become roadblocks preventing the continued progress in **Aerospace and Defense** electronics.
- There is the need to address heterogeneous integration technologies for new capabilities for embedded high-speed computing, cyber, sensors, C4ISR and RF/analog for unique sets of requirements, production volumes and lifecycle timelines.
- That progress is essential to the future growth of the industry and the realization of the promise of **continued impact on aerospace, defense and security applications**.
- The approach is to identify the requirements for heterogeneous integration in the **A-D** electronics industry with 5-, 10- and 15-year horizons, determine the difficult challenges that must be overcome to meet these requirements and, where possible, identify potential solutions and **synergies between the greater commercial sectors and the smaller A-D community.**

Heterogeneous Integration Roadmap for Aerospace and Defense (HIR-AD) Chapter

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5/22/2019

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Cross Chapter Links Needed

- HPC and Data Center
- 3D & Interconnect
- Integrated Photonics
- SiP and Module
- Single Chip and Multi-Chip Integration
- Co-Design
- Emerging Devices
- Security
- Supply Chain

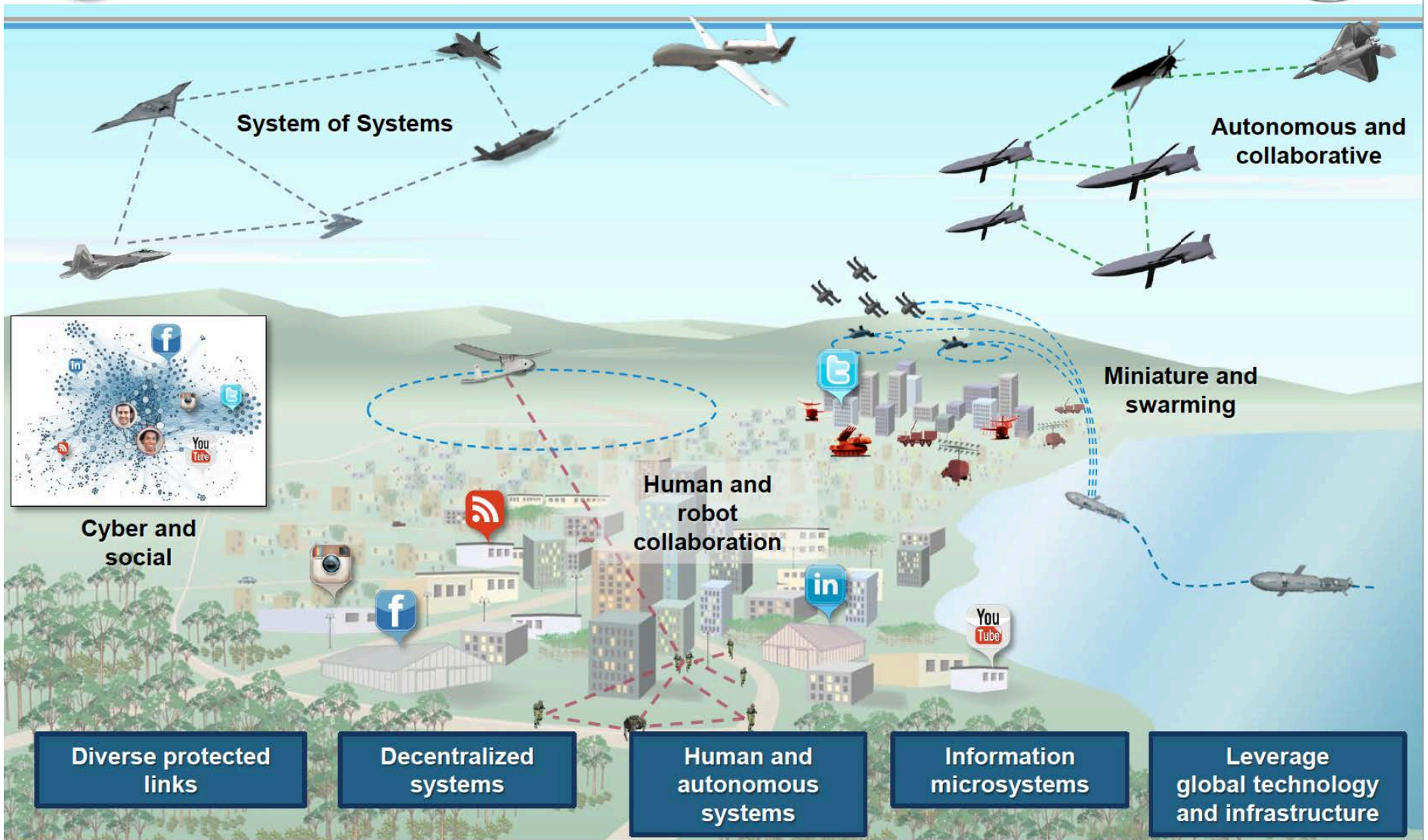
Aerospace and Defense Sector

- DoD Primes: Lockheed Martin, Northrop Grumman, Raytheon, BAE Systems, General Dynamics, and Boeing
- DoD's subsystem suppliers such as General Electric, Rockwell Collins, and Rolls-Royce provide vital subsystems including propulsion, command and control, electronic warfare, and structural subsystems to DoD's primes.
- A-D component suppliers provide component parts including energetic and structural materials, microelectronics, cables, and connectors for prime and major subsystem providers. The HIR A-D TWG focuses on microelectronics
- Pure Play suppliers

The A&D sector has been at the forefront of digital innovations, leading the way for other industries in the adoption of technologies

http://www.businessdefense.gov/Portals/51/Documents/Resources/2016%20AIC%20RTC%2006-27-17%20-%20Public%20Release.pdf?ver=2017-06-30-144825-160

Future Warfighting Systems



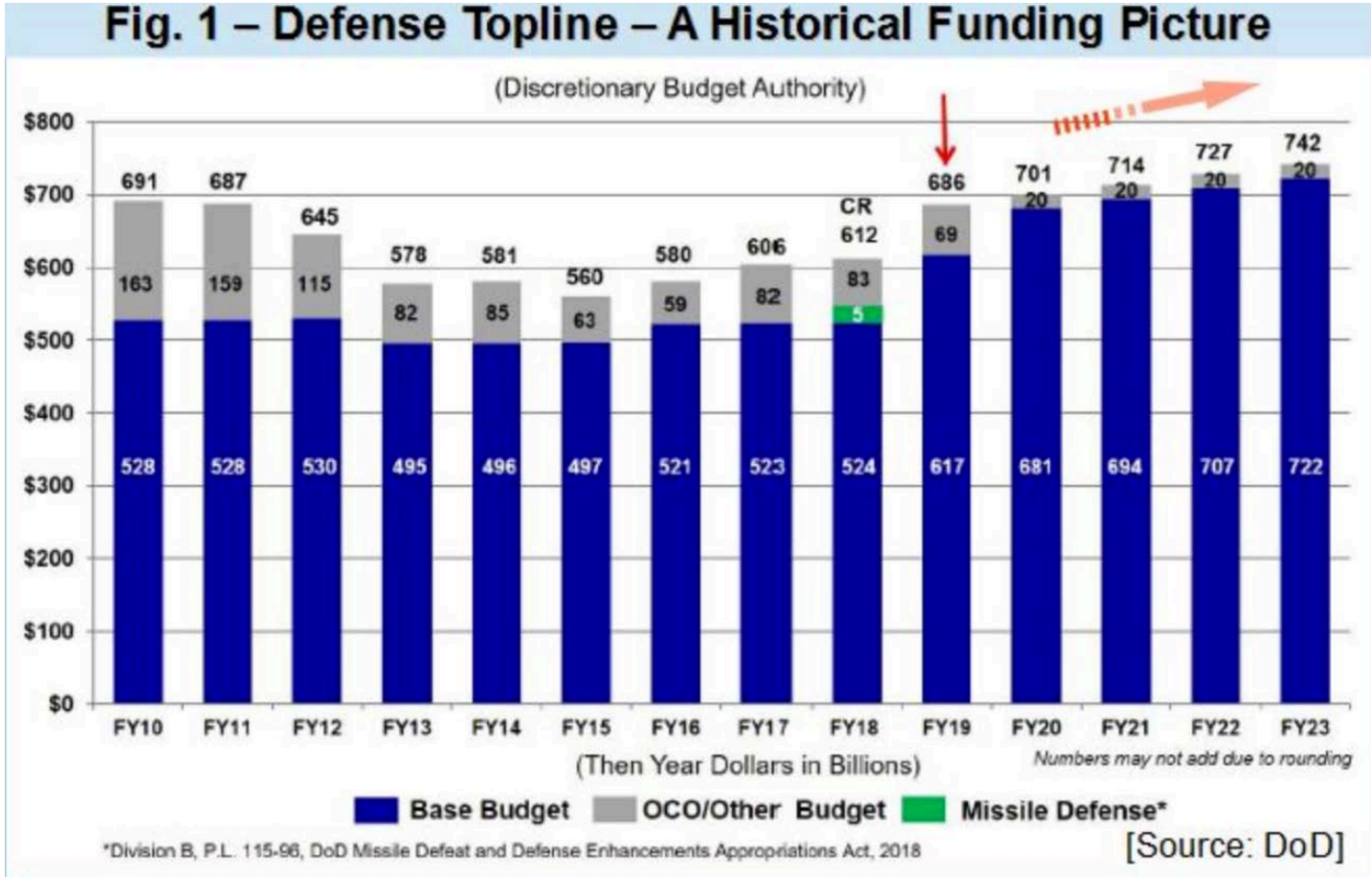
HETEROGENEOUS INTEGRATION ROADMAP

National Defense Strategy (2018)

- National Defense Strategy: “Platform electronics and software must be designed for routine replacement instead of static configurations that last more than a decade … **Deliver performance at the speed of relevance**
- **New commercial technology** will change society and, ultimately, the character of war. The fact that many technological developments will come from the commercial sector means that state competitors and non-state actors will also have access to them, a fact that risks eroding the conventional overmatch to which our Nation has grown accustomed.

https://dod.defense.gov/Portals/1/Documents/pubs/2018-National-Defense-Strategy-Summary.pdf

DoD Funding Historical Perspective



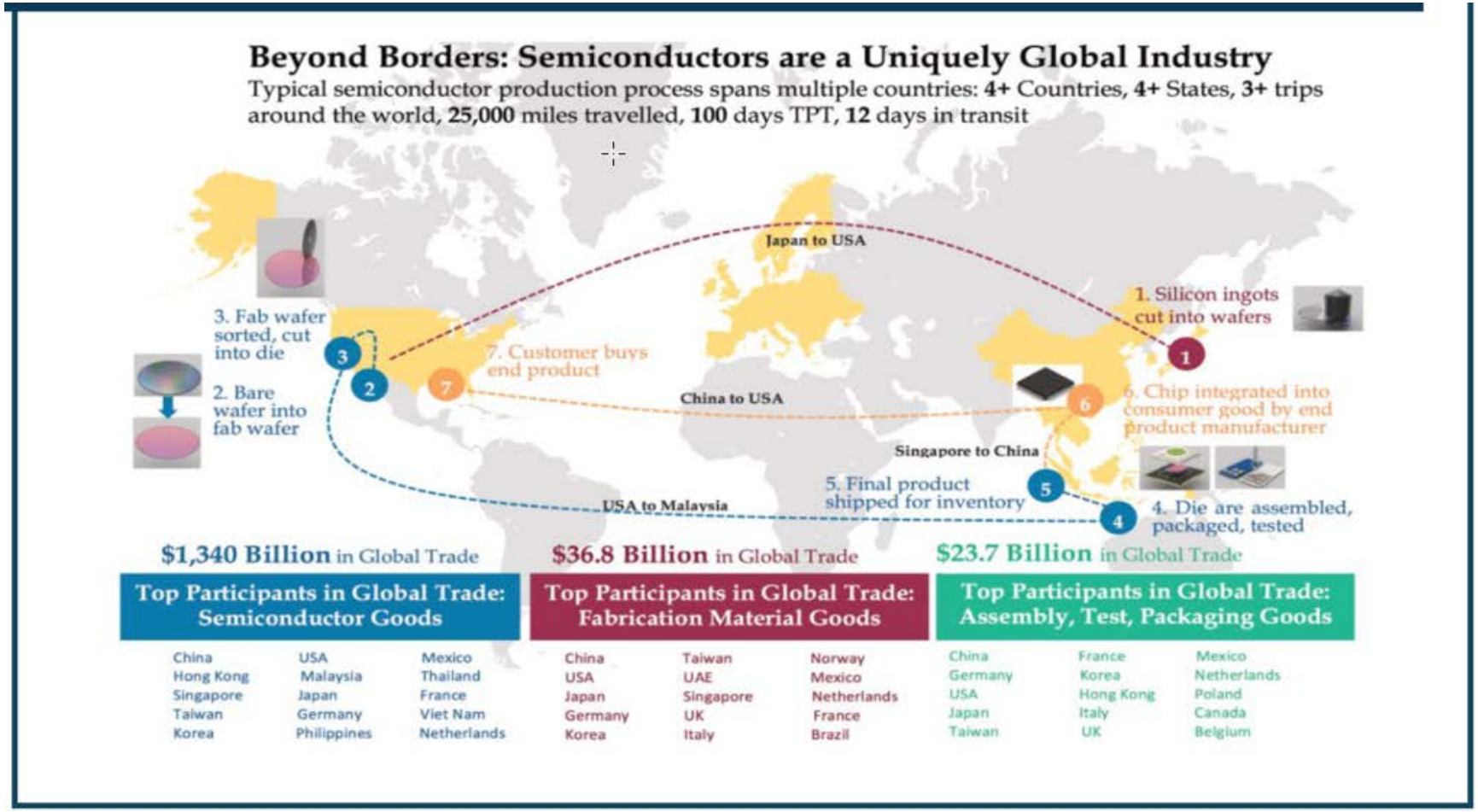
https://www.semiwiki.com/forum/content/7368-meeting-challenges-national-defense-strategy.html

What are the Future Directions & Challenges of Aerospace and Defense Electronics Systems

The Aerospace / Defense Systems market segment is an unique sector

- High Performance – Access to leading nodes and advanced packaging technologies
- High Reliability – harsh environments, human safety
- Long Product Lifecycles – parts obsolescence & upgradability
- Low Volumes – high product mix, affordability
- Need domestic supply chain
- How can heterogeneous integration help to achieve system performance objectives?

IC Manufacturing in a Globalized Independent Supply Chain



http://www.businessdefense.gov/Portals/51/Documents/Resources/2016%20AIC%20RTC%2006-27-17%20-%20Public%20Release.pdf?ver=2017-06-30-144825-160

Changing Foundry Landscape

- Foundries concentrated in Asia
- Chinese players growing
- Increasingly consolidated among leaders

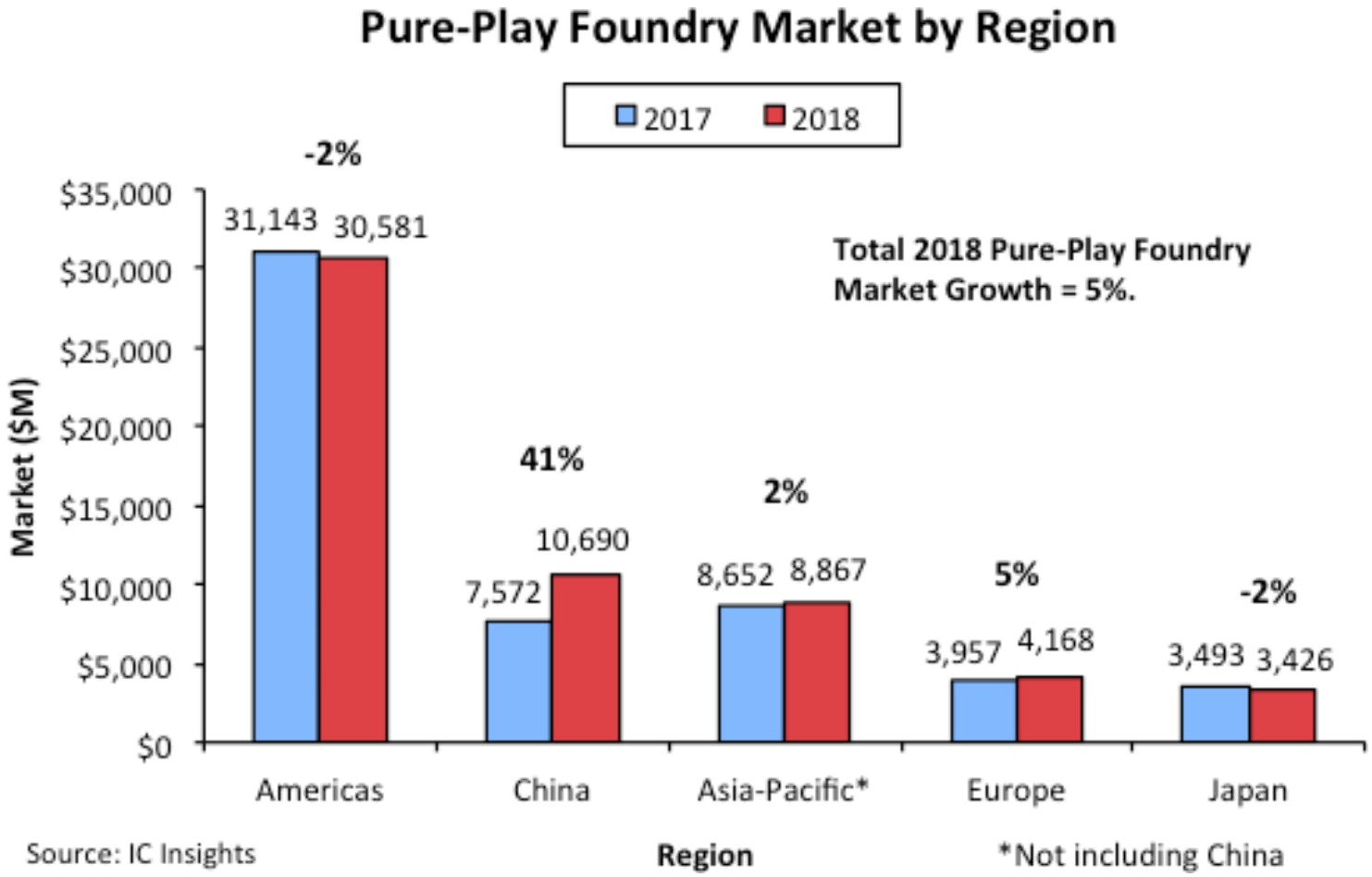
Major 2017 Foundries (Pure-Play and IDM)

2017 Rank	2016 Rank	Company	Foundry Type	Location	2015 Sales ($M)	2016 Sales ($M)	2016/2015 Change (%)	2017 Sales ($M)	2017/2016 Change (%)
1	1	TSMC	Pure-Play	Taiwan	26,574	29,488	11%	32,163	9%
2	2	GlobalFoundries	Pure-Play	U.S.	5,019	5,495	9%	6,060	10%
3	3	UMC	Pure-Play	Taiwan	4,464	4,582	3%	4,898	7%
4	4	Samsung	IDM	South Korea	2,670	4,410	65%	4,600	4%
5	5	SMIC	Pure-Play	China	2,236	2,914	30%	3,101	6%
6	6	Powerchip	Pure-Play	Taiwan	1,268	1,275	1%	1,498	17%
7	8	Huahong Group*	Pure-Play	China	971	1,184	22%	1,395	18%
8	7	TowerJazz	Pure-Play	Israel	961	1,250	30%	1,388	11%
—	—	Top 8 Total	—	—	44,163	50,598	15%	55,103	9%
—	—	Top 8 Share	—	—	87%	88%	—	88%	—
—	—	Other Foundry	—	—	6,597	7,112	8%	7,207	1%
—	—	Total Foundry	—	—	50,760	57,710	14%	62,310	8%

*Includes Huahong Grace and Shanghai Huali.

Source: IC Insights, company reports

- Nearly all foundry growth in 2018 driven by customers in China

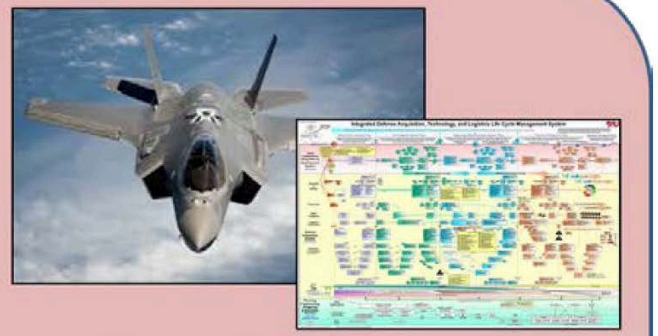


Differences between commercial Products and DoD Business Models

Source: iFixit

- Product last ~2 years (until new one is out) – Revenue Based
- Systems are complex, but differing scale and complexity from DoD Systems
- Requires assured access to components for 2-3 years.

Commercial



- Product Lifecycles are Decades
- Systems are much more complex, and therefore risk managed
- Consequences are Different
- Requires Assured Access to components for Decades
- Capabilities that are not needed Commercially (RadHard)

Military

Timelines and Complexities Are very different for DoD Modern Semiconductor Processes

NDIA: Trusted Microelectronics Joint Working Group: Future Needs & System Impact of Microelectronics Technologies, http://www.ndia.org/divisions/working-groups/tmejwg/final-team-reports

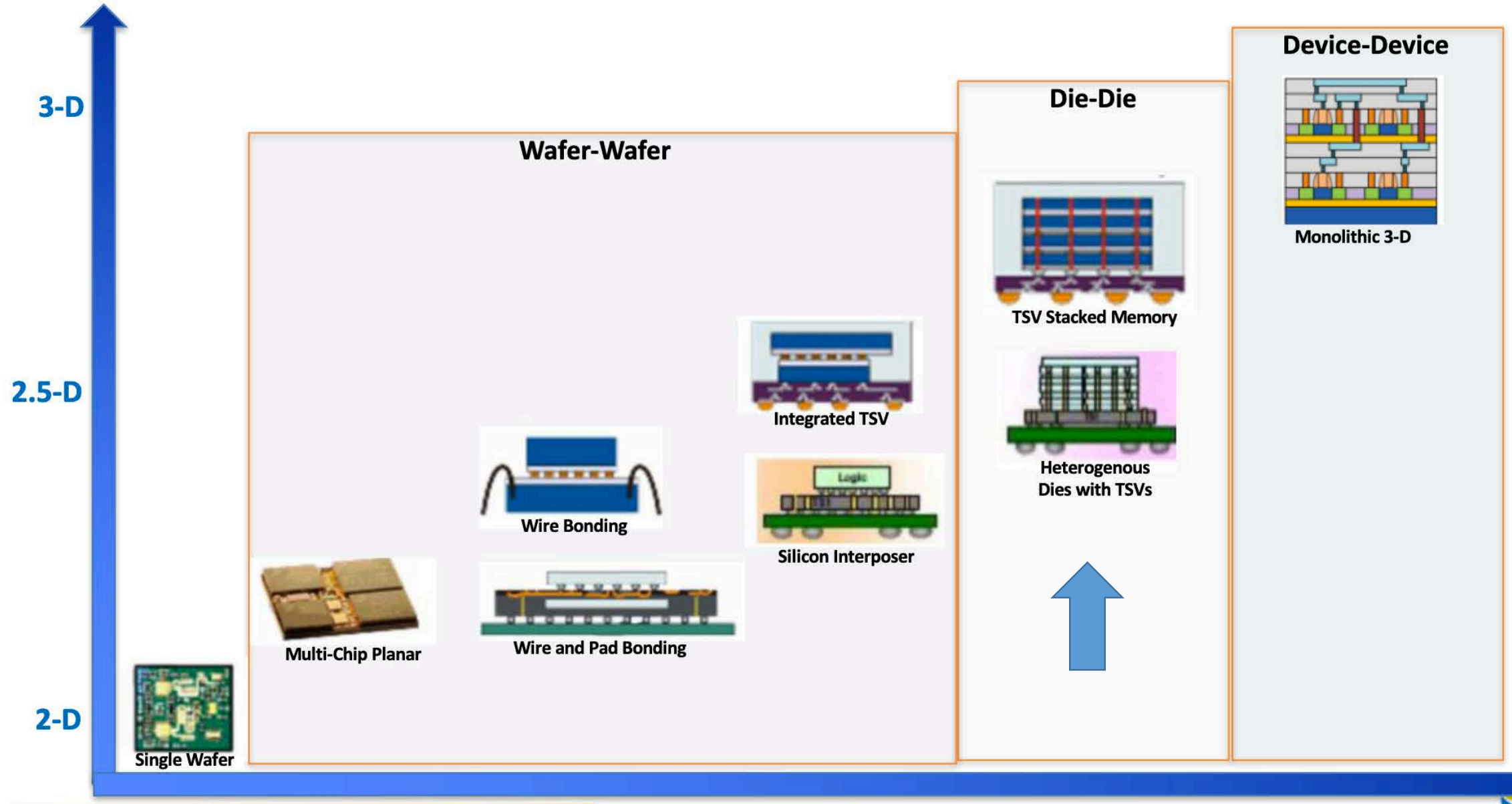
Aerospace and Defense Drivers

- What are system drivers?
  - NRE costs and schedules
  - Qualification / Reliability for harsh environments
  - RF Convergence & Autonomy
- What are technical drivers?
  - Digitization over wide bandwidths and at high dynamic range to enable new capabilities
  - Common DSP HW/SW to reduce required equipment, lower power consumption and improve sustainability / upgradability
  - Integration of RF/analog and digital functions is required
- What are the supply chain issues?
  - Access to the most advanced technology but on-shore in low volumes
  - Parts obsolescence, Security, industry support
  - Possible solutions: standardized interfaces, IP-Reuse ecosystem

What are Some Metrics to Consider?

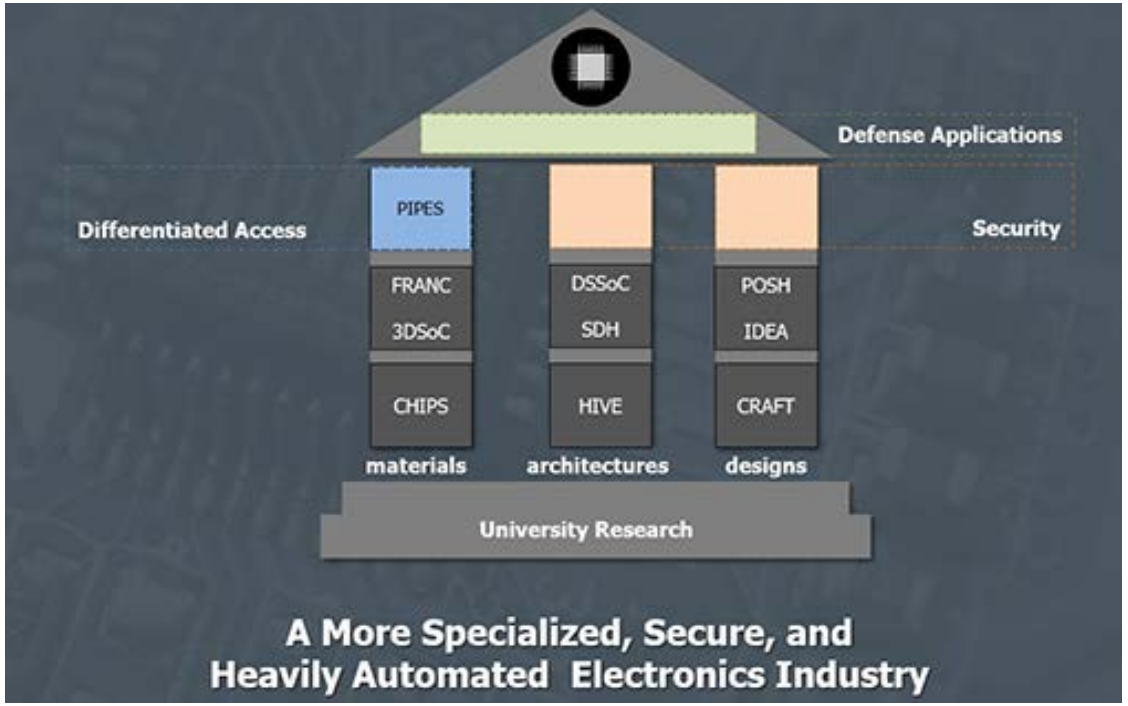
- **Performance:** data rate, latency, throughput, TFLOPs, insertion loss, isolation, dynamic range, etc
- **Energy/Power:** pJoules per bit, Throughput per Joules, TFLOPS/Joule, Leakage power etc.
- **Interfaces:** signaling protocols, error correction, interconnect lengths, ESD etc.
- **Thermal:** Maximum junction temperature, number of hot spots, power densities of hot spots
- **Electrical:** Power distribution losses to components inside package, losses in conversion, peak inductive noise, harmonic noise etc.
- **Reliability/Availability:** MTBF, radiation hardness, metric related to graceful degradation on component failures, lifetime ranges etc.
- **Others:** PLEASE SUGGEST!

3-D IC Classification



DARPA's Electronic Resurgence Initiative

- Today's critical Department of Defense (DOD) systems and platforms rely on advanced electronics to address national security objectives.
- To help tackle obstacles facing a half-century of electronics advancement, DARPA launched the Electronics Resurgence Initiative (ERI) – a five-year, upwards of $1.5 billion investment in the future of domestic electronic systems.

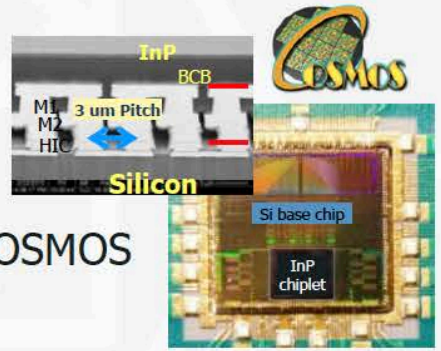


https://www.darpa.mil/news-events/electronics-resurgence-initiative-summit

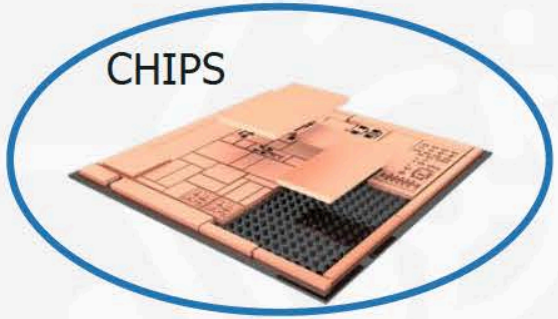
DARPA'S HISTORY OF INTEGRATION INNOVATION

ASEM

COSMOS

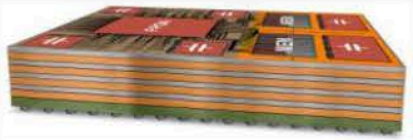


CHIPS

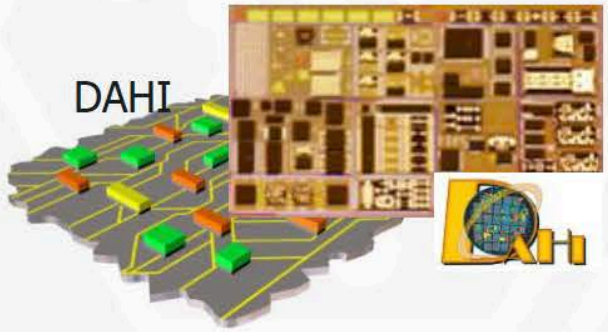


VISA

3D-IC

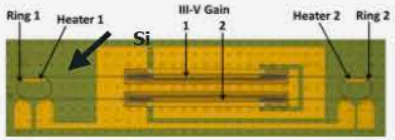


DAHI

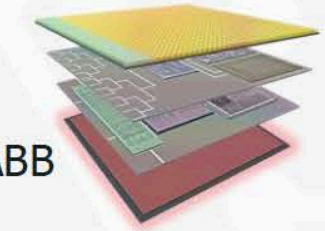


ASEM: Application Specific Electronic Modules
E-PHI: Electronic-Photonic Heterogeneous Integration
VISA: Vertically Integrated Sensor Arrays
COSMOS: Compound Semiconductor Materials on Silicon
DAHI: Diverse Accessible Heterogeneous Integration
MOABB: Modular Optical Aperture Building Blocks
CHIPS: Common Heterogeneous Integration and IP Reuse Strategies

E-PHI



MOABB



1990s 2000s 2010s 2020s

Source: DARPA

Sources: DARPA, Smithsonian Chips

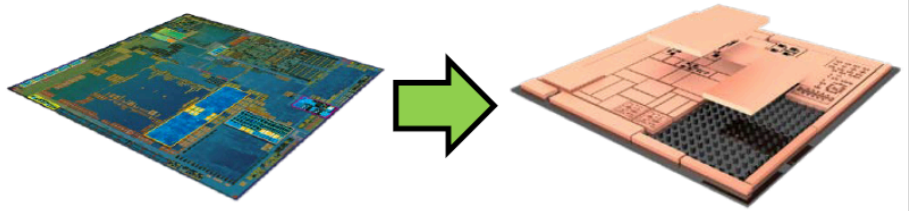
Emergence of Chiplets as the Evolution of Moore's Law

- Chiplets (smaller pieces of silicon) will enable their silicon architects to ship more powerful processors more quickly.
  - Shorter time to market to mix and match modular pieces linked by shorter data interconnections instead of complex SOC design
  - Lower design costs and risks
- Industry leaders like Intel and AMD are implementing chiplets strategies
  - Ramune Nagisetty, a senior principal engineer at Intel calls it "an evolution of Moore's law."
  - AMD's Papermaster: "I think the whole industry is going to be moving in this direction"
- DARPA is leading the development of "chiplet" ecosystem through its CHIPS program

https://www.wired.com/story/keep-pace-moores-law-chipmakers-turn-chiplets/

The CHIPS Program in a Nutshell

DESIGN



Today: Monolithic

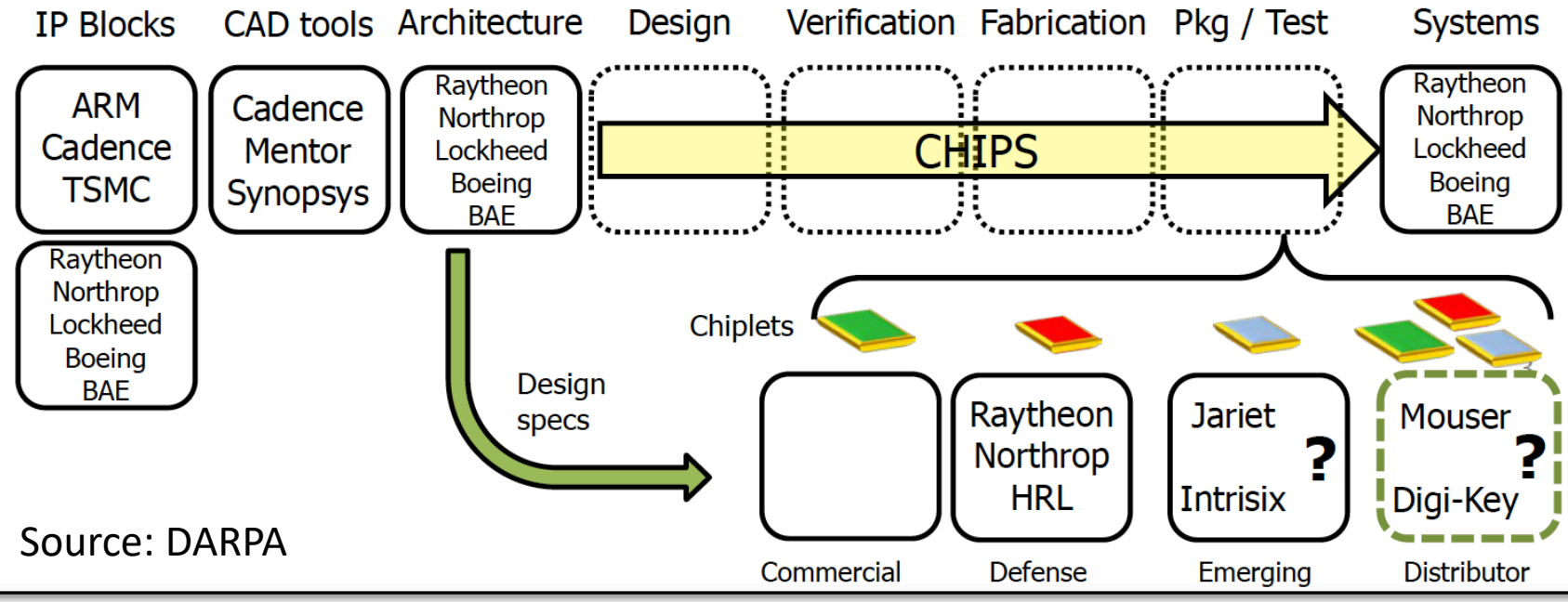
Tomorrow: Pseudolithic + Heterogeneous

Image source: Intel

TECHNOLOGY

- ✓ A universal CHIPS interface standard
- ✓ SOTA manufacturing for DoD
- ✓ A critical set of IP chiplets

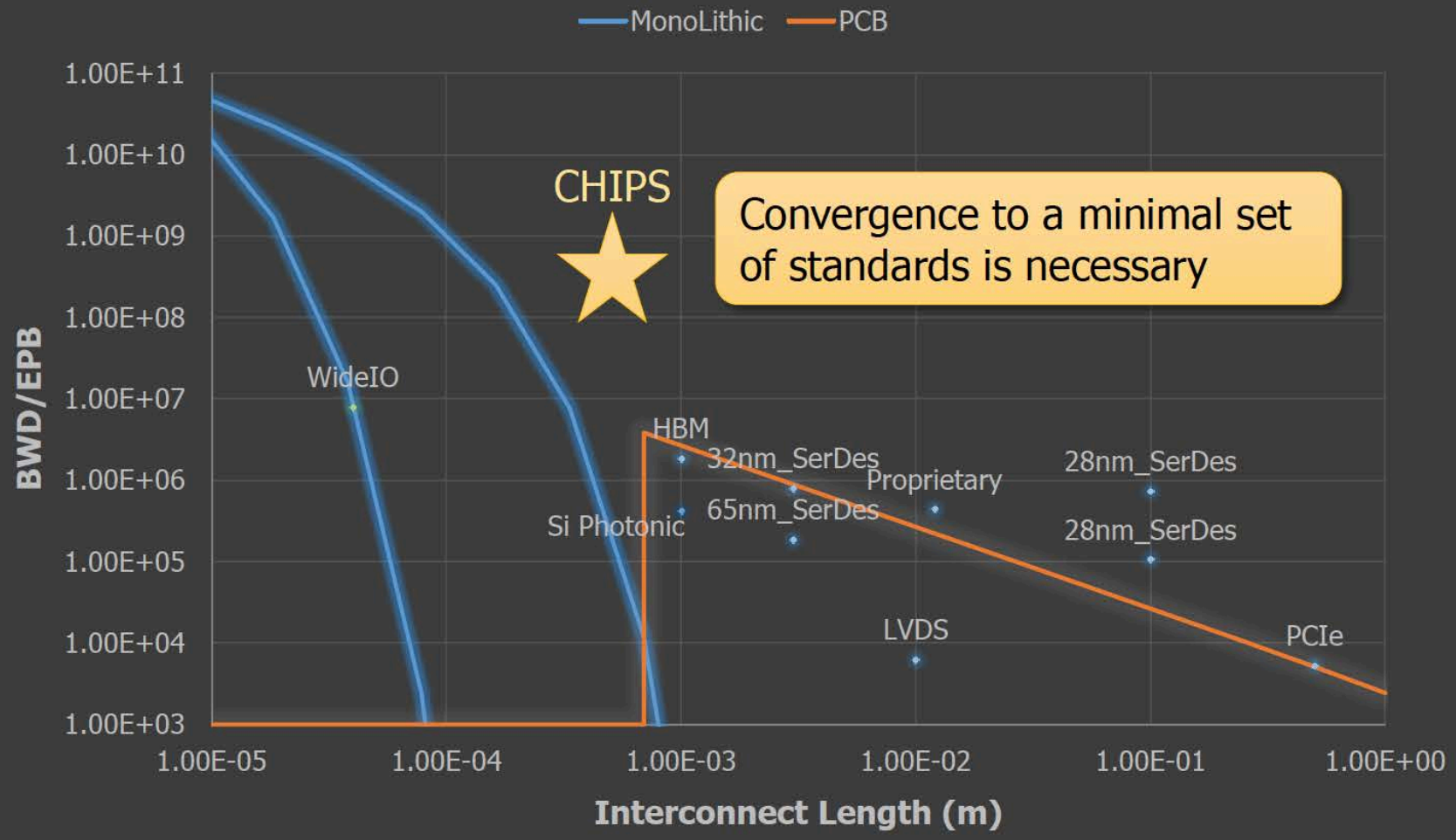
CHIPS END STATE



Source: DARPA

Interface standards: Too many? Not enough? How to compare?

$$\frac{Gbps/mm}{Energy/bit}$$



CHIPS challenge: make a usable interface standard

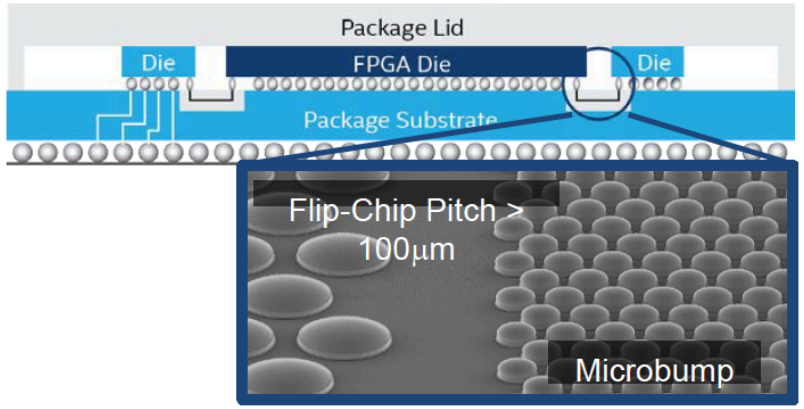
Impact of Advanced Electronics for DoD Today, DARPA: Dr. Jay Lewis, July 19,2017

Source: DARPA

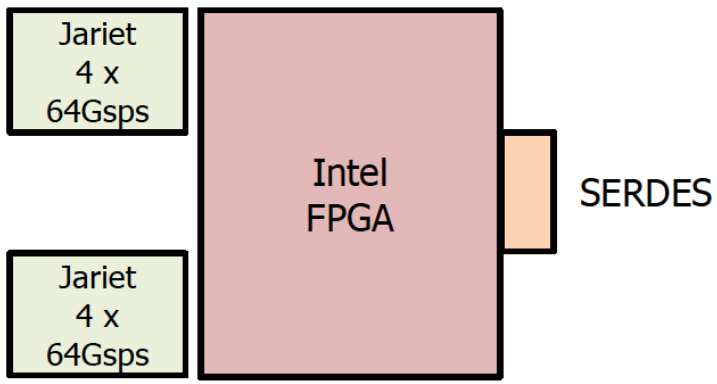
CHIPS Highlight #1: Heterogeneous Integration

Intel production proven manufacturing

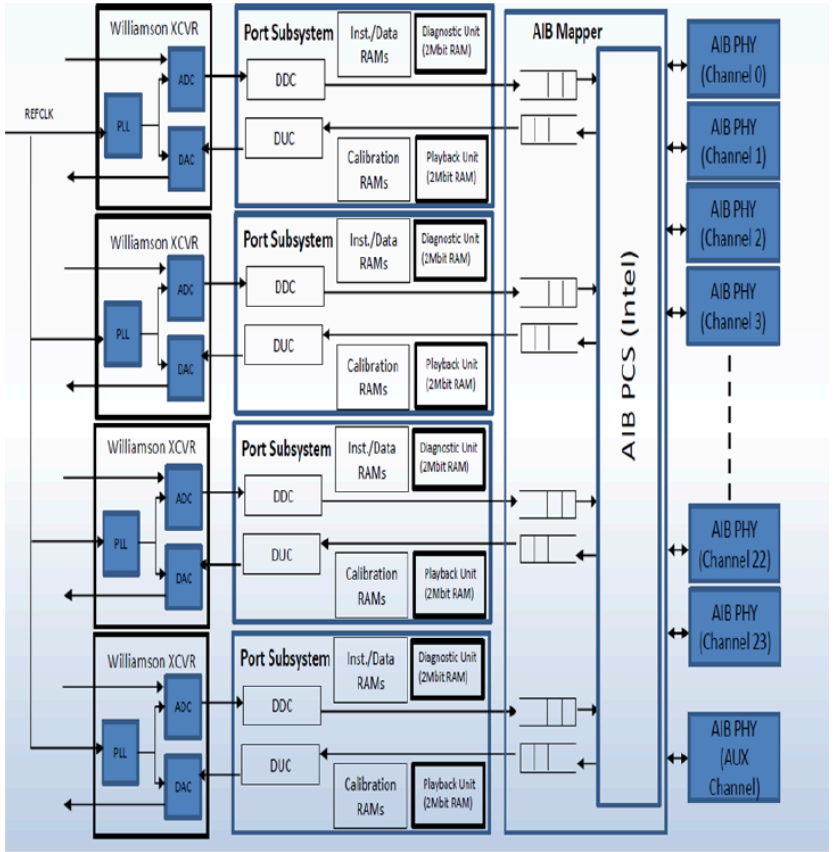
Intel® Stratix® 10 FPGAs and SoCs with Intel EMIB



Intel/CHIPS MCM using EMIB Technology with AIB interface standard



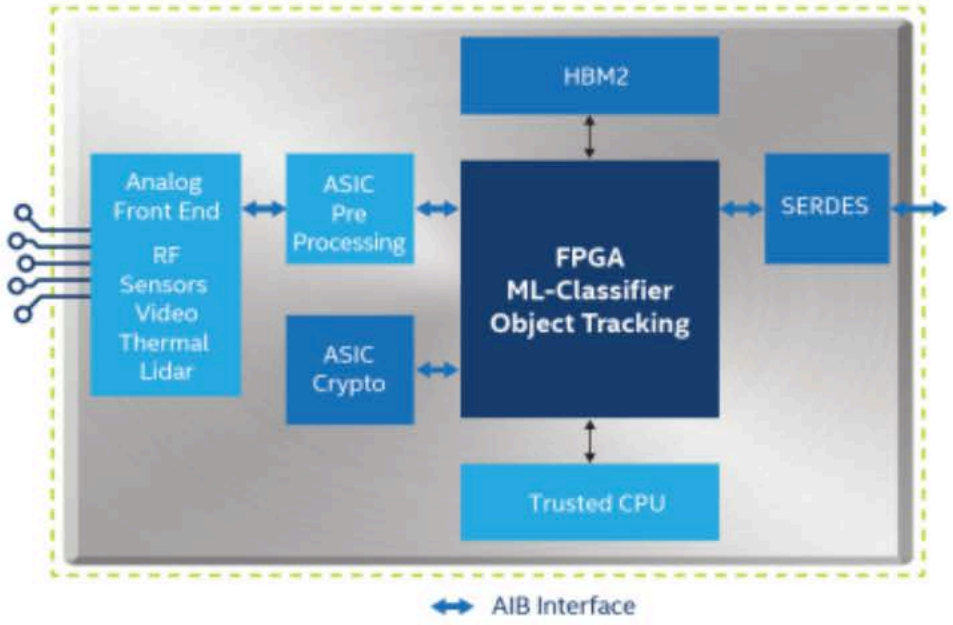
Jariet direct RF sampling at up to 64Gsps, with quad channel 10-bit ADC/DAC IP (existing, lab-proven ACT IP is being reused on CHIPS)



Source: DARPA

Image source: Intel, Jariet

Intel Advanced Interface Bus (AIB) Specification Advanced Interface Bus (AIB) Enables Modular Design



Intel's Advanced Interface Bus (AIB) is a die-to-die PHY level standard that enables a modular approach to system design with a library of chiplet intellectual property (IP) blocks.

AIB uses a clock forwarded parallel data transfer mechanism similar to DDR DRAM interfaces. AIB is process and packaging technology agnostic—Intel's Embedded Multi-Die Interconnect Bridge (EMIB) or TSMC's CoWoS* for example.

Intel now provides the AIB interface license royalty-free to enable a broad ecosystem of chiplets, design methodologies or service providers, foundries, packaging, and system vendors.

- AIB was supported by the DARPA CHIPS program.
- AIB specification is now available to the electronics community

Figure: *example of a possible heterogeneous system in package (SiP) that combines sensors, proprietary ASIC, FPGA, CPU, Memory and I/O using AIB as the chiplet interface.*

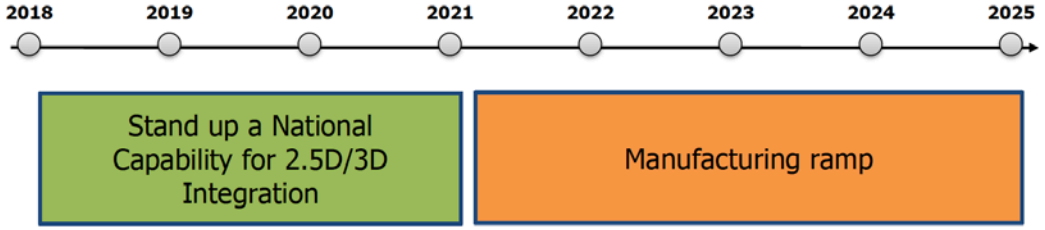
https://www.intel.com/content/www/us/en/architecture-and-technology/programmable/heterogeneous-integration/overview.html

DARPA CHIPS is now seeking to foster a Chiplet Ecosystem for DoD Users

CHIPS Manufacturing Wishlist

		Target Value
Dense Interconnect	Metallization material	Copper
	Front end metal layers	4 – 6
	Front end metal wiring density	~0.5 µm line/space
	Size (full reticle)	26 x 33 mm^2
	Stitching (strongly desired)	6" x 6"?
TSVs	Depth	100-200 µm
	Diameter	25 µm
	Pitch	150 µm
Assembly	Back side bump pitch	150 µm C4
	Back side RDL	Needed, C4 on via?
	Front end bump pitch	55 µm Cu (10 µm roadmap)
	Chiplets supported	7nm to 180nm
	Chiplets assembled	2 - 100

Potential Engagement Path



- Commercial **on-shore** manufacturing
  - (See previous slide)
  - Si interposer w/ TSVs
  - Organic package substrates
  - Copper bumping (<=55 µm)
  - C4 bumping (150 µm)
  - 2.5D assembly
  - 3D assembly
  - Flip Chip Assembly
  - SOTA automation
- Assemble all silicon sources!
- Turnkey model

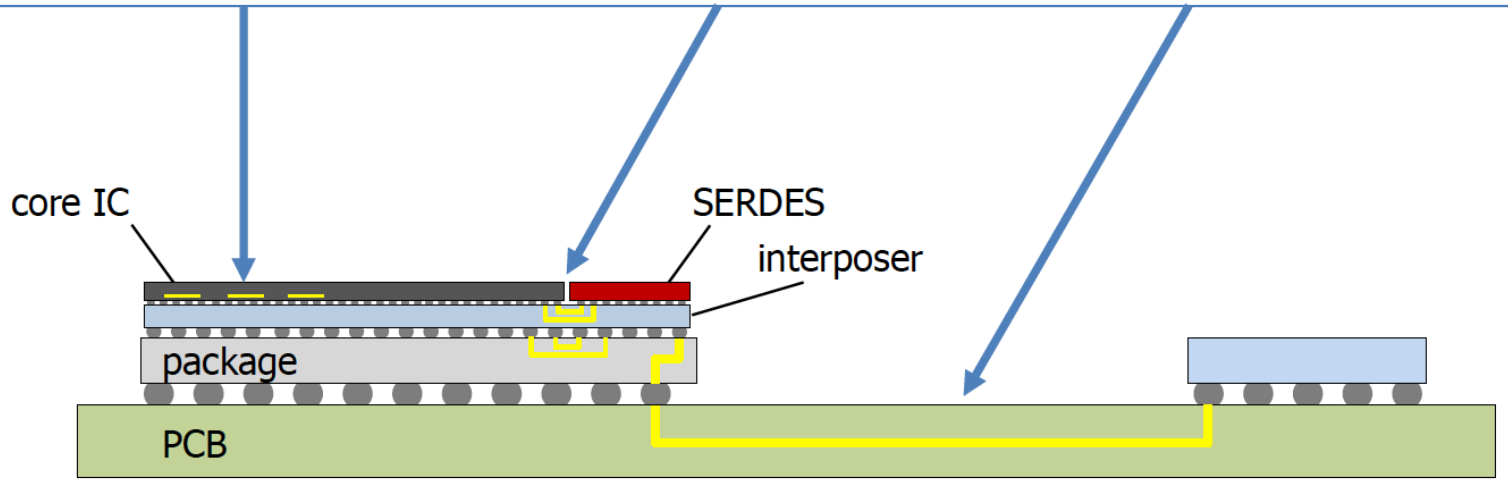
- "MOSIS for 2.5D"
- Agile PDK development
- Yield ramping
- Manufacturing cost optimization
- NPI cost optimization "zero" target
- Long Term Goals:
  - ~$20 turnkey packaging cost
  - 2 week assembly turn
  - Standard fab turns
  - Zero email order

Source: DARPA

State-of-the-art Electronic Signaling

Wide variety of engineering solutions

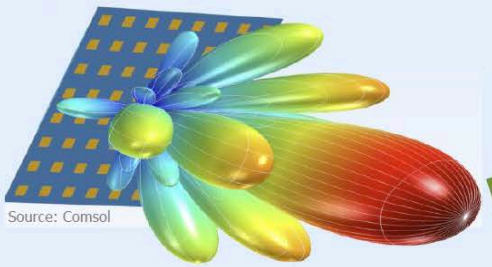
on chip wiring on monolithic die	**in package** wiring on MCM/SiP	**on board** PCB, cables, pins, connectors
• simple gate-to-gate link • full-swing, voltage mode • <100µm or repeaters • 1-100 fJ/bit	• AIB, UIB, USR, HBM • serial/fast or parallel/wide • moderate complexity • 0.1-2 pJ/bit	• PCI-E, LVDS, DDR, SERDES… • current-mode serial links • high complexity • 2-20 pJ/bit



DARPA PIPES -Photonics in the Package for Extreme Scalability

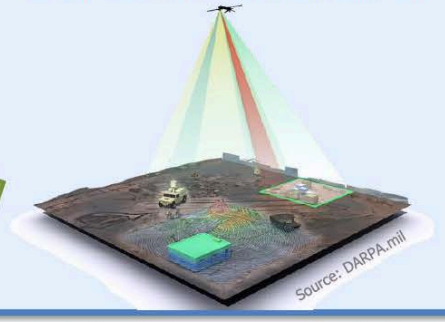
DARPA Applications Limited by Connectivity at All Length Scales

RF Phased Arrays – Radar & 5G
Improved Performance and System Scalability



sensors, edge, DoD

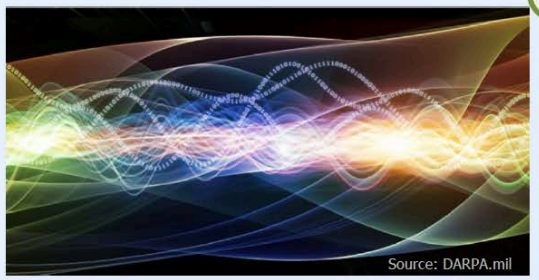
Digital Sensors – Imaging
Scaling Pixel Array Size, Frame Rate, and Power



PIPES Ecosystem

Establish sustained DoD access to domestic design, fabrication, and packaging capabilities

Machine Learning & Simulatio
Large-scale Modeling and Artificial Intelligence

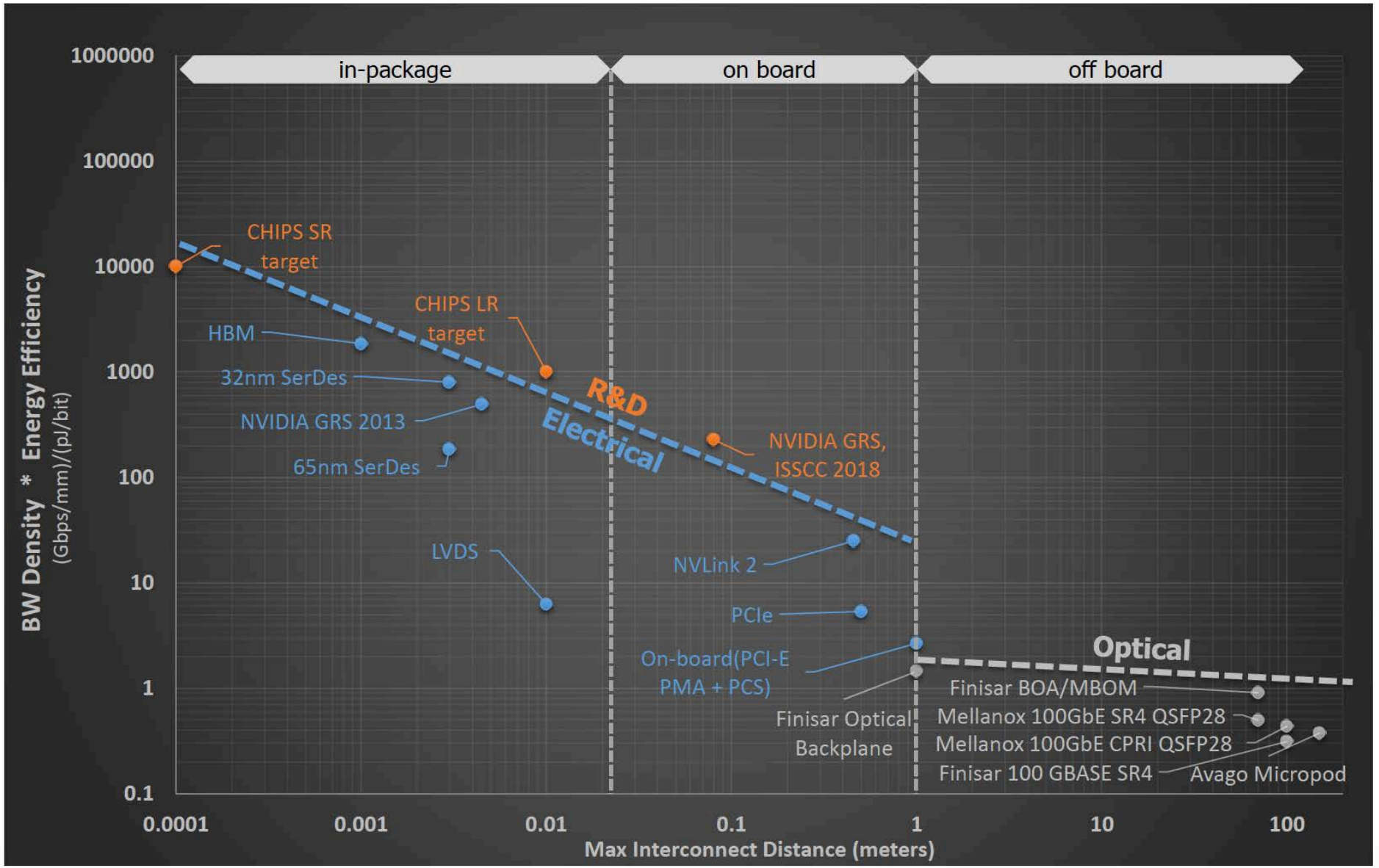


cloud, data center, HPC & AI

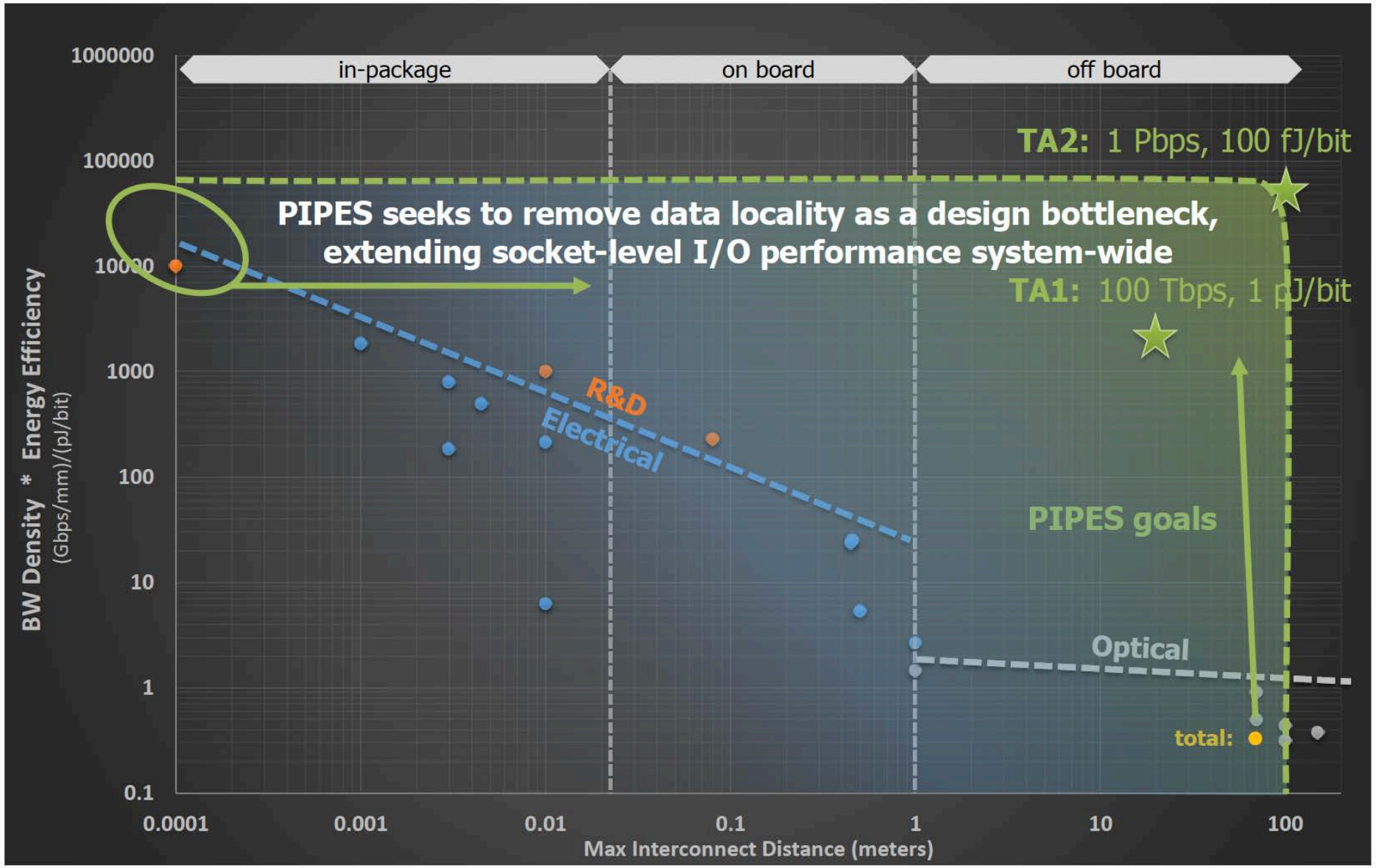
Computing & Data Analysis
Advanced Parallel Systems

Facilitating DoD Access: Create an ecosystem for package-level optical signaling, enabling disruptive advances for artificial intelligence, phased arrays, sensors and processing.

Interconnect Figure of Merit



Interconnect Figure of Merit



DARPA PIPES -Photonics in the Package for Extreme Scalability

Technology Transition with DoD Relevance

Capability providers

- photonic component fab
- optical chiplets, IP blocks
- interface definition
- optical and electrical packaging with custom ASICs

Commercial Participants

- build partnership business model and supply chain
- develop collaborations and discuss joint standards

PIPES Ecosystem

Establish sustained DoD access to domestic foundry and packaging capability

DoD Users

- leverage packaged MCMs
- access technologies for custom designs with new ASICs
- license IP, access trusted suppliers, on-shore packaging
- help define requirements, build prototypes, drive early adoption

Exercising the Ecosystem

- teaming and collaboration through PIPES discussions and "demo phase" activities

DARPA investment

- fill technology gaps,
- connect stakeholders

TA1: Photonically-Enabled Multi-Chip Modules (MCMs)

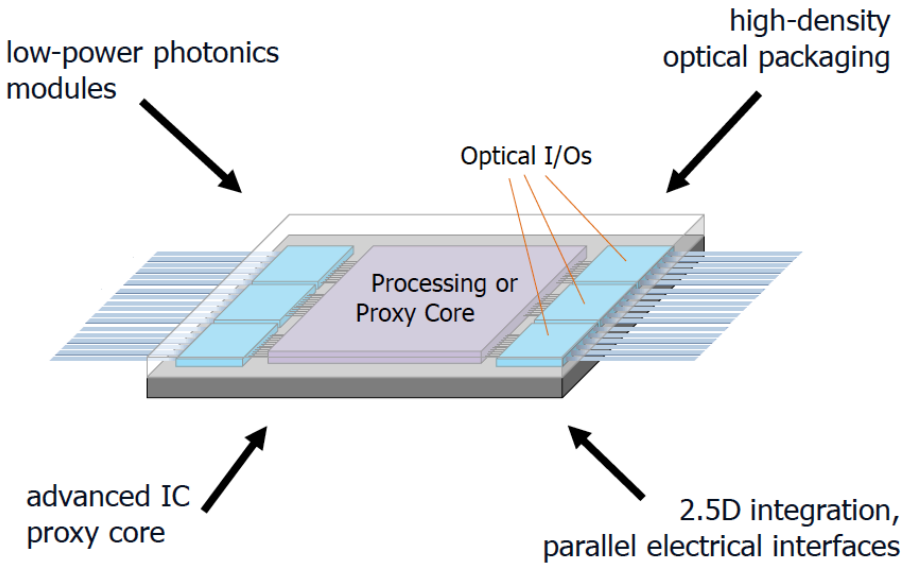
Objective

- Enable **disruptive microelectronics** by embedding photonics in FPGA, GPU, ASIC
- Drive link **energy, density, and BW 10x** beyond current R&D results
- Establish **DoD-accessible ecosystem** for photonically-enabled 2.5D microelectronics

Key Metrics and Deliverables

- Create **enduring domestic capability** for manufacturing and packaging
- **100 Tbps I/O** per IC package (10x SOTA)
- **1 pJ/bit** efficiency (10x SOTA)
- 20 meter reach / 100 ns latency
- Packaged **mission-relevant MCM demo**

100 Tbps DoD-Accessible Capability

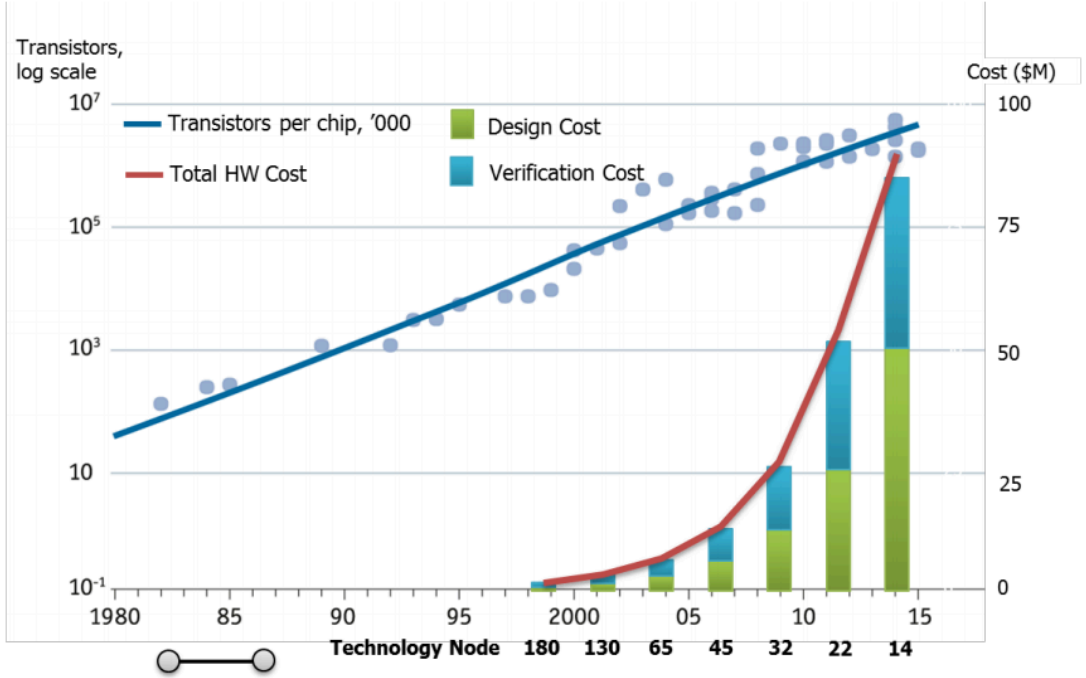


Key Challenges

- high-volume manufacturing & low parasitics
- low-loss fiber coupling & multiplexing
- compact, low-energy Tx/Rx circuits
- high-order multiplexing

Leverage and extend recent R&D innovation for DoD system insertion

Lowering barriers to hardware innovation



New procedures for physical design and verification will lower the design barrier, enabling rapid specialization

Design

Intelligent Design of Electronic Assets (IDEA)

- No human in the loop" 24-hour layout generation for mixed signal integrated circuits, systems-in-package, and printed circuit boards.Machine generated layout of electrical circuits and systems

Verification

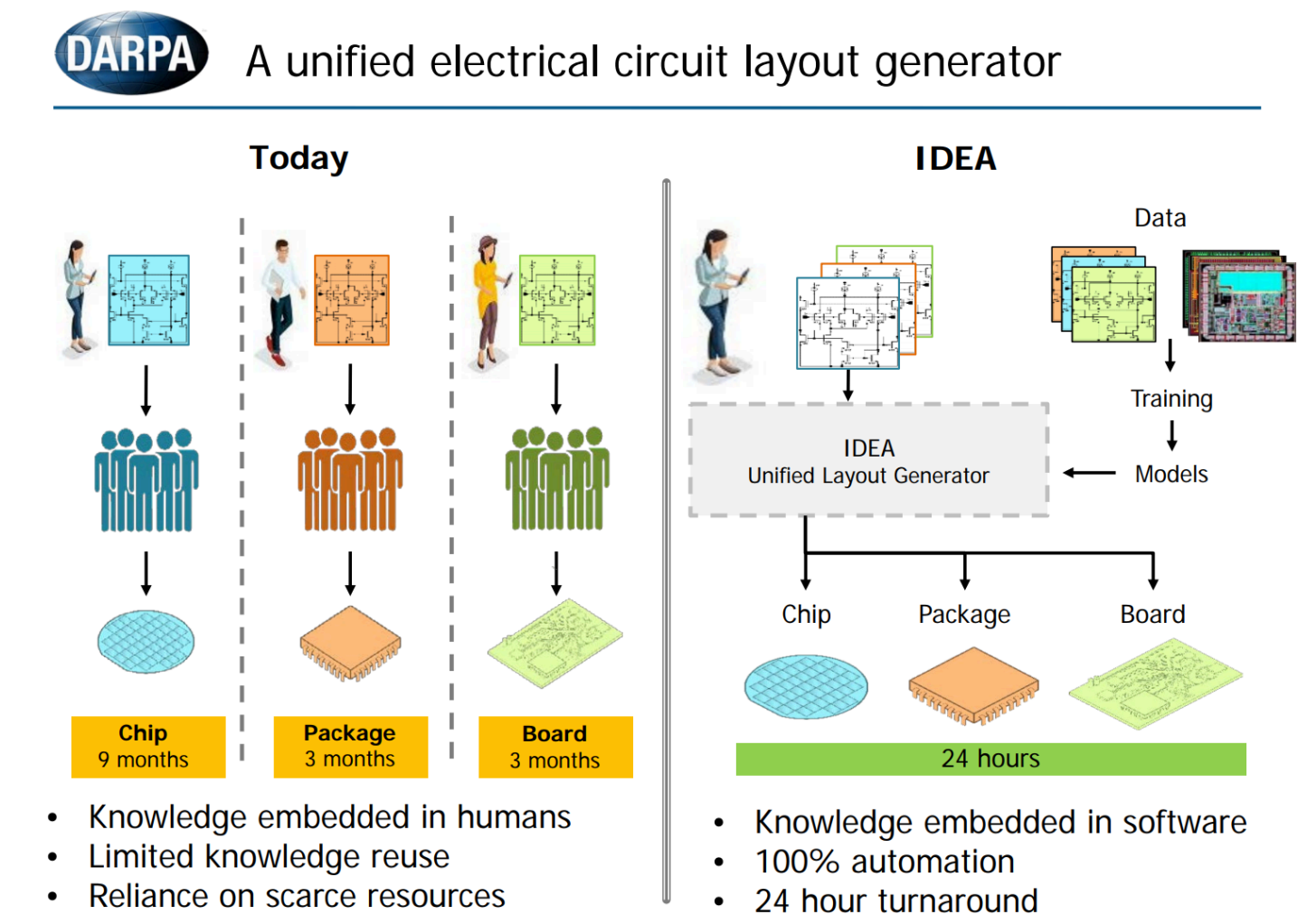
Posh Open Source Hardware (POSH)

- An open source System on Chip (SoC) design and verification eco-system that enables cost effective design of ultra-complex SoCs.

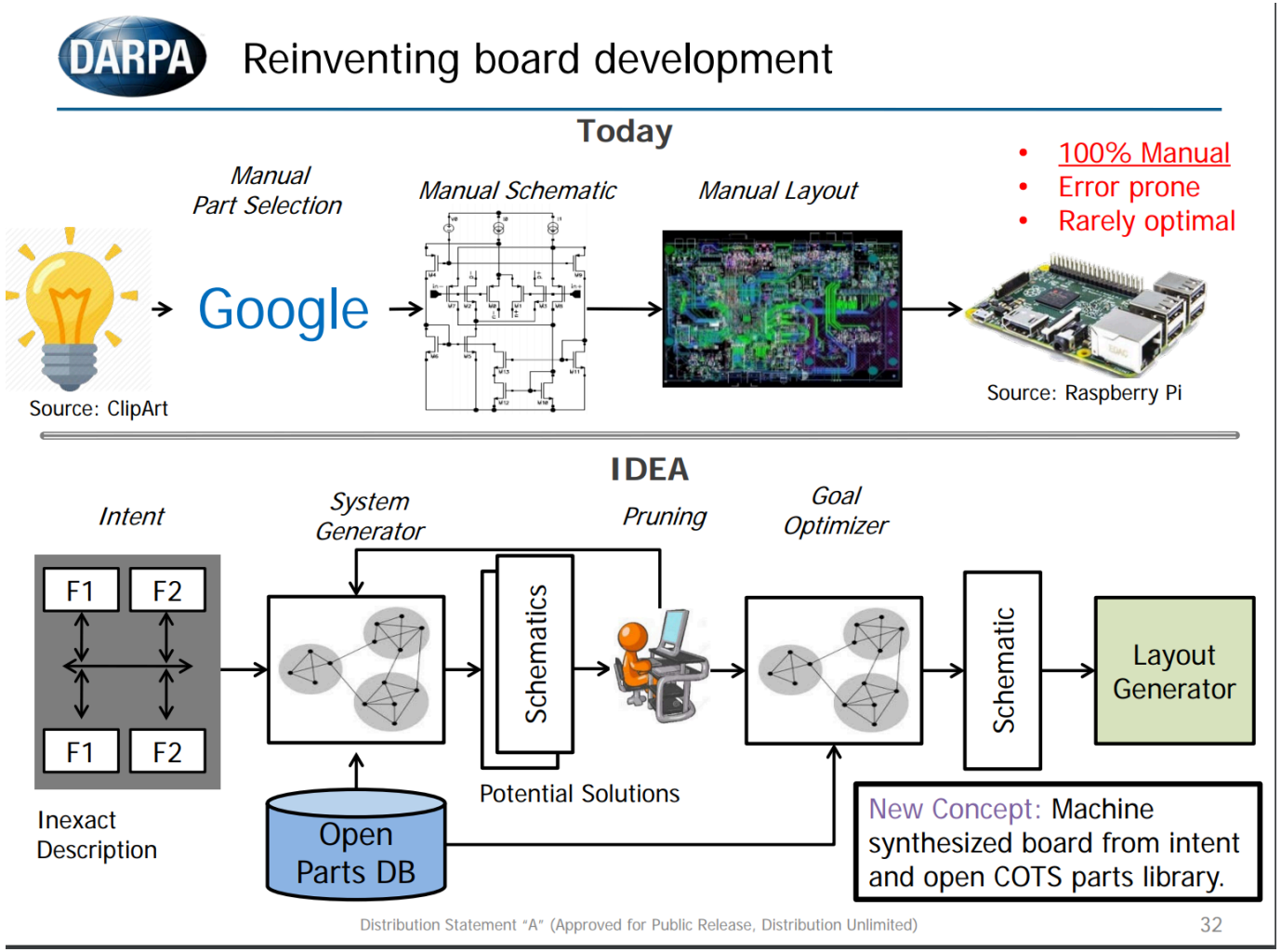
The 1980's DARPA MOSIS effort removed fab cost and fab access barriers and launched the fabless industry. The ERI Design effort will address today's design complexity and cost barriers, creating the environment needed for the next wave of US semiconductor innovation.

DARPA IDEA

- IDEA aims to create a "no human in the loop" 24 hour turnaround layout generator for System-On-Chips, System-In-Packages, and Printed Circuit Boards.



DARPA IDEA


DARPA
Reinventing board development
Today
Manual Part Selection
Manual Schematic
Manual Layout
100% Manual
Error prone
Rarely optimal
Google
Source: ClipArt
Source: Raspberry Pi
IDEA
Intent
System Generator
Pruning
Goal Optimizer
F1
F2
F1
F2
Schematics
Schematic
Layout Generator
Inexact Description
Open Parts DB
Potential Solutions
New Concept: Machine synthesized board from intent and open COTS parts library.
Distribution Statement "A" (Approved for Public Release, Distribution Unlimited)
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The TWG for Developing the Heterogeneous Integration Roadmap for Aerospace and Defense

- Goal: develop a **roadmap for heterogeneously integrated components for applications in Aerospace and Defense**
- **Specific goals:**
  - Identify the A-D specific challenges in the next 5, 10 and 15 year horizons
  - Identify promising solutions and technologies
  - Identify any unaddressed challenges and the types of solution/ technologies needed
  - Document all of these as a chapter in the overall HIR document

The HIR TWG for Aerospace and Defense

- **Outlook:** 5, 10 and 15 years
- Reports will be freely available on the IEEE EPS and Semi websites
  - All based on publicly available data
  - This TWG collectively authors a **single chapter** contributing towards the overall HIR
- **Goals:**
  - Define needs and develop goals
  - Identify challenges/obstacles, working with existing cross-TWGs
  - Identify potential solutions that look promising
  - Identify gaps, research challenges/needs in the coming years for realizing the goals
- We solicit input on ALL aspects of this TWG

HIR Technical Working Group

HETEROGENEOUS INTEGRATION ROADMAP

Heterogeneous Integration Components

- Single Chip and Multi Chip Packaging (including Substrates)
- Integrated Photonics
- Integrated Power Devices
- MEMS & Sensor integration
- RF and Analog Mixed Signal

Cross Cutting topics

- Materials & Emerging Research Materials
- Emerging Research Devices
- Interconnect
- Test
- Supply Chain

Integration Processes

- SiP
- 3D +2.5D
- WLP (fan in and fan out)

HI for Vertical Applications

- Mobile
- IoT and Wearable
- Medical and Health
- Automotive
- **High Performance Computing & Data Center**
- **Aerospace & Defense (Tim Lee, Boeing, Jeffrey Demmin, BAH)**

Design

- Co-Design & Simulation – Tools & Practice
  - Device, package, subsystem & system levels

HETEROGENEOUS INTEGRATION ROADMAP

We like to invite you all to consider joining in the Heterogeneous Integration Roadmap Development and participate in contributing to the Aerospace and Defense Technical Working Group.

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Jeffrey Demmim, demmin_jeffrey@bah.com

Thank you