Heterogeneous Integration Roadmap
Integrated Power Electronics TWG

Doug Hopkins, Ph.D. (Chair)

Doug is a Professor of Electrical and Computer Engineering at NC State University where he founded the Laboratory for Packaging Research in Electronic Energy Systems (PREES). Doug has over 20 years of experience in electronic energy systems. He is a senior member of IEEE and a fellow of IMAPS.

Patrick McCluskey, Ph.D. (Co-Chair) Today’s Presenter

Patrick is a Professor of Mechanical Engineering at the University of Maryland, College Park with 25 years research experience in power electronics packaging. He is the Chair of the Energy and Power Electronics technical committee and a member of the board of governors of IEEE EPS. He is a fellow of IMAPS.
**Heterogeneous Integration of Power (HIP)**

HIP is defined as the integration of separately manufactured power electronic components and subsystems into higher-level assemblies (SiP, PCB/Substrate-embedded systems) that in the aggregate provide enhanced functionality and improved operating characteristics.

**HIP is critical to efficiently distribute clean power to multiple devices requiring widely different voltages and currents.**

SiP through Heterogeneous Integration

- Power passives
- High current Inductors
- Low profile passives
- Power distribution planes
- Advanced materials
- Heat spreaders, heat sinks
- Active cooling systems
- Power semiconductors
- EMI shielding
- Unique design architectures
Critical Challenges of Power Integration

**HIP is critical to efficiently distribute clean power to multiple devices requiring different voltages and currents.**

- **Efficiently** - Reduce power loss so as to minimize need for cooling
  - Reduction in distribution line impedance
  - Reduction in device conversion losses (e.g. switching loss, winding loss)
  - Operation at high frequency
  - Isolation of heat from temperature sensitive components (i.e. selective cooling)

- **Clean** – Minimize noise generated in the devices by power distribution
  - EMI interference, cross-talk
  - $\Delta I$ noise (i.e., switching noise) at high $dl/dt$ or high $dV/dt$
  - $1/f$ noise

- **Multiple** – Distribution to many different devices and device types
  - Each different device and function requires a specific voltage and current to be delivered
  - Multiple conversion steps to supply array of voltages and currents required
  - Efficient scheme to minimize conversions to reduce losses.
Heterogeneous Integration of Power (HIP) Two Directions

Self-Contained Power Electronic Devices  Power Distribution in Integrated Systems

Stand alone  Integrated

Covered by IEEE PELS Roadmap  Cooperation  Covered by IEEE EPS HI Roadmap
In order to address these challenges, the IPE TWG has......

• Analyzed the impact of current and future market drivers
• Identified SiP power distribution requirements
• Identified power metrics for major SiP components (with assistance of component TWGs)
• Identified major challenges and barriers
• Assessed the status of manufacturing Infrastructure
• Identified key enabling packaging technologies
• Set project goals and time horizons
Current Technology Landscape - Overview

- **Current foundational technologies - 2018**
  - Mature semiconductor technology
  - Maturing FOWLP technology L/S = 5um
  - Large panel FOPLP technology entering volume production (L) L/S = 10-15um
  - Active/passive component embedding on large panels in R&D L/S = 20-30um
  - Maturing MEMS & SENSOR technology
  - 2.5D and 3D Packaging technologies are in volume production
  - Wide bandgap semiconductor technology is maturing
  - Manufacturing infrastructure still evolving

- **Current technology drivers**
  - Mobile communication, storage, cloud computing IoT

- **Current technology gaps**
  - High quality, low-profile inductors, capacitors, embeddable power semiconductor devices
  - Thin high voltage materials for stacking
  - Low cost advanced integrated thermal management solutions (integration of fluidics)
  - Multifunctional elements
  - Use of additive manufacturing
  - Too many unique “boutique” processes, tightly controlled PDKs), lack of standards
Key Technologies for Power Integration

- **Efficiently** - Reduce power loss so as to minimize need for cooling
  - Wide bandgap power devices that can operate at high frequency (e.g. GaN) - PELS
  - New trace materials and shorter lengths to reduce interconnect/winding resistance
  - Zero voltage switching to reduce switching loss; lower core loss inductors
  - Thermal isolation through glass and low k substrates, thermal metamaterials on layers
- **Clean** – Minimize noise generated in the devices by power distribution
  - Shielding, low permeability materials, reduced coupling, eddy currents – lower EMI
  - Lower inductance through flip chip, Cu bumps, HDI, SiPLIT to lower $\Delta I$ noise
  - Decoupling – put power transmission on every interconnect level.
- **Multiple** – Distribution to many different devices and device types
  - Efficient scheme to minimize conversions to reduce losses – PELS
  - Embeddable components close to the devices being powered
  - Multiphysics simulation and co-design
Power Delivery

Minimize the stages of power conversion;
Perform power conversion right near the load;

Utilize Advances in:
- GaN
- CMOS integration
- Topologies
- Passive components

P M Raj, FIU and Georgia Tech
Figures from EPC (Alex Lidow) and IBM Zurich (Arvind Sridhar)
Capacitors are key enablers in HIP SIP
Unique opportunities for switched capacitor architectures
# Capacitor Benchmarking

<table>
<thead>
<tr>
<th></th>
<th>Murata Thin MLCC</th>
<th>IPDiA Silicon Trench</th>
<th>AVX Ta Chip</th>
<th>Strategic Need</th>
</tr>
</thead>
<tbody>
<tr>
<td>Volumetric Density</td>
<td>20 μF/mm³</td>
<td>5 μF/mm³</td>
<td>~10 μF/mm³</td>
<td>20 μF/mm³</td>
</tr>
<tr>
<td>Thickness</td>
<td>100 μm</td>
<td>100 μm</td>
<td>600 μm</td>
<td>50-100 μm</td>
</tr>
<tr>
<td>Freq. Stability</td>
<td>10-100 MHz</td>
<td>&gt;1-10 MHz</td>
<td>200 kHz</td>
<td>&gt;1-10 MHz</td>
</tr>
<tr>
<td>ESR</td>
<td>~10 mΩ</td>
<td>50 mΩ x μF</td>
<td>&gt;100 mΩ x μF</td>
<td>~50 mΩ x μF</td>
</tr>
<tr>
<td>% ΔC/V</td>
<td>-13 % to -70%</td>
<td>~ 0 %</td>
<td>~ 0 %</td>
<td>~ 0 %</td>
</tr>
<tr>
<td>Max. Temp</td>
<td>85° C</td>
<td>150° C</td>
<td>125° C</td>
<td>125° C</td>
</tr>
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**FILM EMBEDDING**

**WAFER OR PANEL INTERCONNECTS**
Embedded Film Capacitors

Board or package embedding; I/O decoupling; 100 MHz

- Embedded polymer laminate and dielectrics:
  - 0.1 nF/mm²
  - 0.5 nF/mm²
- Polymer laminate dielectrics
- Polymer film dielectrics

2000 2008 2016 2020

Package embedding;
Core and I/O decoupling; 100-500 MHz

- Embedded ceramic film:
  - 2-3 nF/mm²
  - Thin oxides
  - 20-30 nF/mm²
  - BaTiO₃ film
  - 30-50 nF/mm²
  - enabled by PLZT

Capacitors –
wafer

- Silicon capacitors Deep trench
  - 0.08 µF/mm²
  - 0.25 µF/mm²
  - 0.5 µF/mm²
- Ultra-high surface area silicon 1-2 µF/mm²
- Multilayered dielectrics on deep trench

IVR; Embedded PoL
1-20 MHz

- Embedded Ta electrode
  - 2 µF/mm²
  - >3 µF/mm²

Formed capacitors
Panel

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### Team is growing.

<table>
<thead>
<tr>
<th>NAME</th>
<th>AFFILIATION</th>
<th>ROLE</th>
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<tbody>
<tr>
<td>Patrick McCluskey</td>
<td>Univ. of Maryland, College Park</td>
<td>Co-Chair</td>
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<tr>
<td>Douglas C Hopkins</td>
<td>North Carolina State Univ.</td>
<td>Chair</td>
</tr>
<tr>
<td>Markondeya ‘Raj’ Pulugurtha</td>
<td>Florida International University</td>
<td>New Technologies</td>
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<tr>
<td>Luu Nguyen</td>
<td>Texas Instruments, Retired</td>
<td>Chief Reviewer</td>
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<tr>
<td>Don Draper</td>
<td>Consultant</td>
<td>Power Minimization</td>
</tr>
</tbody>
</table>

The team is growing.
# Status of Write-up

<table>
<thead>
<tr>
<th>TASK</th>
<th>COMPLETE</th>
<th>ONGOING</th>
<th>STILL TO DO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Team Assembled</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Challenges Identified</td>
<td>X</td>
<td></td>
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</tr>
<tr>
<td>Writing Assignments Distributed</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Potential Solutions Identified</td>
<td>X</td>
<td></td>
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<tr>
<td>Roadmap Steps (5 yr, 10 yr, 15 yr) Determined</td>
<td></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Collaboration with IEEE PELS</td>
<td></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Final Version of the Chapter</td>
<td></td>
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<td>X</td>
</tr>
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Independent Power Devices are mapped through the PSMA “Embedded Component Study.” and IEEE PELS Wide Bandgap roadmaps

Next Version: Collaborate More Extensively with PELS and PSMA
**Next Version:**

**Address Distribution Topology**

1. **Power in SiP Distribution**
   - Uses SiP Pkg&Mfg technologies to distribute power from Discrete Power converters

2. **Peripheral Power Distribution**
   - Uses the same “Component” Pkg&Mfg technologies to create power conversion at the interface with the SiP

3. **On-Chip Power Conversion and Distribution**
   - Uses “Component” Pkg&Mfg technologies to create distributed power conversion
Next Version: Specifically Address Planar Magnetics

- Inductor magnetic saturation and $R_{dc}$ are limiting. These specifications define volume, optimal form factor
- In embedded HIP SiP height is limiting. We need planar magnetics

Innovation is needed!