



# **HETEROGENEOUS INTEGRATION ROADMAP 2019 Edition**

## **Chapter 7: Mobile**

<http://eps.ieee.org/hir>

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## Chapter 7: Mobile

This chapter is in preparation, and will be integrated into the Roadmap at Version 1.1, planned for the end of 2019. In its place is the following summary and a series of slides giving the current status of mobile electronics and some information that is relevant to the progress needed over the next 10 to 15 years.

### Executive Summary

Mobile is a major driver for electronics innovation, representing a large proportion of electronics market revenue, the largest consumption of advanced nodes semiconductors, and – perhaps most important of all – is the technology directly used by 75 %-80 % of the global population...

The mobile chapter is one of the six market application chapters in the Heterogeneous Integration Roadmap (HIR). The mission of the Mobile Technical Working Group (TWG) is to articulate the market and technology landscape, identify challenges and roadblocks for heterogeneous integration technologies, and their potential solutions for future generation of heterogeneous integration requirement in mobile device and mobile infrastructure. In this 1st edition of the HIR Mobile Chapter we shall put major emphasis on articulating the driving forces and leading-edge packaging technology as the base foundation from which to project the future directions with near- and long-term horizons. The working plan is:

- Overview the market landscape, driving forces and future directions
- Review the heterogeneous integration focus in mobile
- Articulate crucial enabling heterogeneous integration technologies
- Describe linkage to other HIR Chapters to bring out the full picture
- Project future directions, challenges and potential solutions – near and long term
- Plan for the next edition

# *Heterogeneous Integration Roadmap*



## MOBILE

Technical Working Group

William Chen, Chair

Benson Chan, Mark Gerber, Brandon Prior



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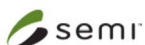
## Outline

- Executive Summary
  - Mobile Technical Working Group Mission and Plan
- The Big Picture
  - Mobile Economy and Global Mobile Network
  - Data Growth and 5G
- Heterogeneous Integration inside the Smart Phone
  - Die Stacking & Package-on-Package (PoP)
  - Inside the Premier Smart Phones
- 5G – Area for Innovation and Creativity
  - 5G in the Smart Phone
  - Antenna-in-Package (AiP)
- Heterogeneous Integration for the Mobile Network
- Future Visions
- Wrap-up
  - Difficult Challenges
  - Summary
- References and Acknowledgments

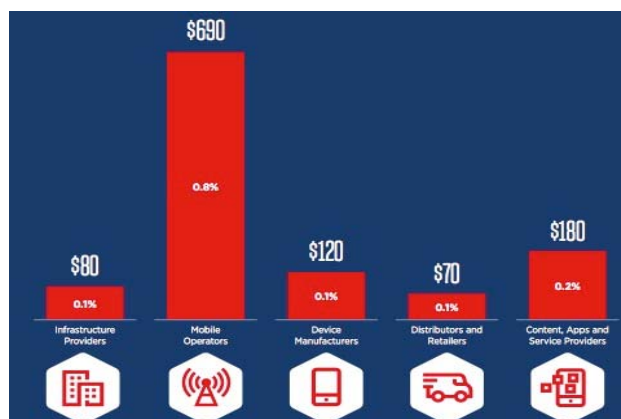


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## The Big Picture



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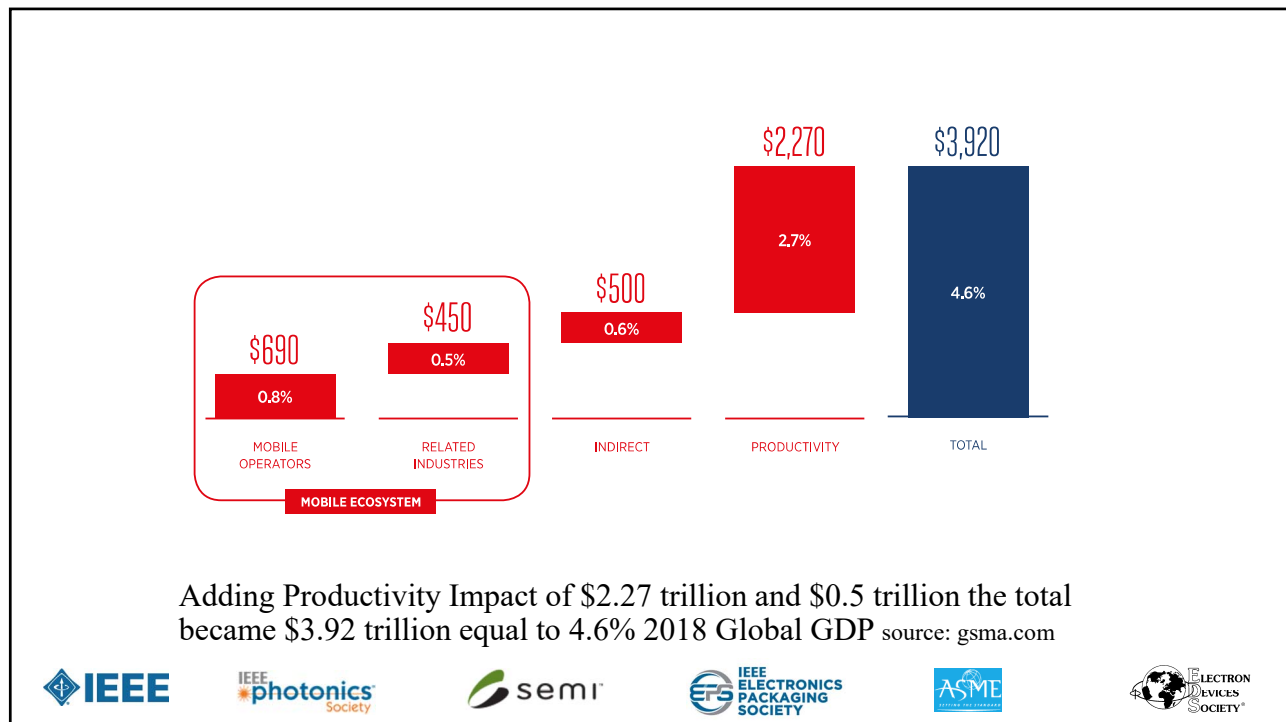


### Mobile Contribution: \$1.14 Trillion to 2018 Global GDP

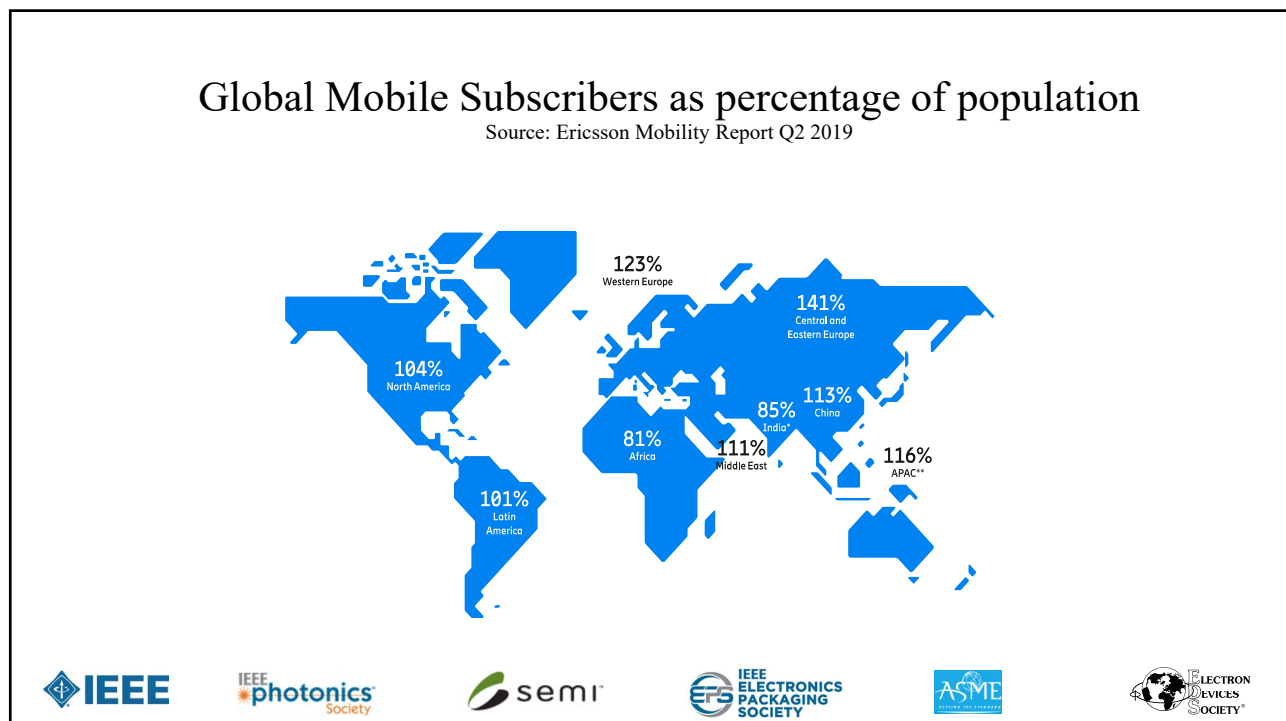
GSMA ([www.gsma.com](http://www.gsma.com)) is an industry association representing the worldwide mobile communication industry. In GSMA report “The Mobile Economy 2019” the mobile industry contributed \$1.14 trillion to 2018 Global GDP, as shown above.



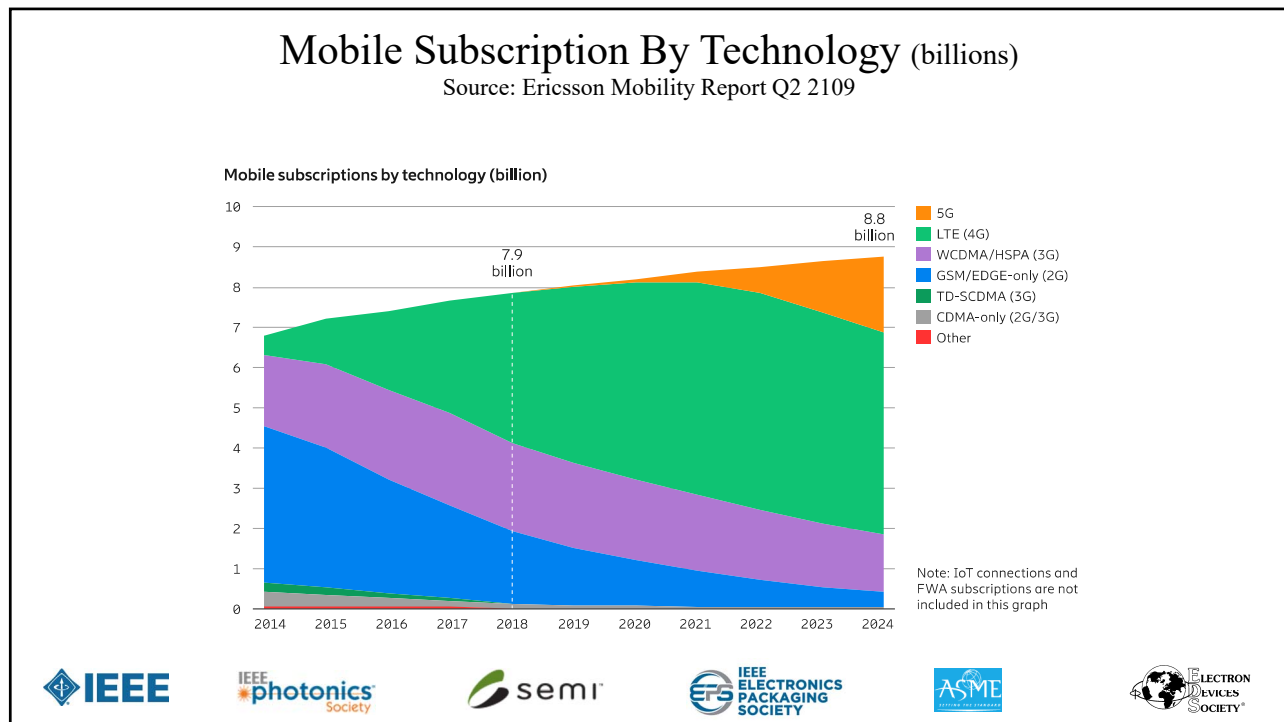
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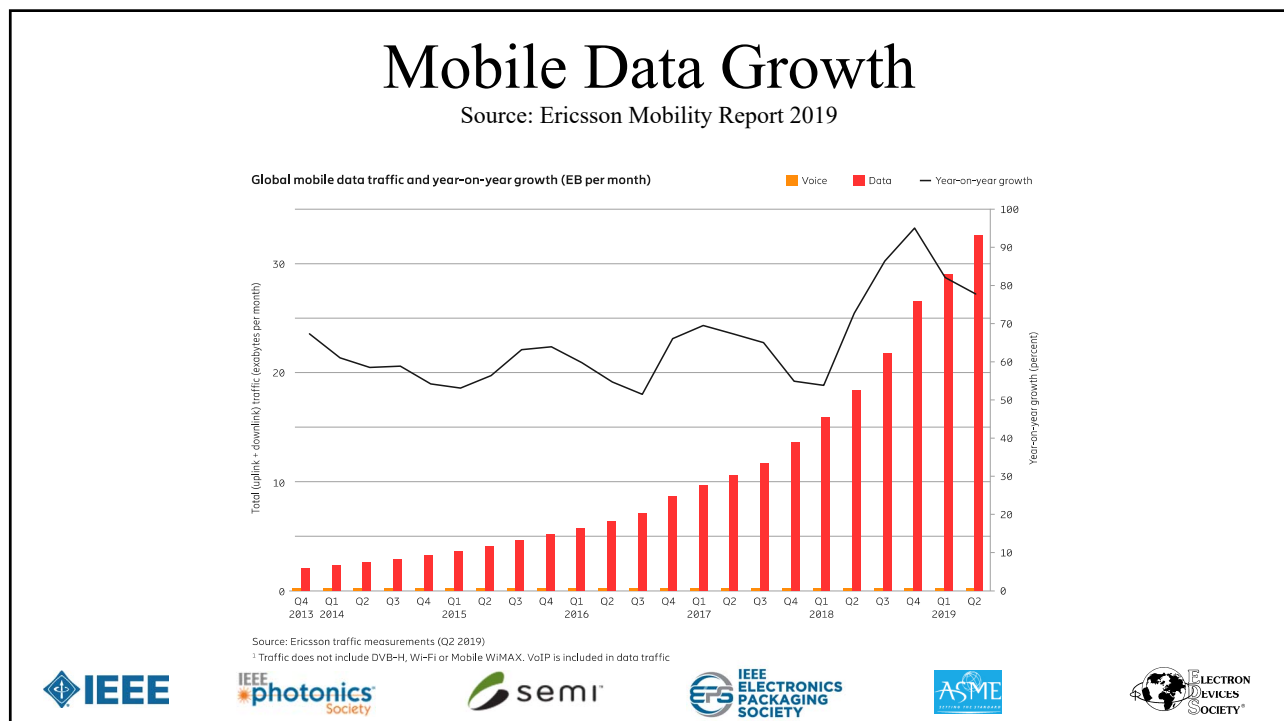
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Segment	2018	2019	2020	2021
5G	612.9	2,211.4	4,176.0	6,805.6
2G	1,503.1	697.5	406.5	285.2
3G	5,578.4	3,694.0	2,464.3	1,558.0
LTE and 4G	20,454.7	19,322.4	18,278.2	16,352.7
Small Cells	4,785.6	5,378.4	5,858.1	6,473.1
Mobile Core	4,599.0	4,621.0	4,787.3	5,009.5
<b>Total</b>	<b>37,533.6</b>	<b>35,924.7</b>	<b>35,970.5</b>	<b>36,484.1</b>

### CSP Wireless Infrastructure Revenue Forecast (source: Gartner 08-22-2019)

Gartner (08-22-2019) projected that communication service providers (CSPs) using non-stand alone (NSA) technology to introduce 5G service initially. New Radio 5G (NR) equipment will start to roll out in 2020.



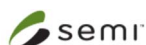
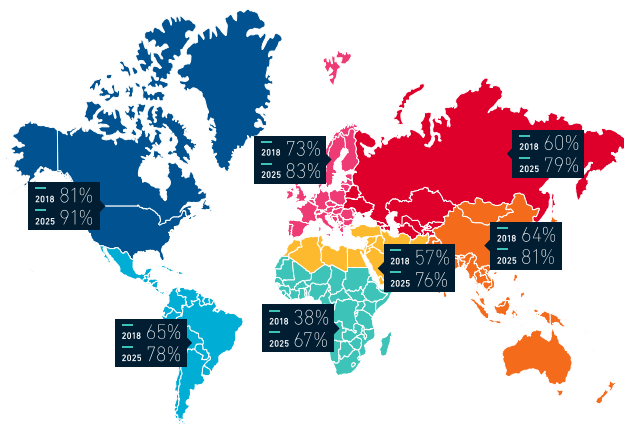
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## Global Smart Phone Adoption

Source: GSMA The Mobile Economy 2019

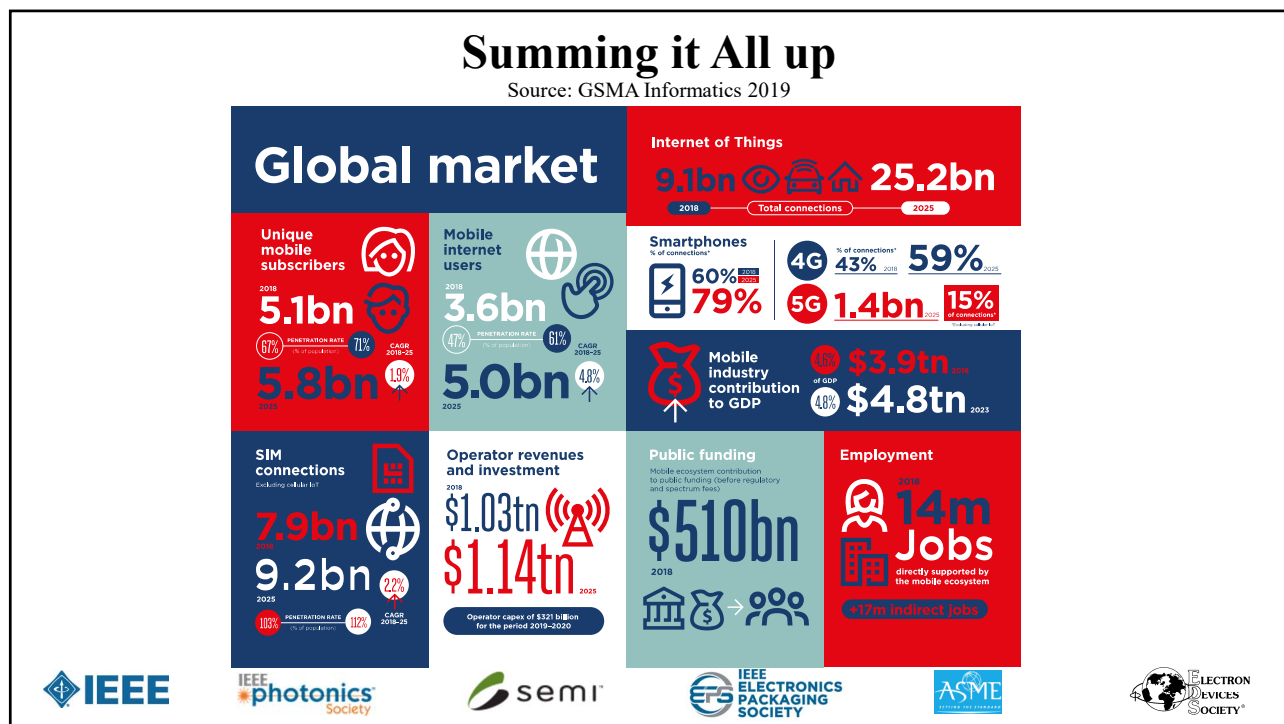
Global smartphone adoption will reach 80% by 2025

Smartphone connections as a percentage of total mobile connections

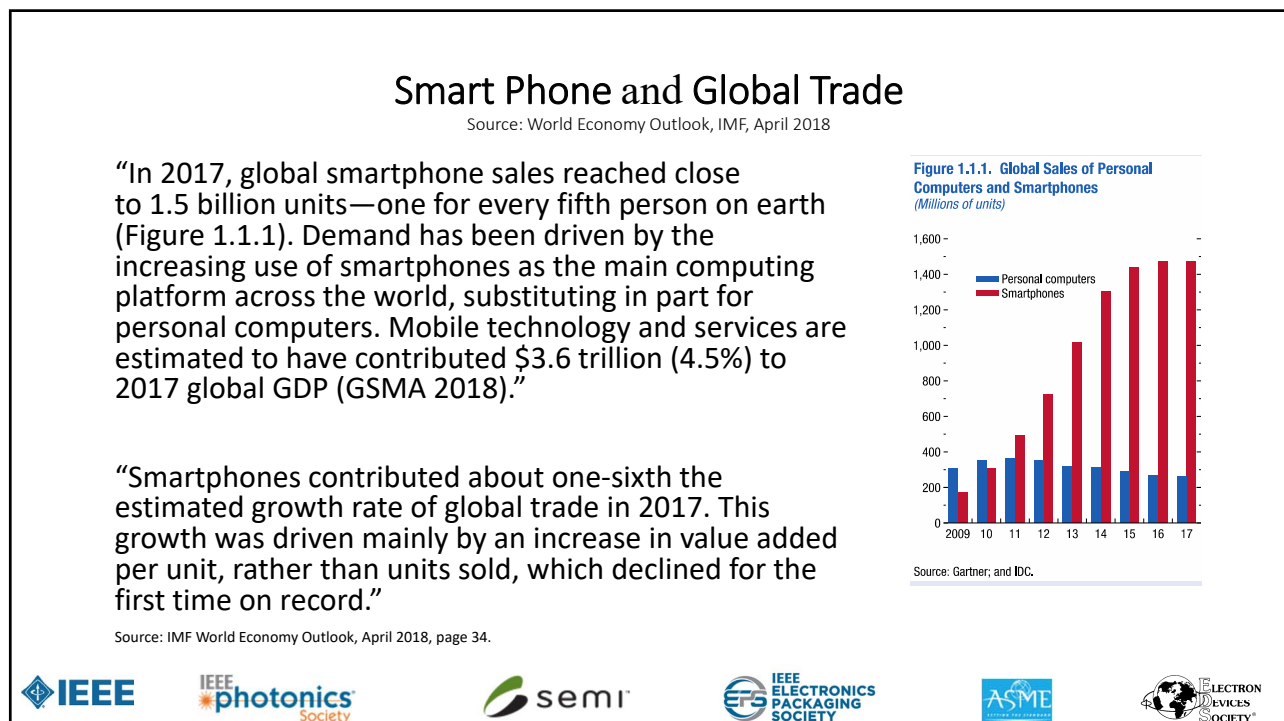


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## Inside the Mobile Phone



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## Mobile 1926

The idea for people to communicate freely anywhere untethered has existed long ago. Shown to the right is a cartoon “wireless telephony” from artist Karl Arnold published in the German magazine *Simplicissimus* in 1926.

Source: Wikipedia – History of Mobile Phone



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## Smart Phone

- The smart phone is the major human-machine interface device, with its 5bn units installed base.
- More functions and intelligence added to interact with human, machine and environment around the world
- It is the platform for most advanced nodes and innovations to meet the consumers “unfulfilled” needs.



From L to R : Apple iPhone XS Max, Samsung Galaxy S9+, Huawei 20 Pro

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## Smart Devices (Phone) (1)

The Smartphone is the “one device” for human to human and human to machine interfacing. It is a “society-transforming technology” that implemented a confluence of functions in addition to telephony – internet and web access including web browsing, search, GPS map, touch screen, large display, adequate battery life, and expanding Apps

By adding new functions (such as face recognition) on a regular basis from generation to generation, the manufacturers build in the upgrade cycle for consumer buyers. In addition to electronics there are mechanical, thermal and operating design requirements including the toughened glass required for touch screens and lithium ion battery for sufficient battery life.



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## Smart Devices (Phone) (2)

Smartphones today can have from 10 to 24 devices packaged as SiP. SiP counts above 20 may be found in flagship smartphones, with 24 being found in the early iterations of 5G phones. The SiPs include:

- 2 and 5 Camera Modules
- 1-2 Optical Sensors (from simple proximity to full facial recognition)
- At least 3 MEMs Sensors (accelerator, gyro, pressure)
- 1-2 stacked Memory Packages with controller
- 1-4 Power Amplifier Modules
- 1-3 switch filter modules
- WLAN/Bluetooth Module
- Power Management
- PoP – Application Processor & baseband processor
- Antenna Module - Antenna-In-Package (AiP) for 5G phones

As the phone continue to add more functions to meet market demands, the use of SiPs continue to increase.



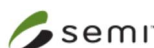
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## Heterogeneous Integration through SiP

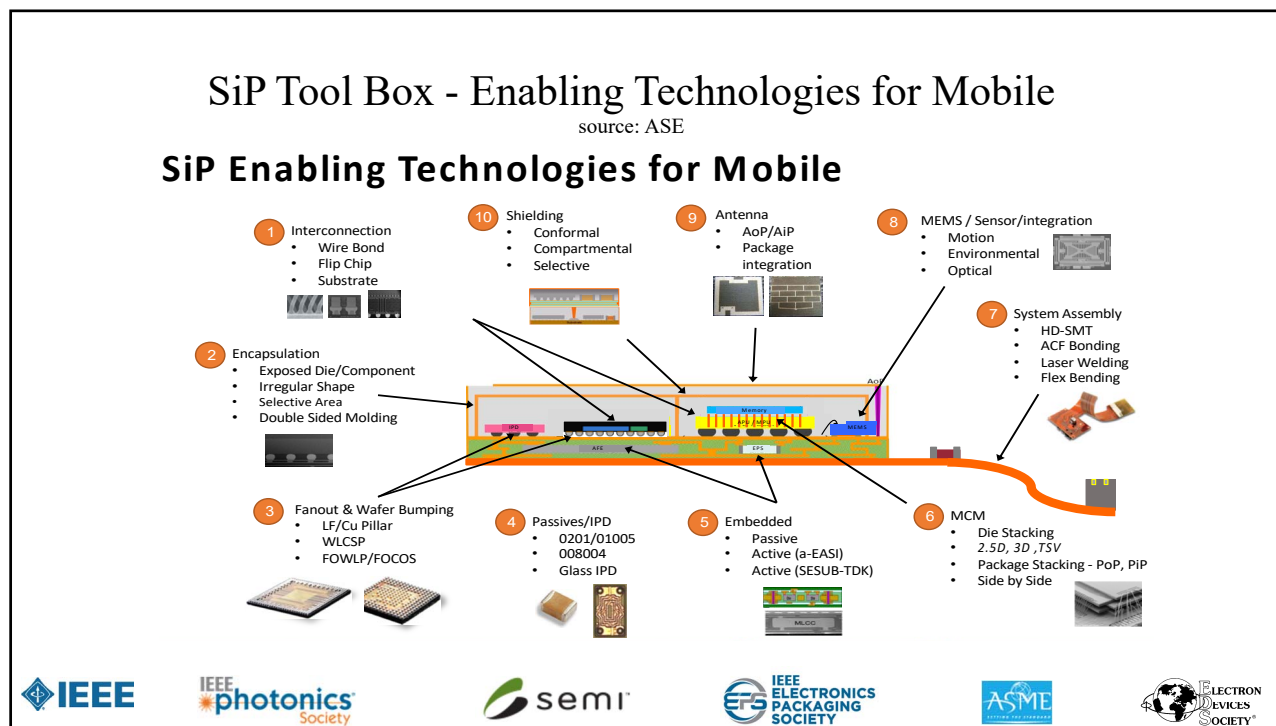
- In Gordon E. Moore's famous Moore's Law paper he said "It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically."

Source, "Cramming More Components onto Integrated Circuits," *Electronics*, pp. 114–117, 19 April 1965.

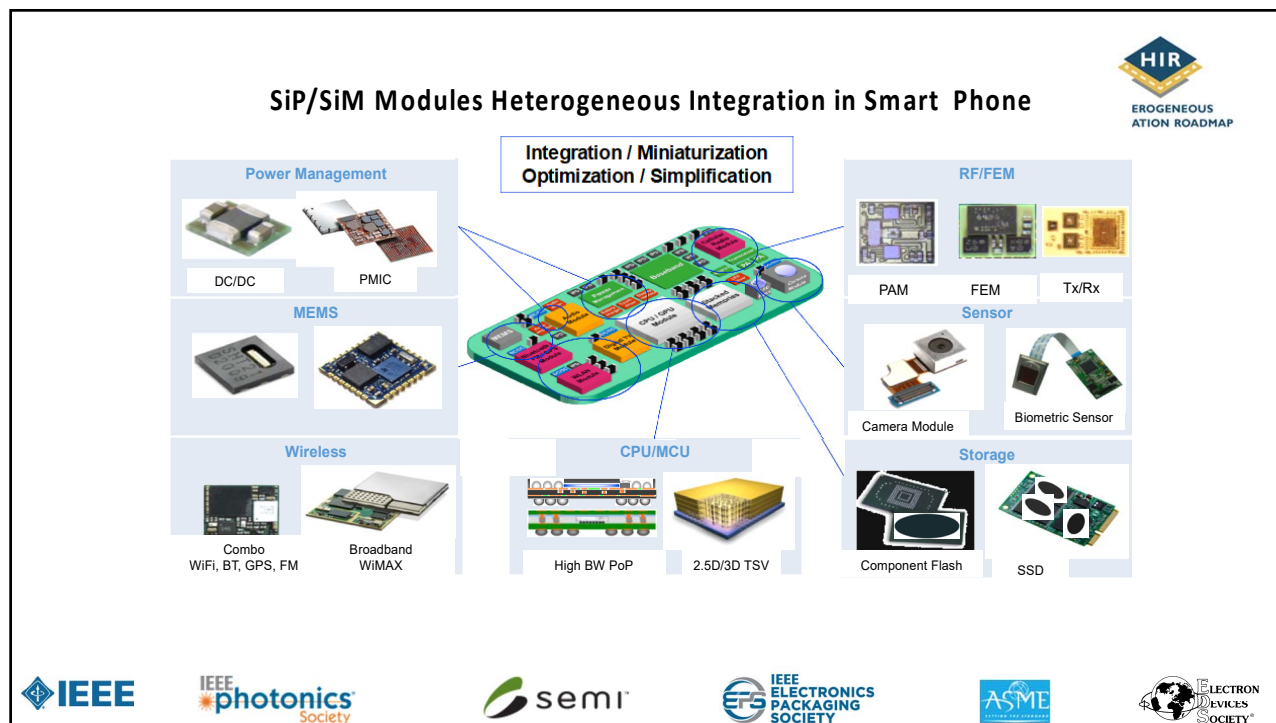
- We may paraphrase his words as follows: "It may prove to be more economical to build large systems out of smaller functions through **Heterogeneous Integration into SiPs & Modules**, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically."



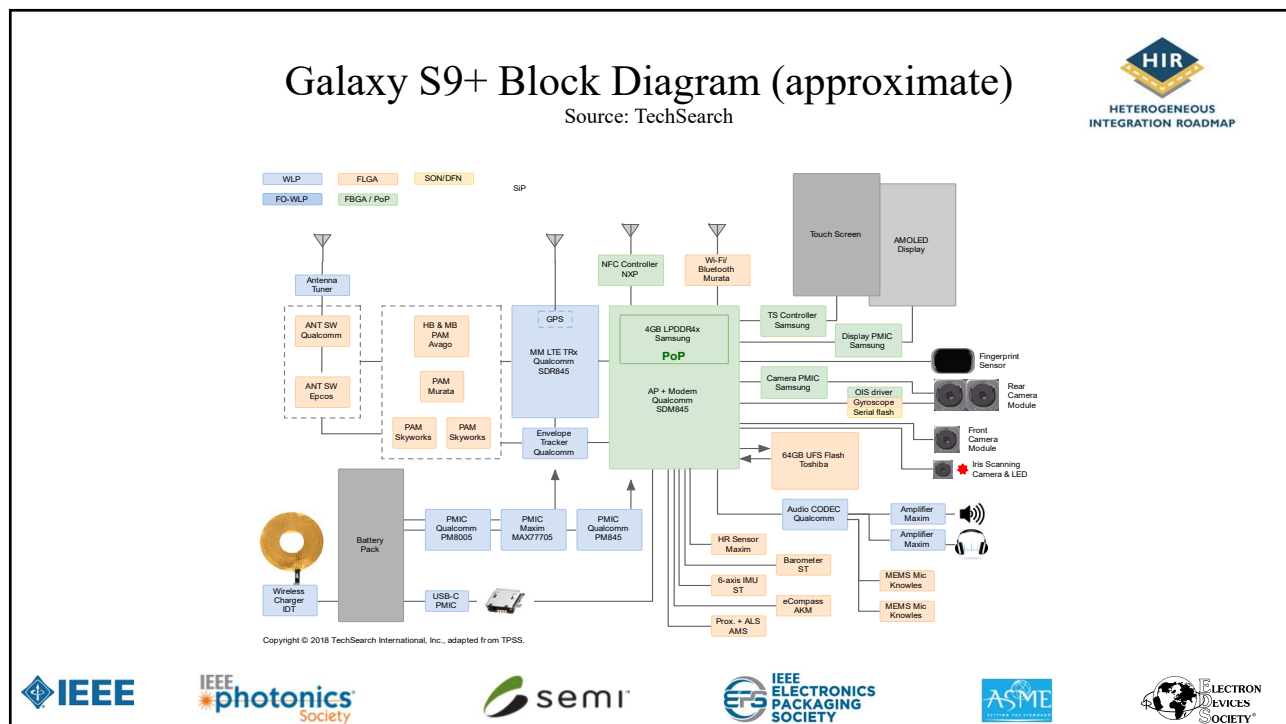
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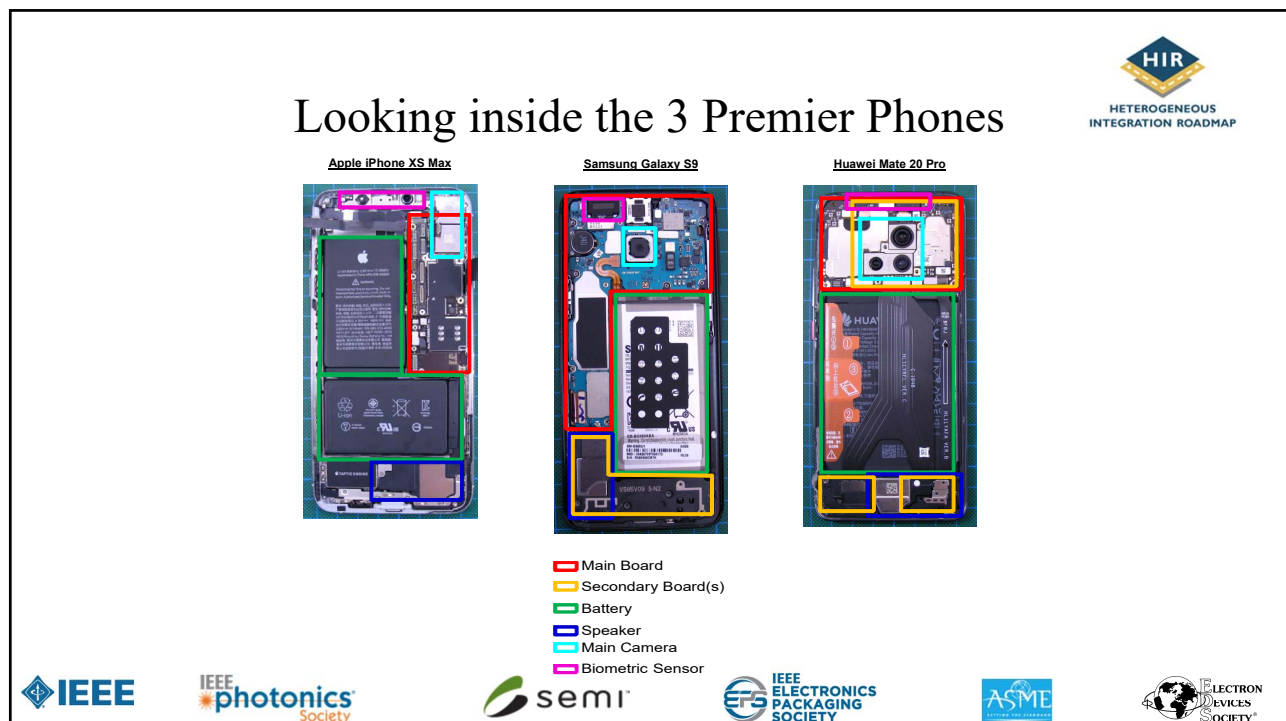
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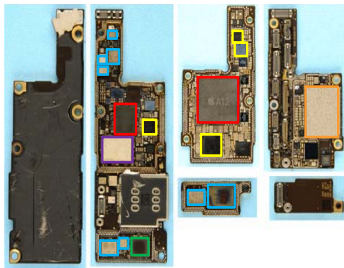


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## Main Boards Layout of three Premier Phones

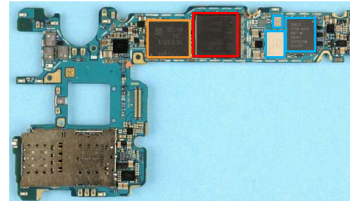
Apple iPhone XS Max



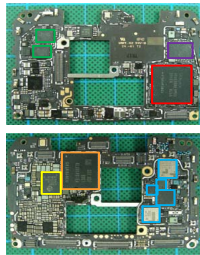
### Main Boards Layout

Source: Prismark

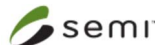
Samsung GalaxyS9



Huawei Mate 20 Pro



- APP/BBP/DDR
- Flash Memory
- PMIC
- RF TRX
- RF FEM
- WiFi



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## SiP/SiM Module in iPhone 8 Main Board Assembly



Device Advanced Node – 10 nm

10 nm Processor/DRAM

**FAN OUT SiP** 1  
**SiP** 8  
**WLP (WLCSP)** 11  
**Memory Stacked Die** 2

Teardowns of APPLE XSMax,  
 Samsung Galaxy S9+ and Huawei  
 20 Pro all show similar adoption  
 of leading edge Heterogeneous  
 Integration

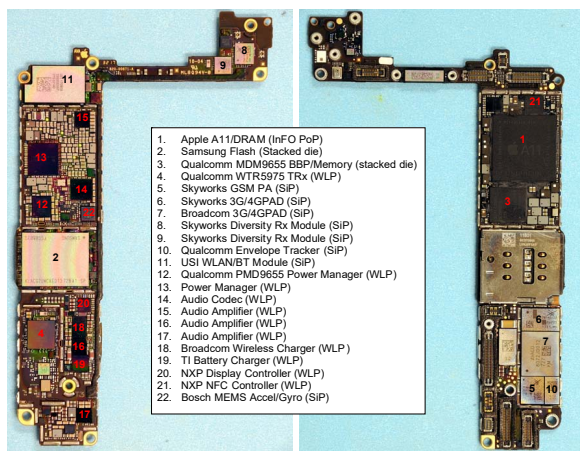
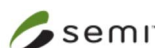


Photo source: Prismark/Binghamton University



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## Packaging for the Application Processor (AP)



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## Stacked Die Packaging for Application Processor and Baseband Processor

For application processors, there are three major stacked SiP in volume production:

- Stacked-Die-in-Package
- Package-on-Package (PoP) based upon Flip Chip CSP
- PoP based upon FO-WLP Fan-Out Wafer Level Package (FO-WLP) or Panel Level Fan-Out (PLP)

The first two utilize mature assembly and materials/tools and are widely practiced; Apple has been the single user of the wafer fan-out approach for application processors. Recently, Samsung has released a smart watch processor using a form of PanelLevel Fanout Package.

Stacked-Die is widely used for memory packaging, accounting for 90% of the stacked die products. See "Advances in Memory Die Stacking" ECTC 2018, by Andreas Marte et al



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## Stacked-Die-in-Package

Shown below is an example of stacked die in package with a processor die packaged in FCCSP format as the bottom package. FCCSP offers a lower profile, better electrical performance, and higher I/O than a conventional wire bond CSP package. The Intel baseband processor found in the iPhone XS is packaged in a 8x9mm FCCSP with a three-layer embedded trace-substrate [ETS]. Source: Prismark & Binghamton University

INTEL BASEBAND IN IPHONE XS

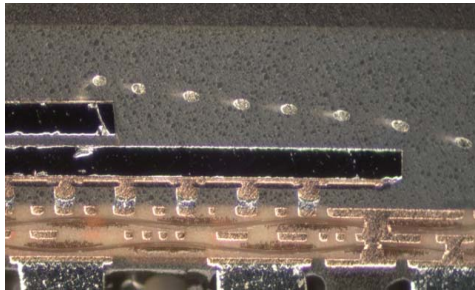


Photo Source: Prismark/Binghamton University

8 x 9mm FCCSP

- 580 $\mu$ m thick
- 0.4mm pitch

3L ETS substrate

- 30 $\mu$ m thick
- 20  $\mu$ m L/S

Processor is 75 $\mu$ m thick

- 115 $\mu$ m pitch Cu bump
- Molded underfill

Stacked DRAM wire bonded

- 75 $\mu$ m thick die
- 20 $\mu$ m Die attach film



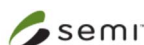
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## Package-on-Package (PoP) (1)

Package-on-Package (PoP) is described in Wikipedia as “an integrated circuit packaging method to combine vertically discrete logic and memory ball grid array (BGA) packages. Two or more packages are installed atop each other, i.e. stacked, with a standard interface to route signals between them. This allows higher component density in devices, such as mobile phones, personal digital assistant (PDA), and digital cameras.” Source: Wikipedia

PoP solutions are commonly used in baseband and applications processors in mobile phones. High-end phones have seen the fastest adoption of PoP packaging to provide high I/O and performance requirements. The main advantage of stacked PoP is that devices can be separately fully tested before assembly.

PoP are used in many high-end phones. This market is expected to continue at around 800M units per year. Apple, Qualcomm, Samsung, Huawei, and MediaTek remain the largest users of PoP, and many others are in volume production.



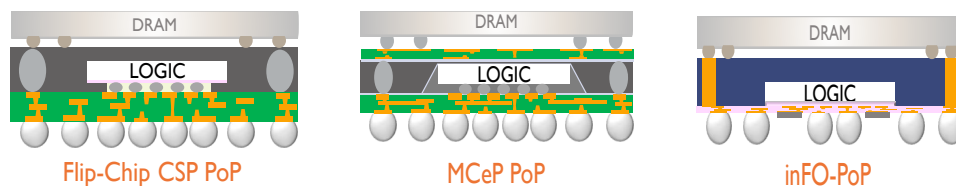
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## Package-on-Package (PoP) (2)

The three schematic figures below are three different types of PoP Packages in production today in smart phones, tablets and smart watches.

To the left is the Flip Chip CSP PoP with the Logic Die (Application Processor or Baseband) assembled on a substrate in the form of FCCSP. The middle figure with an additional substrate to accommodate additional I/O from HBW memory packages represents the MCeP PoP. To the right is the Fan Out PoP used by TSMC InFO wafer level technology for the Apple Smart Phone and Smart Watches and by Samsung Panel Level technology for Samsung Smart Watches.

Source: The 3 figures below are taken from Yole Development Report "Fanout Packaging 2019 Technology & Market Trends"



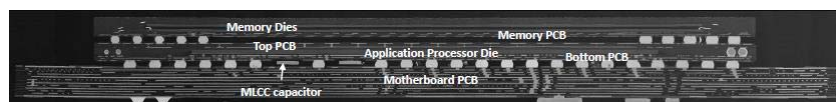
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## Examples of three types of PoP

Source Yole Report



*Example of Flip-chip package for APE- Exynos 8 APE in Samsung Galaxy S7*  
Source: System Plus Consulting APE comparison report



*Example of MCeP package for APE- Qualcomm's Snapdragon 820 APE in Samsung Galaxy S7*  
Source: System Plus Consulting APE comparison report



*Example of Fan-Out package for APE- Apple's A11 APE in iPhone 8*  
Source: System Plus Consulting APE comparison report

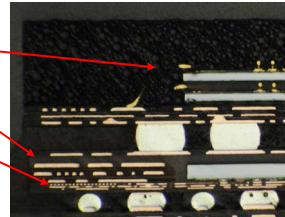


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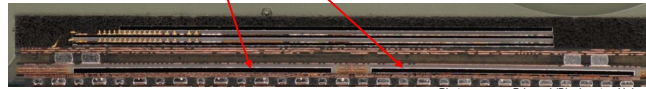
## Samsung Smart Watch Tear Down Application Processor in Panel Level Fan Out

Source Prismark Partners and Binghamton University

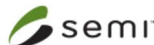
- 8 x 9.5mm PLP / PoP Package
  - 1.0mm height
- Top package is memory "ePoP"
  - 2 DRAM, 2 NAND, 1 controller
  - 3L substrate, 90µm thick
  - Underfill between packages
- Processor/PMIC die embedded in 4L substrate
- 4L RDL for high density routing
- Processor / PMIC side by side



Photos source: Prismark/Binghamton University



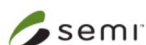
Photos source: Prismark/Binghamton University



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## PoP Summary

- PoP is the dominant solution for mobile processors and memory packaging, trading off space constraint and cost and performance.
- Apple AP has chosen the Fanout technology for its AP and memory packaging.
- Samsung has chosen Panel level Fanout for its smart watch.
- In the examples for Samsung Galaxy S7, the Exynos 8 AP and the Qualcomm Snapdragon 820 AP selected two different FC CSP PoP solutions.
- With 800 million units shipped annually, and a good knowledge base and manufacturing capacity across the industry, innovations will continue to bubble up for this dynamic market.
- Different forms of PoP FO are being developed per conference presentations.
- Will processor and memory evolve in vertical stacking (as in PoP) or in side-by-side configurations? Will there be some hybrid format emerging?

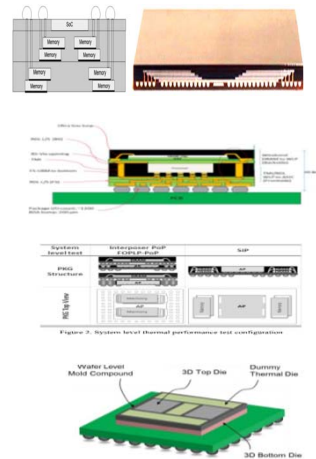


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## PoP Development Trends

Examples of innovation and research in PoP-like architecture, process materials and manufacturing:

- “3D MiM (MUST-in-MUST) for advanced System Integration.” Au-Jhih Su et al (TSMC) ECTC 2019 and “3D Heterogeneous Integration with Multiple Stacking Fanout Package” Feng Cheng Hsu et al (TSMC) ECTC 2018.
- “Ultra thin FO Package-on-Package for Mobile Application” Hsiang-Yao Hsiao et al (IME) ECTC 2019.
- “Study of Advanced Fan Out Package for Mobile Applications” Taejoo Hwang et al (Samsung) ECTC 2018.
- “Die-to-Wafer (D2W) Processing and Reliability for 3D Packaging of Advanced Node Logic” Luke England (GF) & Ping-Jui Kuo (ASE) et al ECTC 2019
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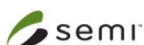


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## Premier Phone Teardowns

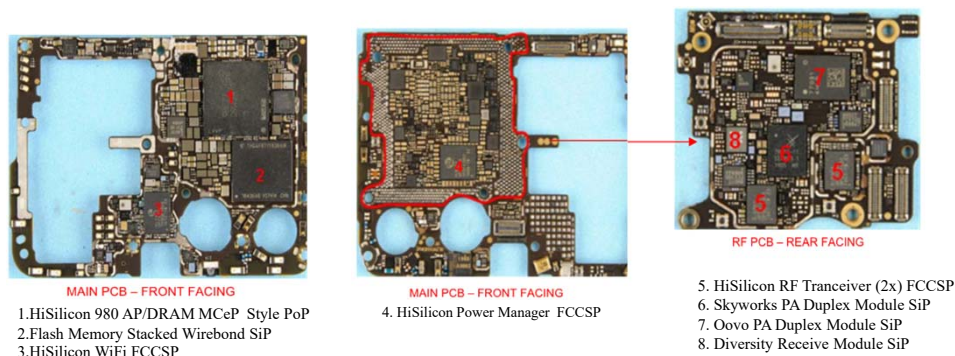
### Huawei P30 Pro

### Samsung Galaxy S10 mmWave 5G

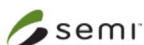


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## Huawei P30 Pro Tear-Down Source Prismark and Binghamton University

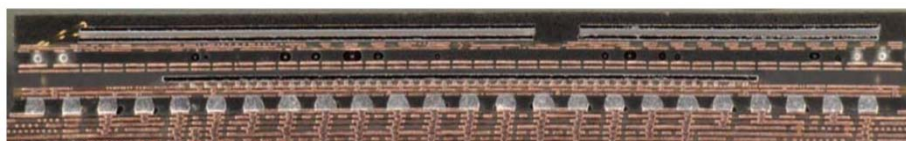


Shown above is the Huawei Pro30 Main Board Layout. Note the abundance of SiPs & FCCSPs



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## Huawei P30 Pro Tear-Down Source Prismark and Binghamton University



Above is the HiSilicon Kirin 980 in MCeP style PoP package with 1 mm mounted height. This remains the most common PoP configuration for advanced Smart Phones.

The top packages are memory LPDDR4X with four die 60 um thick using gold wirebond 3L substrate 70 mm thick

The bottom application processor die, 75 um thick, has copper pillar bumps at 120 um pitch with capillary underfill. 2L upper substrate is 110 um thick, and 3L mSAP substrate is 115 um thick, 15 um L/S.

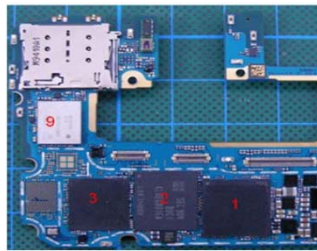


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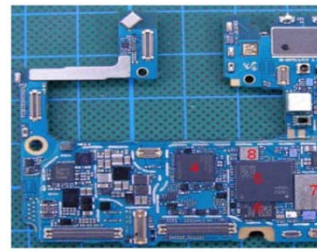


## Samsung Galaxy S10 mmWave 5G (1)

Samsung S10 5G is first to the market with 5G mmWave. Most of the components are the same with addition of 5G baseband component, additional RF module and the antenna/tranceiver modules (which will be shown later) .



- 1.QCOM 855 AP//DRAM: FCCSP PoP
- 2.Samsung UFS NAND: Wire bond stacked CSP
- 3.QCOM 5G Baseband: FCCSP/wire bond DRAM
- 4.QCOM RF Transceiver : FCCSP



- 5.Qorvo PAD: SiP
- 6.Qorvo PA: SiP
- 7.Skyworks PAD: SiP
- 8.Skyworks 2G PA: SiP
- 9.Murata WiFi/BT: SiP



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## Samsung Galaxy S10 mmWave 5G (2)

The application processor uses MCeP style PoP structure for the Qualcomm Snapdragon 855 application processor. The twin wirebond memory packages are mounted over the lower application processor, which was flip-chip mounted over 3 layer Embedded Trace Substrate (ETS) 10 um L/S. The application processor die with Cu pillar 25 um height and 100 um pitch is thermal compression bonded over NCF underfill.

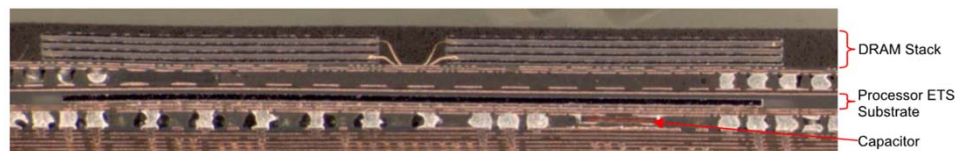


Photo source: Prismark/Binghamton University

- 12.3 x 12.4mm MCeP® style PoP
- 1.3mm height, with 4 die DRAM stack
  - Reduced substrate thicknesses
- Samsung LPDDR4X with 8 (1GB) Die
- Gold wire bonds
  - Die: 50µm thick; FOW: 50µm
  - 120µm EMC thickness over die

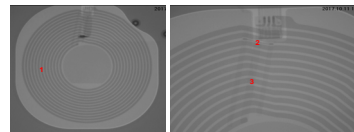
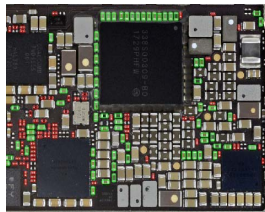
- Processor Package
- 100µm thick die; 25µm Cu bump height
  - TCB with NCP at <100µm pitch
  - 4 capacitors (0402) between bottom solder balls
  - 2L "Upper substrate": 100µm thick
  - 3L Embedded Trace Substrate (ETS); 130µm thick, 10µm L/S, 55µm via diameter



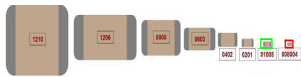
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## Leading Edge Materials and Technologies Implementation as seen in recent smart phones (Apple iPhone 8)

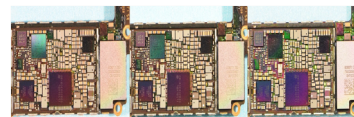
Source: Prismark Partners October 2017



Wireless Charging Coils



About 1000 Passives:  
smallest 01005



Nano Coating Material

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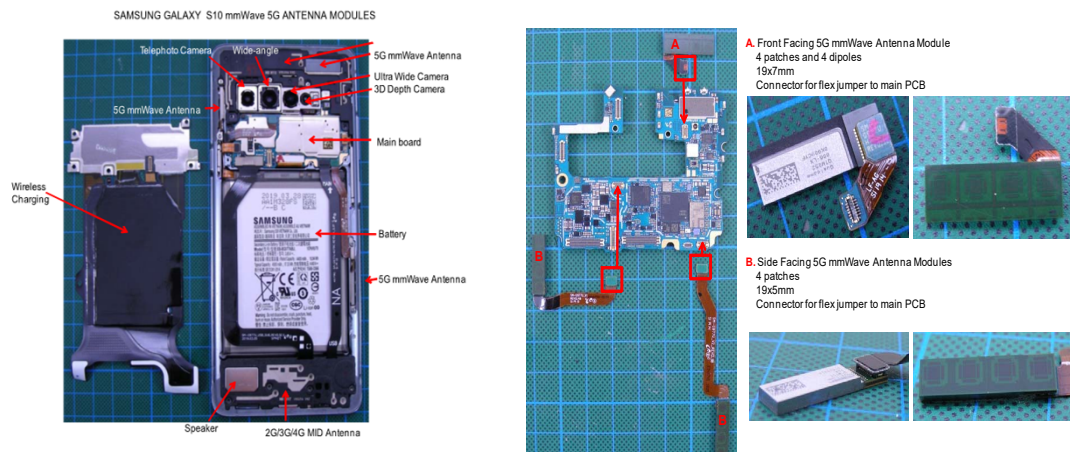
## Navigating 5G Challenges Innovations & Collaborations



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## Antenna Module in Samsung Galaxy S10 mmWave (3)

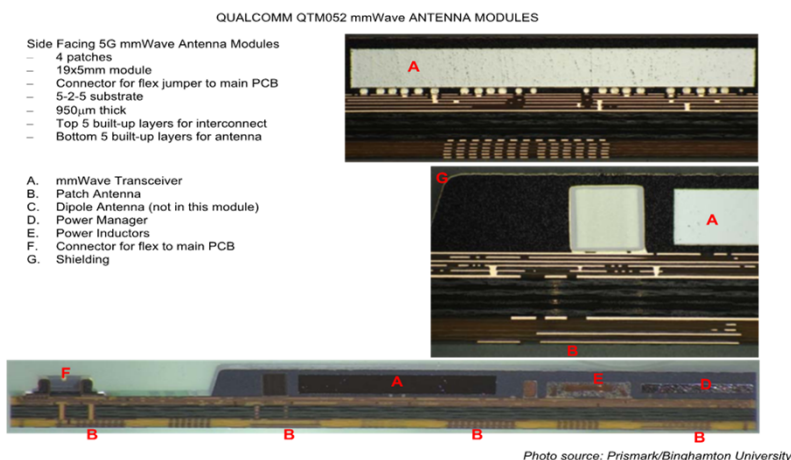
Source: Prismark Partners



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## Qualcomm QTM 052 Antenna Module

Source: Prismark Partners



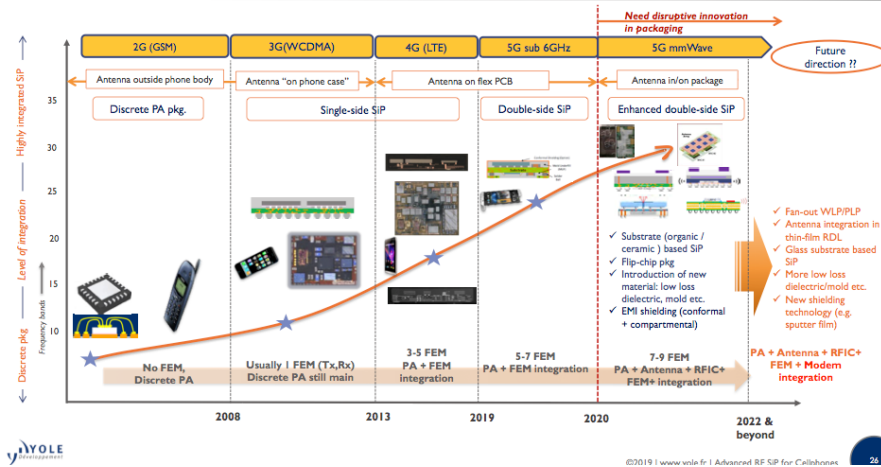
42



## Mobile Front End Module Trend

Source: Yole

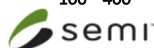
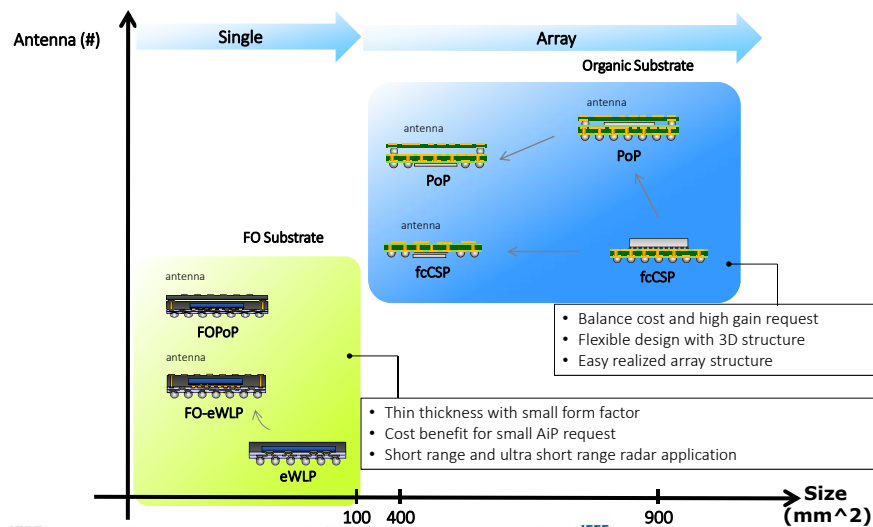
### MOBILE RF FEM PACKAGE TREND



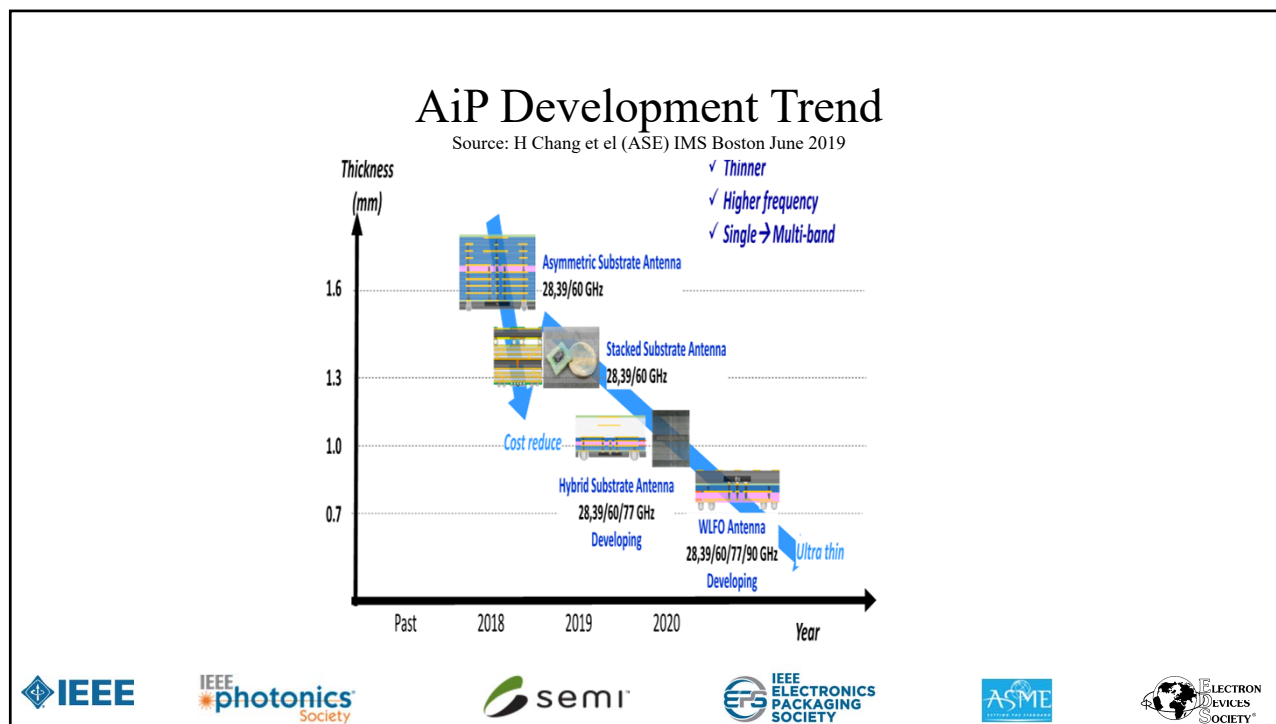
43

## Antenna in Package Evolution

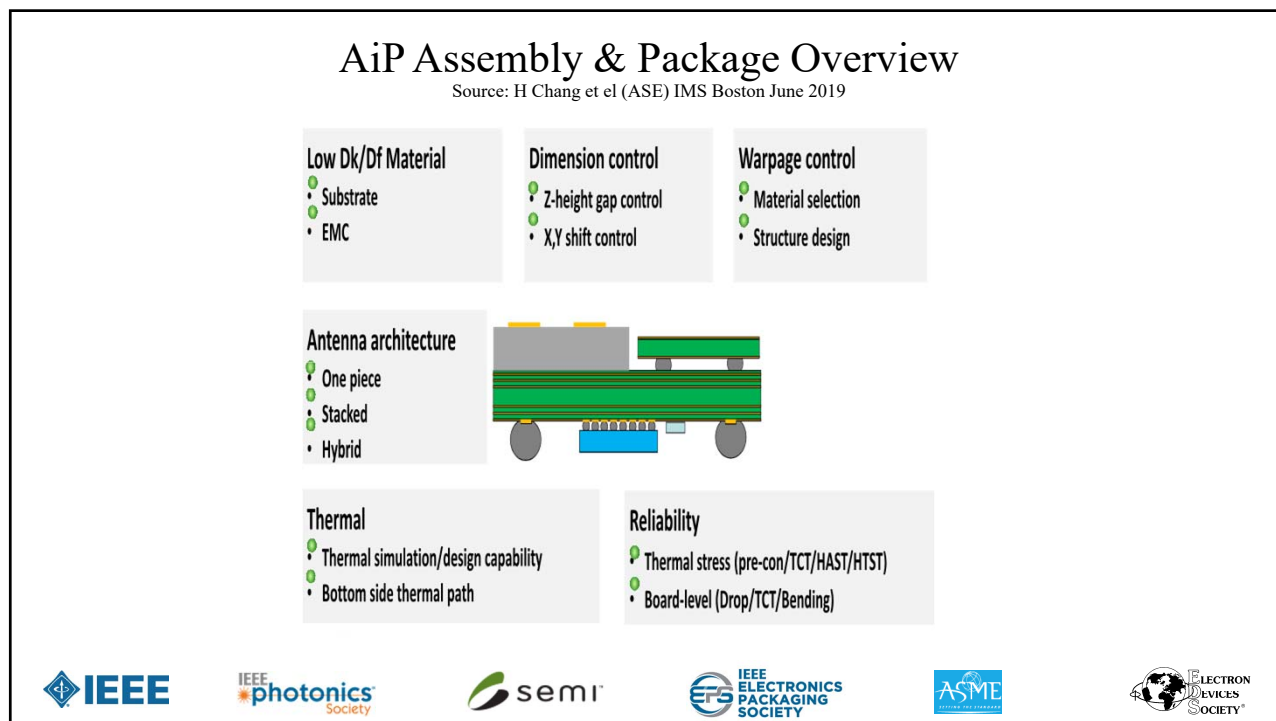
Source: Sheng-chi Hsieh (ASE) ECTC 2019



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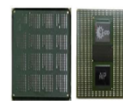
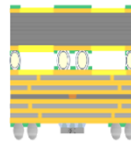
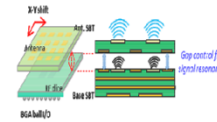
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## AiP Substrate Stacking

Source: H Chang et al (ASE) IMS Boston June 2019

### Typical

- Frequency : 28, 39, 60GHz
- Package size: 11x11mm ~ 44x56 mm
- Technology
  - High accuracy alignment stacking
- Stacking capability
  - Gap control: +/-30um, CPK>1.33
  - X/Y shift: +/-30um, CPK>1.33



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## Some Recent Technical Papers

- “InFO\_AiP Technology for High Performance and compact 5G Millimeter Wave System”, CT Wang et al (TSMC) ECTC 2018
- “Advanced Thin-Profile Fan-Out with Beamforming Verification for 5G Wideband Antenna”, Sheng-Chi Hsieh et al (ASE) ECTC 2019
- “Low-Loss Additively-Deposited Ultra-Short Copper-Paste Interconnections in 3D Antenna-Integrated Packages for 5G and IoT Applications”, Atom O Watanabe (GIT), Nabuo Oqura (Nagase) et al, ECTC 2019
- “Novel Multicore PCB and Substrate Solutions for Ultra Broadband Dual Polarized Antennas for 5G Millimeter Wave Covering 28GHz & 39GHz range” Trang Thai et al (Intel), ECTC 2019
- “Mm-Wave Antenna in Package (AiP) Design Applied to 5th Generation (5G) Cellular User Equipment Using Unbalanced Substrate” Ying-Wei Lu et al, ECTC 2018

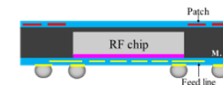


Figure 1. InFO\_AiP structure

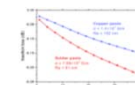
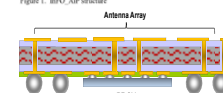
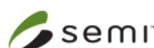
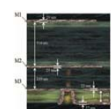


Figure 3. Frontside view of the fully assembled microwave antenna module (covering the antenna patches)

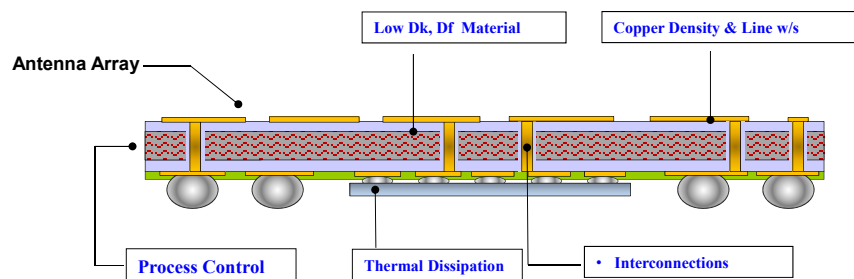


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## Antenna Design Requirements

Source: Sheng-chi Hsieh (ASE) ECTC 2019

- Design for robust Beamforming and Directivity
- Shrink interconnections between die and antenna
- Low-loss and low-dielectric constant material
- Highly accurate process control
- Thermal dissipation design, materials and processes
- Design for Test



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## Mobile/Smart Phone: A Driving Force for Innovation

- As the dominant human-machine interface, Smart Phone, tablets and smart watches connected to high speed networks and the cloud will lead the industry in diverse applications in medical and health, industry IOT, finance, education and other fields that we cannot yet imagine.
- Smart Phones are made up of SiP/SiM Modules, leading the way for the continued innovation, sophistication, and implementation of Heterogeneous Integration Technologies across broader electronic applications.
- Smart Phone will be the platform driving and launching innovative technologies – 5G, AR, VR & AI – that will propel innovation and the proliferation of electronics in our world for many years to come.
- The Heterogeneous Integration Roadmap will play a significant role in bringing the ecosystem together to foster the spirit of innovation and collaboration.



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## Network & Data Center System Packaging



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## Heterogeneous Integration for Mobile Networks

*(see Chapter 2)*

Heterogeneous Integration for Mobile Network Systems is covered in the High Performance Computing and Data Center Chapter. We have “borrowed” a few slides from that chapter to give a high-level view of the drivers, challenges and potential solutions.

We recommend that readers access that chapter’s full discourse on that topic.

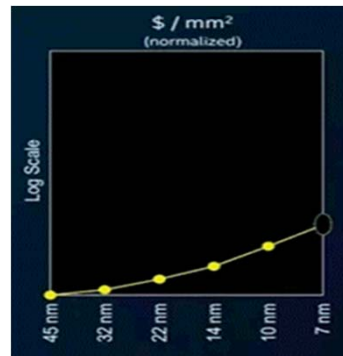


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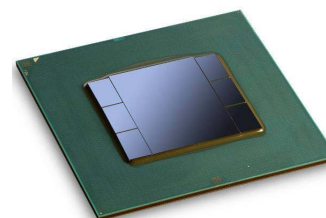
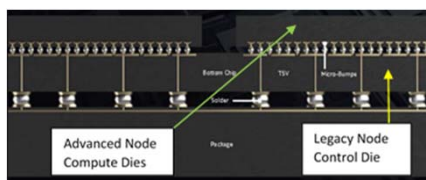
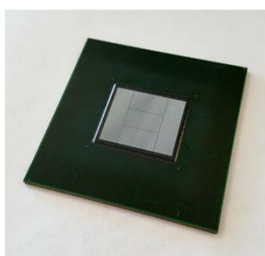
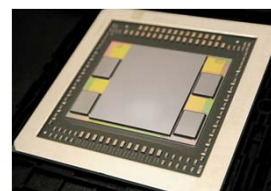
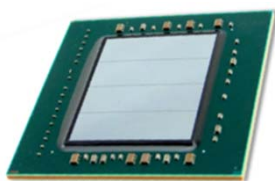
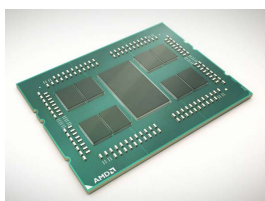
## Drivers for Heterogeneous Integration in the HPC/DC Segment

Source : K Ghose HIR HPC Data Center TWG

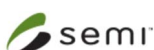
- **Die cost per unit area increasing** with node shrinks and refinements (hypernodes)
- **Package IO, latency/BW and power** constraining single-die substrates
  - **It's all about moving data!**
  - **Memory access bottlenecks limit single-chip solutions**
- **Emerging applications demand domain-specific accelerators**
  - Analytics/Intelligence on demand
  - Big data processing
  - IoTs
  - Blockchain processing
- **Emerging processing paradigms, devices**



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Source : K Ghose HIR HPC Data Center TWG

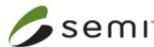


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## Heterogeneous Integration Challenge Areas

Source : K Ghose HIR HPC Data Center TWG

- On-package interconnections
- Off-package interconnections
- Signal integrity and distribution needs
- Power distribution and regulation
- SiP-level global power management
- Security and reliability issues
- Design and Test tools
- Supply chain



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## Potential Solutions: A 60,000 feet View

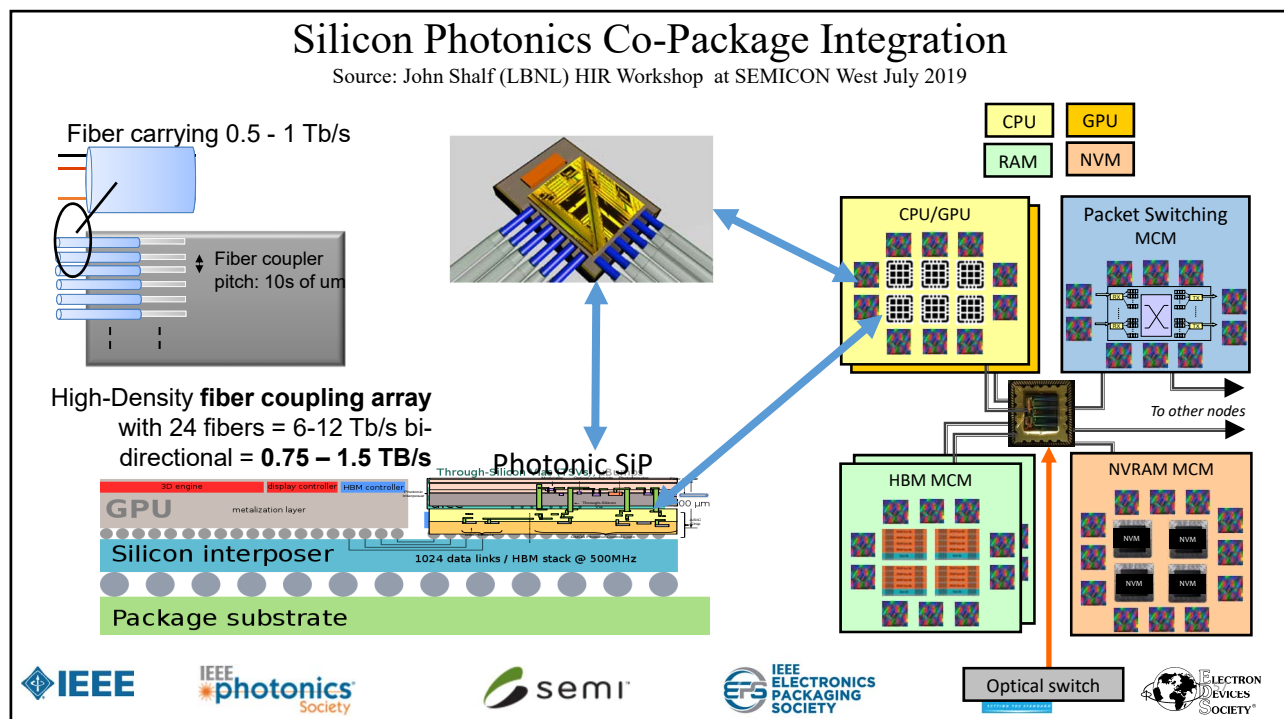
Source : K Ghose HIR HPC Data Center TWG

- Integration of accelerators, general-purpose processors, stacked memory (HBM, Stacked SRAM, MRAM) using 2.5D and/or 3D integration
  - Includes tessellated/tiled realization of computing chiplets
- Wide, short connections among chiplets (Silicon bridges, vias), in-package photonics for IO
- Aggressive signal encoding at all levels – intra-package, I/O
- Aggressive solutions for thermal management and cooling
  - SiP-level global power management
  - Thermal vias, dummy die with micropillars, conformal lids, water cooling, 2-phase cooling,...
- High-voltage power supply to package and package-internal distributed conversion to chip-level voltages
- System level tools for design and optimization
- Techniques for realizing secure solutions and graceful degradation
- Standards
  - CXL, ODSA, others and active interposers
- Integrated Si Photonics.... and Others

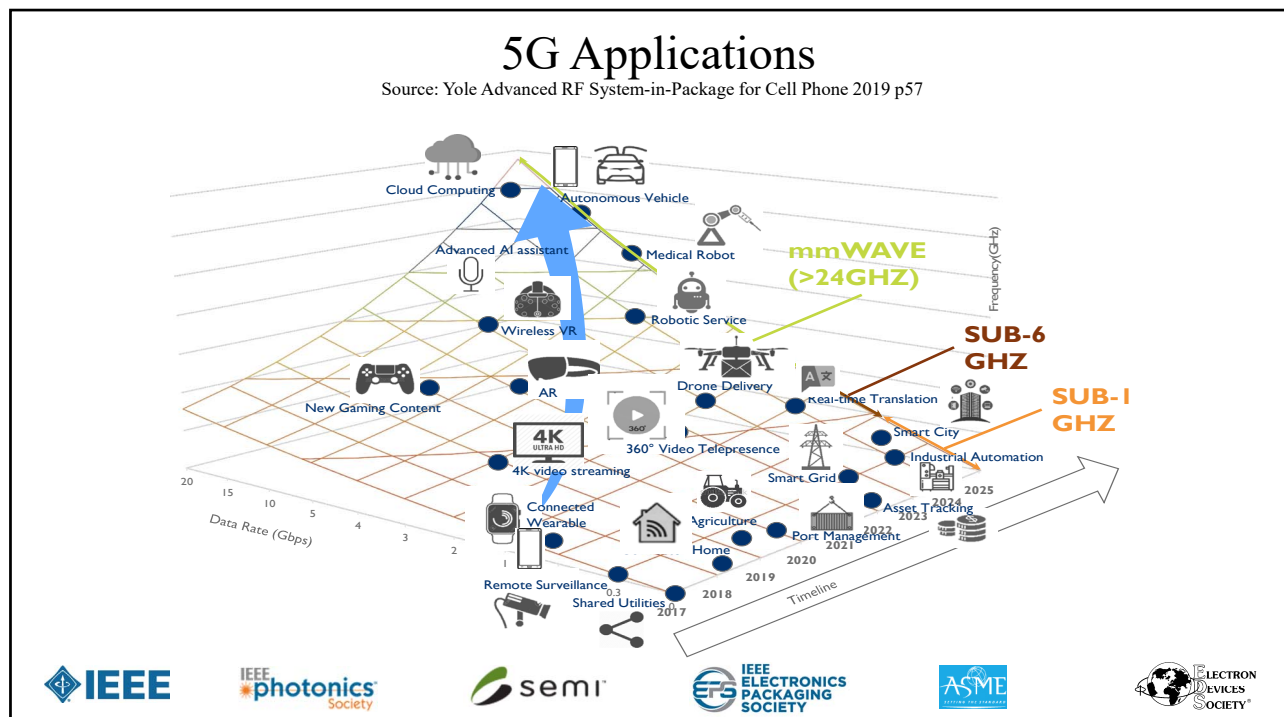


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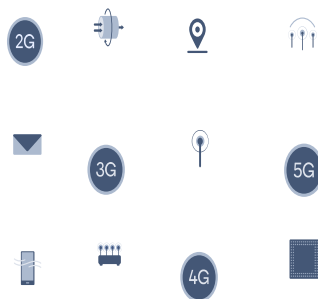


## Future Vision



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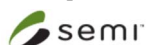
### Connectivity



### Processing



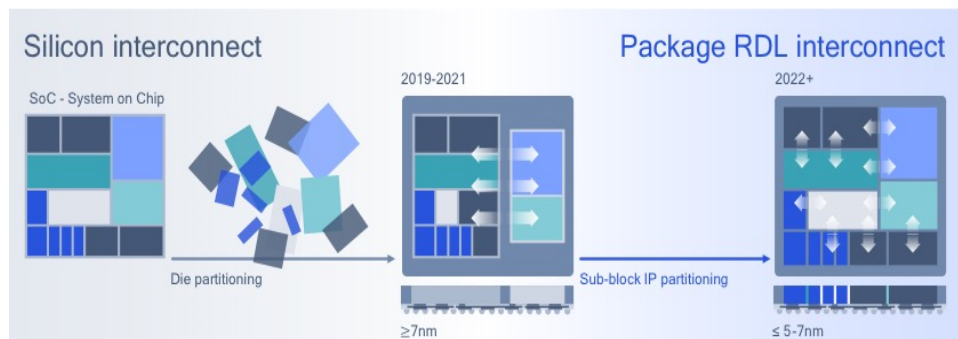
Presentation “Mobile is the Future”  
by Steve Mollenkopf Qualcomm CEO at ERI Detroit July 2019



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## Next-generation SoC design in the 5G era

Integrates with all package technologies



Presentation "Mobile is the Future"  
by Steve Mollenkopf Qualcomm CEO at ERI Detroit July 2019



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## Evolution of mobile design architectures



## Evolution of mobile form factors



Presentation "Mobile is the Future"  
by Steve Mollenkopf Qualcomm CEO at ERI Detroit July 2019




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### AI hardware acceleration research


Example: compute-in-memory AI research

- Analog compute
- New memory design
- Need low bit-width AI models




**Traditional computer architecture**

- Compute and memory are separate and data has to be shuffled back and forth
- Good for general purpose operations



**Compute-in-memory**







- Computations, like add and multiply, are done in memory
- Good for simple math operations and when memory becomes bottleneck



**A paradigm shift from traditional computer architecture can bring orders of magnitude increase in power efficiency**

\* Compared to traditional Von Neumann architectures today

Source: Presentation “Enabling the next industrial revolution with AI & 5G”  
by PR Chidi Chidambaram (Qualcomm) SEMICON West, 9 July 2019

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## The Next Big Phones Could Bring a Billion People Online

Bloomberg Business Week, 10 June 2019  
by Shira Ovide



“Two of the biggest mobile operators in Africa – MTN Group & Orange SA – this year started selling quasi smart phones for as little as \$20.” “Designed for 3G because 4G does not reach 2/3 of MTN’s 230 million customers”

“Africa has the worlds lowest share of people using internet, under 25%. The cohort of 800 million offline people spread across the continent’s 54 countries is younger and growing faster than most, but incomes are lower”.

“Boosting a poor country’s mobile internet use by 10% correlates with an average 2 percentage-point increase in gross domestic product”.

“Like energy and transportation, internet access has become an essential component of infrastructure, economic development and social empowerment”





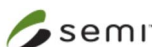



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## Challenges

### Mobile Network and Smart Devices: A Driving Force for Innovation

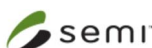
- Increased functionalities while retaining same form factor, battery life and user experiences
- Expanding affordability to broad global population: Broadband Internet access for all?
- Innovations to fulfill full potential of 5G
- Increased personal security across all phones 4G - 5G and Beyond 5G
- Synergy in 5G and Artificial Intelligence
- Global availability and sustainability



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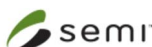
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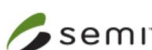
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## Acknowledgments

We wish to acknowledge with gratitude many useful discussions with many colleagues helping us to shape the structure of this Mobile chapter.

We wish to thank Patricia Macleod for her valuable advice.

We wish to acknowledge the contributions of the Paul Wesling and Denise Manning helping with the chapter completion.



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