HETEROGENEOUS INTEGRATION ROADMAP

2019 Edition

Chapter 10: Integrated Power Electronics

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I. Introduction

Heterogeneous integration (HI) is not possible without a source of power for the multiple devices and components involved. While it is possible to supply this power externally to one or more devices, it is typically advantageous to integrate the conversion and distribution of this power into the HI system. This makes power delivery one of the most critical elements in an HI system and one clearly requiring its own chapter of the roadmap.

HI provides significant advantages for power electronics as it permits wide bandgap power devices – which surpass silicon in power handling capability, efficiency, and operating temperature – to be integrated with silicon control, logic, and memory devices and with lower operating temperature passive devices. Nevertheless, HI of power electronics comes with a raft of challenges for SiP designers, as the power electronics require space, generate heat, and can cause electrical noise in the circuits. The challenges can be divided into three categories represented by the position and function of the power conversion and delivery. These three categories, which are discussed in detail below, are (1) reducing power converter size; (2) delivering power efficiently; and (3) distributing clean, high-quality power at multiple voltages ranging from 1-5 V up to 300V to multiple levels of stacked packages.

A conceptual SiP unit cell had been proposed early in the HIR study as a basis for discussion and is shown in Figure 1 with example functional die to be integrated. Characteristics outlined by the SiP Working Group (Chapter 21) are discussed in more detail. However, 10 basic electrical, thermal and mechanical metrics are identified for electrical power delivery as shown to the right of Figure 1. The selection of technologies to provide suitable performance then falls to what partition is chosen for the SiP. The possibilities for converting and delivering power are best described in Figures 2a-2d and described below.

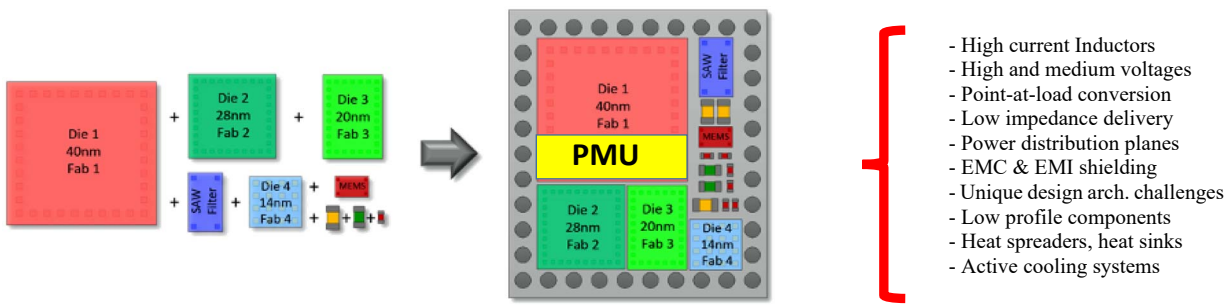


Figure 1. Basic unit cell proposed early in HIR studies for discussion.

Discrete Power Delivery

Substantial developments for highly dense discrete power conversion modules are being developed by the major power semiconductor manufacturers and power supply houses. The "point-of-load" would be located at the next level higher in packaging, e.g. board level and converter power for delivery directly to the SiP. Multiple voltages would be available for either direct supply to the SiP or delivery to other "in-package" converters as discussed in the following figures. The availability of technologies is much greater and limited by compatibility with the board-level system packaging technologies. Advantages are optimizing for low cost, high density and independent thermal management. Disadvantages are relatively higher distribution pathway impedances along with EMI problems of relatively long leads and high frequency pulsed load currents including capacitor charging/discharging. Self-contained prognostics are easier to manage in association with board-level power management.

Power in SiP Distribution

Power is converted and delivered at the system level package. The on-SiP converters bring in power from the Discrete Power supplies, and reduce and divide the power for delivery to the heterogeneously integrated subsystems. The power management can be substantially complex, delivering a multitude of buses at different voltages that allow loads to dynamically select chip power. The complex delivery system can include power monitoring, fault monitoring and control. Alternatively, the on-SiP conversion may be pass-through power to the loads and only provide power management. The power architecture of conversion and delivery would be decided by the SiP substrate designers. The converters would preferably use available SiP technologies for fabrication. The limited SiP technologies provide

fewer choices and lower power densities. However, being on-SiP allows for better power buffering for faster response and higher voltage distribution to the subsystems.

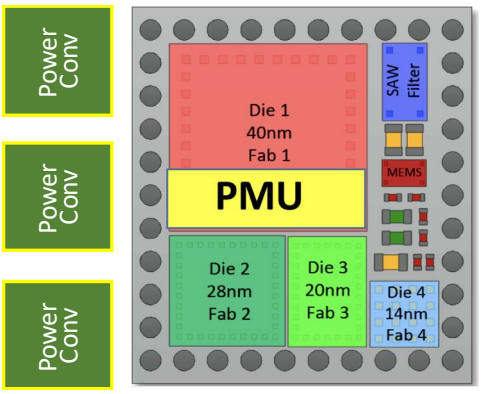


Figure 2a. ***Discrete Power****. The power conversion is provided outside the SiP substrate and delivery is provided through distribution channels*

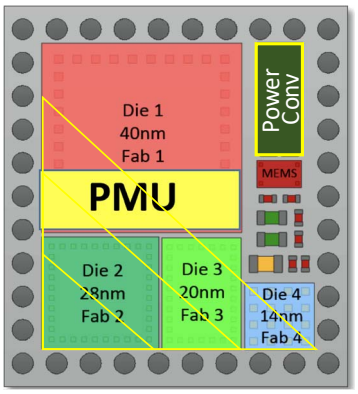


Figure 2. ***Power in SiP Distribution*** *uses SiP Pkg & Mfg technologies to distribute power from off board Discrete Power converters.*

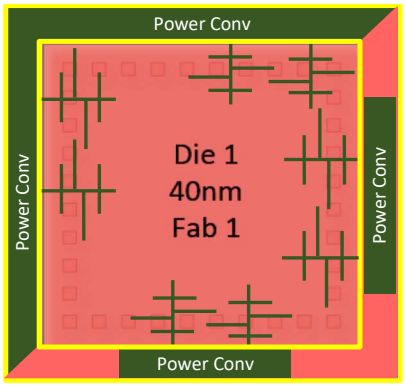


Figure 2c. ***Peripheral On-Chip Power Conversion and Distribution*** *uses the same "Component" Pkg & Mfg technologies to create power conversion at the interface with the SiP.*

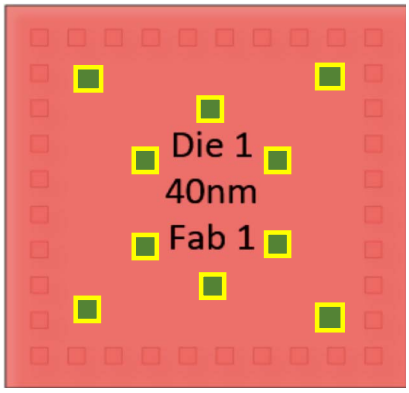


Figure 2d. ***Embedded On-Chip Power Conversion*** *uses "Component" Pkg & Mfg technologies to create local conversion and at-load distribution.*

Peripheral On-Chip Power Conversion and Distribution

This approach integrates power conversion onto the chip, to allow for voltage step-down from voltages up to 300V to ones as low as 1-5V, bringing power from the SiP distribution system onto the chip. Due to the high currents and fast responses, a combination of high voltage distribution to the chip and redistribution and conversion on-chip has high probability. Fabrication technologies would need to align closely with chip fabrication technologies, and require a new set of design skills to augment the chip-level designers. Because of the captive functionality, the power monitoring and management would be considerably less complicated, with very predictable loading by design. Again, local buffering becomes a requirement, though some off-loading of buffering could be possible at the sacrifice of low impedance and high-speed response. Thermal and mechanical management are all part of the chip designer's purview. The power supply thermal loading is typically not as high as for CPU and graphic chip processors, since the power supplies strive for very high efficiency while loads are zero-percent efficient.

Embedded On-Chip Power Conversion

The highest level of integration is Point-of-Use conversion deployed across the chip. This provides use of relatively high voltage distribution and the fastest load response, particularly combined with new capacitor technologies (e.g. trench technology). Again, a new set of design skills are required to augment the chip-level designers. Because of the high level of integration, the relative power densities may be lower since optimum power technologies may not exist, unless new technologies are developed.

Roadmap Outline

This roadmap for Power Electronics for Heterogeneous Integration will address the timeline for the development of the power conversion and distribution techniques needed to supply clean, efficient power at a variety of voltages to the wide range of devices in an HI system without significantly increasing system size. These needed advancements can be broken down into the following three main categories:

1. Reducing power converter size
2. Delivering power efficiently
3. Distributing clean, high-quality power at multiple voltages to multiple levels of stacked packages

This 2019 edition of the roadmap focuses on the first of these categories – reducing power converter size. This requires the development of wide bandgap (WBG) semiconductor devices which can convert higher levels of power more efficiently, combined with packaging technologies that can reduce the size and increase the power density of the converter circuits. Developing smaller converters is important because utilizing distributed conversion where each component is near to its power supply is critical to minimize interconnection losses and signal noise. Key areas that will be covered in the roadmap are the following:

1. Wide bandgap power electronic devices (GaN, SiC, GaO, diamond) that are thinner in size and can operate at higher frequency, higher efficiency, and higher temperature.
2. Capacitors (smaller discretes, embedded layers, embedded trench capacitors) that combine battery levels of energy storage with capacitor levels of high frequency power transfer.
3. Inductors (planar magnetic structures, new core materials, low loss internally-cooled windings).
4. Novel device interconnection approaches and materials, including stacking sequences, multifunctional (thermal and electrical) vias and busses, bumps, flip chip solders, and direct copper attach.
5. Thermal management of the power electronics, including the development of higher thermal conductivity joining materials and encapsulants, anisotropic conductive joining materials, thermal metamaterials, thermal isolation approaches, and integrated microfluidics.

The second of these categories, to be discussed in the upcoming 2020 roadmap, is delivering power efficiently. This is necessary to reduce losses and thus the need for cooling. One of the best ways to reduce the size and weight of the cooling system for power electronics and make it easier to integrate is to reduce the heat generated in the first place. Key approaches to increase the efficiency of power conversion and distribution that will be covered in the roadmap are the following:

1. Developing methods for distributed conversion. Moving power converters close to the devices to which they are supplying power reduces the length of interconnection traces, reducing parasitic losses. This requires developing new circuit topologies and size-reduction techniques from the first category.
2. Developing low resistance traces and vias that can support high voltage and current. This will also reduce parasitic interconnection loss.
3. Developing thin film, flexible dielectric interposers with high breakdown voltage to minimize leakage.
4. Designing low voltage, low capacitance switching on chip to minimize CV loss.
5. Gate driver circuitry that is smaller and more efficient.
6. Refining software for active power management.

The third of these categories, also to be discussed in the 2020 Roadmap, is distributing clean, high-quality power at multiple voltages to multiple levels of stacked packages. This requires designing the power conversion and distribution system to minimize noise and maintain signal quality. Since there will be multiple chiplets and components that will each require different levels of current and voltage, this requires a distributed conversion architecture, in which many individual power converters are located close to the components for which they are delivering power. Placing the converters close to the components not only minimizes noise, but it also reduces the power loss, by allowing high voltage at low current to be used for distribution up to the point of use. Key approaches to achieve this objective that will be covered in the roadmap are the following:

1. Developing new distribution architectures, such as placing wide bandgap power chiplets on a CMOS substrate, placing converters on the periphery of the chip, placing a separate power device on the SiP near the chip, or placing a separate package near the SiP.
2. Developing new SiP bus architectures.
3. Improving power quality and matching to minimize reflection noise.
4. Minimizing noise at high frequency.

5. Improving EMI shielding.
6. Improving filtering.
7. Minimizing switching (dI/dt and dV/dt) noise.

This roadmap will address each of these categories in the following sections. Sections will begin with a current assessment of the best practices, approaches, materials, and devices currently available. This will be followed by a discussion of where the technology needs to be in the next 5, 10 and 15 years. The needed technology developments in each area required in those time frames will be discussed along with a timeline and resources required to achieve these advancements.

Reducing Power Converter Size

Wide bandgap power electronic devices (GaN, Al(Ga)N, SiC, GaO, diamond)

The improvement in power efficiency that comes from using SiC and GaN devices is now well understood and accepted. Power losses are a combination of the following three factors: on-state loss, off-state loss, and switching loss. Increasing levels of doping decrease the on-state resistance, but also lower the breakdown strength. The higher intrinsic breakdown strength of SiC and GaN means they can be doped more highly while still maintaining the needed breakdown strength. This results in lower on-state resistance and correspondingly lower on-state Joule heating losses. The wider bandgap of SiC and GaN reduces intrinsic carrier concentration, thus lowering the reverse leakage current and reducing the already low Joule heating losses in the off-state. The higher saturation electron drift velocity of the SiC and GaN lead to faster switching speeds with lower capacitance and thus lower switching losses. These increases in efficiency reduce the power losses, so less heat needs to be removed and integrated cooling systems can be smaller. Required cooling system size is also reduced by the ability of these wide bandgap devices to operate at higher temperatures. Typically, SiC devices are chosen today for high power applications, due to their higher breakdown strength and thermal conductivity, while Al(Ga)N/GaN devices are preferred for high frequency applications.

Table I: Currently available SiC and GaN diodes

SiC Diodes	SiC MOSFET/JFET	GaN FET HEMT)
Wolfspeed	***Wolfspeed***	***EPC***
1.7kV, 50A Bare Die	1.7kV, 48A – TO247	300V, 6.3A – Die: BGA
1.7kV, 25A – TO247	1.2kV, 60A – TO247	200V, 31A – Die: LGA
650V, 50A – TO247	1.2kV, 71A – Bare Die	100 V, 90A – Die: LGA
Fairchild	***ROHM***	***GaN Systems***
1.2kV,20A – Bare Die	1.7kV,20A – TO220/TO247	650V, 60A – Die: Top-side
1.2kV, 20A – TO247/TO220	1.2kV, 95A – TO247	100V, 90A – Die: Top-side
650V, 30A – TO220	650V, 118A – TO247	100V, 90A – Die: Bottom-side
ROHM	***Microsemi***	***Transphorm***
1.7kV, 20A – TO200	1.2kV, 80A – TO247/D3PAK/SOT227	650V, 50A – TO247
Microsemi	***ST Microelectronics***	
1.7kV, 10A – TO247	1.2kV, 65A – TO247	
1.7kV, 30A – TO247	650V, 100A – TO247	
ST Microelectronics	***Infineon***	
1.2kV, 20A – TO220	1.2kV, 35A – TO247 (JFET)	
650V, 40A – TO247		
Infineon		
1.2kV, 40A – TO247		

In addition to improved efficiency, Al(Ga)N HEMT devices can operate at higher frequencies. Higher frequency operation permits the use of smaller passive components, thereby reducing overall converter size. Al(Ga)N HEMT devices are also typically grown in thin epi-layers and thus can be used with thinned wafers, reducing packaging thickness and increasing the ability to embed the GaN devices in substrates and printed wiring boards. Some of the currently available SiC and GaN diodes and transistors, and AlGaN/GaN based HEMPs, are provided in Table 1.

The main issue remaining with GaN devices is that the lack and high cost of bulk GaN material has limited the development of vertical GaN devices. As long as the use of GaN is limited to planar (HEMT) devices, the current through each device is limited. Research is currently being conducted toward developing vertical devices in epi-GaN [1,2] on heterogeneous substrates to address this issue, and it is expected that these devices will become available in the next 2-5 years. Another limitation to GaN HEMTs is the operating voltage. Currently GaN HEMT devices are available up to 650V to 900V. Research is being conducted to develop GaN HEMTs at higher voltages, with 1200V devices expected to be available in the next 2 years [3].

As SiC and GaN reach increasing levels of commercial penetration, research is now focusing on devices made from semiconductors with even larger bandgaps, such as diamond and GaO [4,5]. These ultra-wide bandgap devices promise even greater efficiencies and switching frequencies than GaN and SiC. However, they are more difficult to dope, which makes creating junctions and contacts for devices more difficult. It is anticipated that many of these new devices will be released in the next 5-10 years. As such, some of the expected developments are presented in Table II. More details are available in the International Technology Roadmap for Wide Bandgap Power Semiconductors [6].

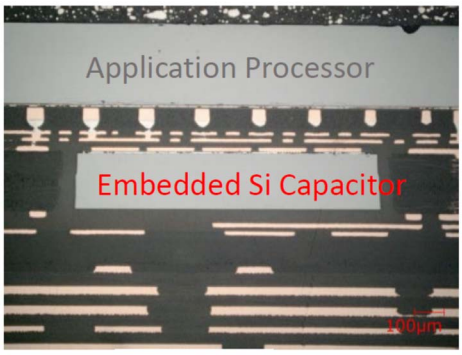
Table II – Expected Developments in GaN and SiC

	2 years	**5 years**	**10 years**	**15 years**
1200 V GaN HEMT devices	**X**			
Vertical GaN power devices	**X**	**X**		
Gallium Oxide Based Power Devices		**X**	**X**	
Diamond Based Power Devices			**X**	**X**

Capacitors

After diode and transistor switching devices, capacitors are the next most important devices in a power converter. These devices smooth the output signal from the switching devices regardless of whether the system is a DC-DC Buck Converter, a DC-DC Boost Converter, a DC-AC inverter, or and AC-DC rectifier. The size of these capacitors is a function of switching frequency, the power rating, voltage stability and output current, and the required capacitance. Higher frequencies require lower capacitance for smoothing so the devices can be reduced in size.

Capacitors essentially require thin dielectrics with sufficient permittivity along with high surface area electrodes to achieve high power densities. The dielectrics range from simple oxides to multicomponent oxides that require complex high-temperature processes. High surface area is achieved with trenches, multiple layers of stacking, or sintered particles. The details of the capacitor architectures and underlying technologies are described in Chapter 15 (Materials) of the Roadmap. Thinned silicon-based capacitors can often be embedded as discrete devices in substrates and boards, as shown in Figure 3, and smaller-value capacitors can often be embedded as layers of dielectric in between conducting layers, as shown in Figure 5. Another capacitor currently being developed [7] is the silicon-based trench capacitor, as shown in Figure 4, where the trenches are etched in the silicon, conformally coated with an oxide or oxynitride, and then coated with TiN or other counter electrodes, thus using the vertical dimension to make a number of parallel MIM capacitors of reasonably large area to increase capacitance. This concept of high surface-area electrodes with high volumetric densities is also extended from electrostatic energy storage with oxide dielectrics to electrochemical energy storage with supercapacitors and batteries. Thus, battery levels of energy storage with capacitor levels of high-frequency power transfer are supplied from wafer- or package-integrated components.



Source: LTEC Corporation

Figure 3. Embedded Discrete Silicon Capacitor

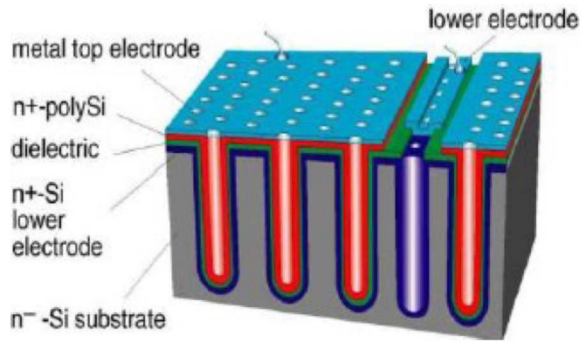
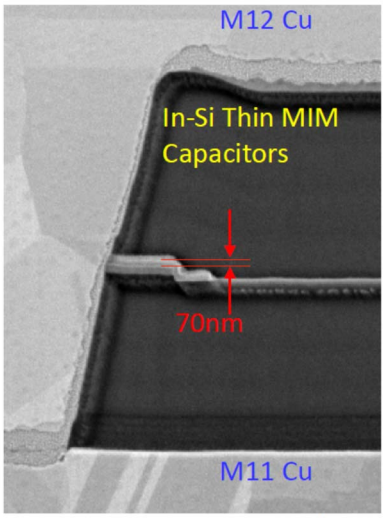


Figure 4. Silicon Trench Capacitor (courtesy of Murata Corp)



Source: LTEC Corporation

Figure 5. Embedded Capacitor Layers

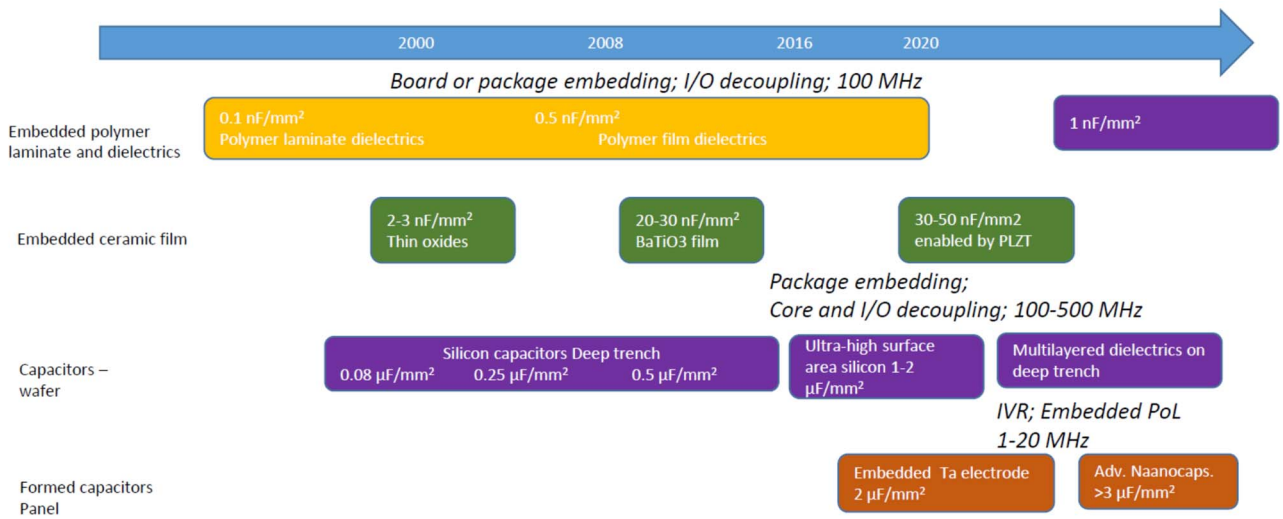
Table III shows the current state-of-the-art of commercial capacitors and Table IV outlines the needs moving forward. Electrolytic capacitors based on tantalum provide the highest capacitance densities, while MLCCs are beginning to achieve comparable densities but with lower ESR (equivalent series resistance) and smaller form-factors. MLCCs are preferred for applications that demand such lower parasitics and integration into smaller footprints. Silicon trench capacitors are emerging as alternatives to MLCCs because of their direct compatibility with wafer front-end process infrastructure and integration advances as capacitor arrays in both wafer fan-out packages and laminates. Densities of 1 microfarad/mm^2 are now reported with trench capacitors with 100-200 µm devices, making them strong candidates for wafer- or package-integrated power delivery. Companies such as TSMC and Murata are leading the trench capacitor effort while KEMET and Murata are leading the effort in thin embedded high-density electrolytic capacitors. Details are provided in Chapter 15 (Materials).

For higher voltage and current-handling, electrolytic and polymer film capacitors from companies such as KEMET, TDK, AVX and Wurth are widely used. For low resistance and higher currents, film capacitors have advantages, while electrolytic capacitors provide the highest advantage, with polypropylene as the prime candidate. Anodized tantalum for voltages up to 48 V and anodized aluminum for higher voltages are the key classes of electrolytic capacitors. The emergence of conducting polymer electrodes to replace the liquid cathode in electrolytic capacitors has resulted in much wider acceptance of these capacitors for both high density and higher frequencies, as an alternative to replace several MLCCs.

Table III. Current State-of-the Art of Commercial Capacitors

	Murata Thin MLCC	Murata Trench Caps	AVX Ta Chip	Emerging Need
Volumetric Density	20 µF/mm³	10 µF/mm³	~10 µF/mm³	20 µF/mm³
Thickness	100 µm	100 µm	600 µm	50-100 µm
Freq. Stability	10-100 MHz	>1-10 MHz	200 kHz	>1-10 MHz
ESR	~10 mΩ	50 mΩ x µF	>100 mΩ x µF	~50 mΩ x µF
% ΔC/V	-13 % to -70% (1 to 4 V)	~ 0 %	~ 0 %	~ 0 %
Max. Temp	85° C	150° C	125° C	125° C
	PICK AND PLACE			FILM EMBEDDING WAFER OR PANEL INTERCONNECTS

Table IV. Roadmap for Embedded Film Capacitors



Inductors

High-efficiency power conversion at the System on Chip (SOC – microprocessor, DSP, microcontroller) load is becoming a critical path for power delivery, as it can achieve several objectives such as higher efficiency, higher transient performance and better granularity in optimized power delivery to an increasing number of on-chip voltage domains and/or microprocessor cores. As switching regulators are the preferred topology, the role of magnetic components such as inductors is becoming more important.

The conventional solution of having a power management IC (PMIC) close to the SOC containing multiple dc-dc converters (currently up to 20) and linear regulators is becoming a footprint and performance roadblock due to the need for discrete passive components on the motherboard for each switching regulator (i.e. input and output capacitors and output inductor) as discussed in the previous section on capacitors. The output inductors are a particular pain-point because of their large footprint and height profile as well as their unit cost.

The holy-grail for SOC power management is to make the multiple PMIC passives "disappear" onto or into the SOC substrate/package (Intel FIVR 2014, Dialog Semiconductor Merckx SIP 2018) and ultimately onto the SOC itself (Ferric Semiconductor/TSMC 2017, Dialog Semiconductor 2018). These two configurations are referred to respectively as Power Supply in Package (PSiP) and Power Supply on Chip (PwrSoC). This level of miniaturisation and integration will enable a paradigm shift to granular power for SOCs or what could be referred to as a micro- or nano-grid of integrated voltage regulators, either near-chip (in the package substrate or interposer) or on-chip. As an example, a review of a PMIC datasheet with 6 buck regulators operating at 3MHz and 13 linear regulators using discrete chip inductors with a height profile of 1mm shows that moving all the passives off the motherboard would typically result in a 2x area reduction, a 6x volume reduction and a 3x to 4x height reduction of the power supply solution.

Solutions that are currently being pursued to reduce the size of magnetics and allow them to be integrated in-package or on-chip include micro-inductors fabricated using thin film semiconductor/MEMS processing (Ferric/TSMC, Dialog) on silicon or on package interposers, and magnetics embedded in organic packages or substrates (Intel FIVR, Dialog Merckx, AT&S/Tyndall 2020).

The big challenge for the use of integrated magnetic solutions is the need for high performance components which are typically taking up a footprint of less than 1 to 2 mm^2 and have a profile of less than 200 µm. High performance requires that the micro-inductor to deliver efficiencies in the 90%+ range, ideally as high as 95/96%. A key figure of merit is the inductance per milliohm (typically nH/mOhm) for DC current carrying capability and an AC resistance (Q-factor) associated with the high frequency ripple currents and associated harmonics.

Another important figure of merit is the inductance per mm^2. A small footprint for the magnetics is required:

- to minimize the expensive silicon area being utilized;
- the need for the inductors not to impact on the routing of interconnect from the SOC to package/substrate, or interposer to the motherboard; and
- ultimately to try to ensure that the micro-inductor footprint is similar to or smaller than the silicon circuit area that is being powered, as for example might be the case with a microprocessor with multiple cores with the expectation being that we will be dealing with 100+ core processors within the next decade.

Achieving the above footprint and performance specifications typically requires a significant increase in the frequency of operation of the voltage regulators from the standard used today of 1 to 10MHz. Over the last decade, technical papers from both academia and companies have presented integrated voltage regulator solutions that have operated from 20MHz up to and beyond 300Mhz. Typical inductances required range from 100-200nH at 20Mhz to 1 to 5nH for operation at 100Mhz or higher.

Air-core inductors embedded in the processor substrate have been used in commercial product (Intel FIVR) and offer a good solution for IVRs in the range of 100MHz and beyond. Other solutions include the use of low resistance RDL (redistribution layer) interconnect on the IC or an inductance provided by interconnect going from/to the processor chip through bumps, vias and susbtrate interconnect. Two challenges relate to the low inductance per milliOhm capability for small footprints, and the potential issue of EMI radiation causing interference with neighboring on-chip analog circuits.

The performance of inductors and transformers is fundamentally limited by the availability of magnetic materials. Current work-horse magnetic materials such as ferrites and metal ribbons have inherent limitations that make them inapplicable for high-frequency switching topologies.

Extensive academic research and pre-commercial (Intel, Enpirion, Ferric/TSMC, Dialog) work has been reported on the use of thin-film soft magnetic materials being used to enhance the inductance per milli-ohm (nH/mOhm) and per mm^2. To date, no commercial product has been released using thin-film magnetics on silicon.

Such "metastable" structures are currently only deposited with sputtering techniques, which are unfortunately limited to lower film thickness and low-throughput processes. These nanomagnetic films meet all the requirements for magnetic properties but are expensive to deposit in adequate thicknesses for power handling. The magnetic materials in the inductors are made of amorphous cobalt alloy with low coercivity (< 1 Oe) and high saturation field (~ 25 Oe). The magnetic films are separated by thin insulation layers (laminations) in order to suppress eddy current loss.

The multi-layered magnetic films, such as those in Figure 7, show high permeability of 300 to 600 up to 100 MHz. Inductors with the films as magnetic cores show stable inductance until 100 MHz. Originally developed by Intel, and recently by Ferric/TSMC, sputtered films are considered a strong contender for on-chip power regulation while

magnetic composites are the preferred candidates for substrate-embedded magnetics with higher current-handling and lower losses. The major challenge here is to minimize AC losses due to hysteresis and, especially, anomalous losses in the magnetic material, which can be considerable. Details are provided in the HIR Materials Chapter.

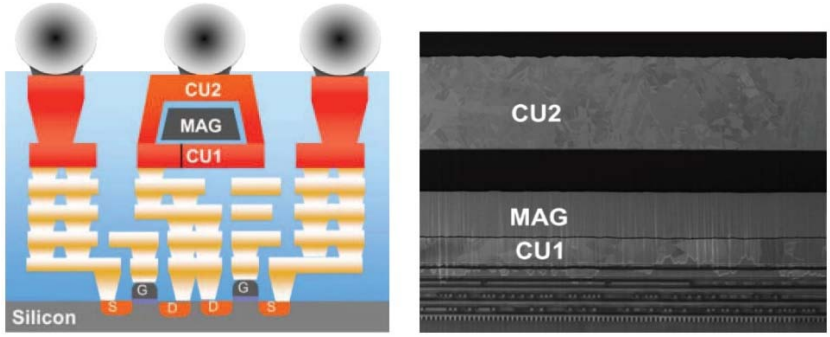


Figure 6. Left: Illustration of magnetic thin-film inductors integrated with ICs. Right: SEM cross-section of magnetic thin-film inductors integrated with ICs. However, all these approaches fall short in meeting the power density, scalability and efficiency challenges (Courtesy of Ferric Inc).

Currently, proposed thin-film, magnetic-core, micro-inductor solutions at a pre-commercial stage are all utilizing a solenoid construction, whereby a two-layer copper interconnect of windings is separated by a multilayer thin film magnetic core. This configuration presents a relatively straight-forward manufacturing process with the processing of a single multilayer magnetic film being the only deviation from conventional processing. A higher inductance density solution with lower DC resistance involves the wrapping of the conductor/winding layers in a magnetic film (a clad structure) (Intel, Tyndall). This offers potentially better EMI control but presents significantly extra complexity in fabrication.

A significant challenge with thin-film magnetic materials, compared to conventional bulky ferrite chip-inductor solutions or air-core inductors, is their saturation current of around 0.5 to 1.0 amps. Air-core inductors do not have such a constraint. Using coupled inductors allows the saturation current to be increased up to 2.5 to 3 Amps. Intel demonstrated more than a decade ago how a highly granular array (more than one hundred inductors on silicon) of multi-phase coupled inductors could overcome this issue. Further work is needed here to establish how to trade-off the area taken up by a large array of micro-inductors against the need for the distribution of very high I/O count interconnect from an SOC to the motherboard.

A novel concept recently presented by Tyndall is the idea of moving away from a lateral, planar magnetic structure to a 3D inductor whereby a copper pillar is coated with a suitable high frequency magnetic material. The solution presents the opportunity for 100 to 200 micron high, 1-5nH inductors with very low dc resistance giving up to 6nH/mΩ in a footprint of as little as 0.2 x 0.2 mm^2.

Alternative approaches to silicon-based micro-magnetics are being extensively studied by passive component companies and, more recently, by PCB/substrate companies. Emerging approaches utilize magnetic polymer composites with flake morphologies or incrementally enhance ferrites and metal flakes. This effort has been led by Nitto Denko, KEMET-Tokin and Murata. High permeability and softness (low coercivity) with frequency stability (high resistivity for low eddy currents and high FMR) requires nanostructured cobalt and iron alloys (< 5nm) with interspersed oxides (<5 nm) to enable exchange coupling and electrical isolation.

Recent research (AT&S, Tyndall) in the European Horizon project (GaNonCMOS) and by other organic substrate companies is focused on the embedding of magnetic materials in the organic substrate and utilizing the substrate's copper interconnect and through-hole/blind via structures to form suitable windings. This follows AT&S' previously successful business in embedded silicon die. While promising, more work is needed to deliver high performance inductor components that can operate at 20MHz+ and have an acceptable footprint.

While the emphasis here has been on the miniaturization of magnetics for integrated voltage regulators, by moving to very high frequencies in the range 20MHz to over 100MHz, there is a significant challenge in addressing the issue of associated high-efficiency power switch technology that can operate at multi-MHz frequencies. One option is to use specific power semiconductor process technologies, whether in silicon or wide-band gap materials, as part of a PSIP configuration. A variant on this is to use tailored converter topologies that operate at low frequencies (1-10MHz) but using low-value inductances suitable for magnetics on silicon or competing technologies. This is particularly appropriate in the context of hybrid converters combining switched capacitors with an inductor or

resonant topologies. However, in the case of PSIP and PwrSOC solutions, the challenge is on using multi-level semiconductor switches fabricated using the advanced CMOS nodes being used in the associated SOC.

Manufacturing Supply Chains

As mentioned previously, the only commercial integrated voltage regulation (IVR) solution to date is the Intel FIVR technology using embedded air-core inductors in the micro-processor package. Through their partnership with Ferric Semiconductor, TSMC has been able to demonstrate the capability to fabricate magnetics on silicon devices on advanced-node silicon with overall converter efficiencies close to 90%.

Integrated magnetics presents a potentially significant disruption to the traditional supply chain for discrete magnetic components. At first glance, the TSMC engagement in the fabrication of magnetics on silicon, and the Intel progress made more than a decade ago, would suggest that, in a similar way to high density trench capacitor technology, integrated magnetics on silicon will become a key offering for semiconductor foundries, in their BEOL (back end of line) as part of their SOC/processor business. However, while the semiconductor foundries can leverage a 30+ year history in the magnetic disk-head industry and, more recently, the experience gained in MRAM, and even thin film magnetic sensors, there are other sectors of the microelectronics industry supply chain that may also be able to play a role in the roll-out of high-volume integrated magnetics.

The OSAT (Outsourced Semiconductor Assembly and Test) houses offer BEOL wafer processing in the form of wafer bumping and RDL processing. The copper thickness used in RDL is potentially more suited to deliver low-resistance magnetics, and therefore the OSAT companies could add value through the integration of high-efficiency magnetics – this possibility is enhanced when one considers that the inductor winding line/space dimensions typically should be in the range 50 to 100 µm to deliver appropriately low DC resistances.

As we have already mentioned, organic substrate companies providing microprocessor packages are already exploring the embedding of both semiconductor die and magnetics. Trends in line/space dimensions for these substrates are moving into the 10 to 20 µm range and lower. Therefore, there is a business opportunity to be explored by this sector of the microelectronics supply chain, either to embed silicon magnetics into the microprocessor substrate or to integrate laminated magnetic layers with fine geometry conductors.

There is an open question at present regarding whether or not the integrated magnetics should be monolithically fabricated on the advanced CMOS wafers or should be processed separately for later packaging/assembly. The challenge here is to ensure that the magnetic component footprint is compatible with the advanced CMOS devices and that the magnetics component process yield is appropriately high.

While sputtering of magnetic laminations is currently the principle approach to deposition of soft magnetic laminations, some companies (Enachip) are exploring alternative processes based on electroplating technology which could offer much higher deposition rates using lower-cost manufacturing systems. In parallel, some of the semiconductor equipment companies (Evatec) are exploring how to dramatically speed up sputter deposition rates to deliver cost-effective sputter deposition processes.

An area that still needs addressing is the nature of wafer-level test of magnetics on silicon. Wafer-level testing can be done for small-signal inductor testing. However, high-current inductor testing at wafer-level needs to be considered. Furthermore, the output inductor in a converter circuit sees a combination of both dc current and ac ripple which determines the true inductor performance in terms of in-converter efficiency. Currently, such so-called large-signal testing is undertaken using discrete micro-inductors either using a special test board or in the final power converter circuit. In the case of the converter circuits being part of the SOC/microprocessor, it is highly unlikely that an in-converter power circuit will be available for test in advance of the final SOC silicon.

Very little information has been published on the reliability issues for integrated magnetics, whether on silicon or embedded in an organic substrate. Issues that may require investigation include performance drift due to thermal and/or thermomechanical stressing or ageing. Experience from the disk-head, MRAM and magnetic sensor sectors should provide a valuable benchmark.

Finally, the issue of potential near-field EMI from micro-magnetics causing interference in SOC/microprocessor circuits needs to be explored and, if needed, solutions for mitigation explored and implemented.

Novel device interconnection approaches and materials

Miniaturized and stacked packages handling ever larger amounts of power have higher power densities, and the heat generated in the package must be discharged through a smaller backside surface area. Furthermore, limited access to the devices within a substrate renders traditional convection cooled heatsinks mounted on the back of the

package ineffective. Therefore, new approaches and materials are needed for packaging and interconnect. In particular, the smaller packages have led to a drive for replacing wirebonds with flip chip and other direct bonding approaches that allow double-sided cooling. Finding reliable attach materials, however, has proven to be a challenge, as new soldering and sintering methods have been developed and studied, but their long-term reliability is still uncertain.

Another interconnection development driven by the package size reduction has been the development of multifunctional electrical and thermal conduits such as through-substrate vias and through-silicon vias that are designed to extract heat from the central regions of the package while establishing electrical connections between layers of the package. This review will discuss recent developments in package approaches, interconnections, and thermal management for embedded power electronics and will complement similar efforts by PSMA in their Power Technology Roadmap [8].

Multiple advances in packaging methods have characterized the progress of power electronics integration in the past decade. A few major packaging developments include: (i) planar interconnects; (ii) flip-chip bonding; and (iii) chip embedding [9]. Planar technology has been used in the industry and has resulted in developments in stacking and interconnection. Exploration of flip-chip technology has yielded methods of converting standard dies to a format compatible with their technology, useful in an industry that still favors the aluminum wirebond [9]. Chip embedding has developed a variety of methods of embedding active, passive, and formed components into organic and inorganic substrates.

Planar Interconnects

Planar interconnects were created by both Siemens and Mitsubishi [9,10] for use in their vehicles' power modules in the early 2010s. Their one-layer approach to the planar interconnect scheme saw reductions of up to 50% in parasitic inductance [10,11]. Since these single-layer modules were introduced, the technology has matured significantly with the introduction of copper clip bonding and the incorporation of multiple layers. Copper clip bonding was developed to replace aluminum wirebonds due to better electrical and thermal conductivity. The electrical connections that double as heat conduction paths make copper clips an efficient way to reduce the size of the package.

The multilayered approach has also made progress. For instance, one module laid the chips in a parallel arrangement between sheets of copper [12]. This approach to planar connections between the power electronics and the gate drivers consistently achieved improved thermal and electrical performance [12]. The multilayered approach consists of a cooler-substrate-die-substrate-cooler arrangement that allows for efficient cooling of both sides of the package, but leaves little room for variations in the heights of the die [13-15]. Height variations in the die cause some chips to be distant from the single DBC or PCB plate that forms the top of the package which can affect the quality of their electrical and mechanical connections. Recent structures allow for planar connections of components of varying heights by employing copper spacers. The copper spacers are used to augment heights of the smaller chips and establish strong electrical and mechanical contact [16]. Reductions in parasitic inductance and the ability to incorporate a variety of components in planar packages has enabled the integration of power components, improvements in performance compared to traditional packages, and reduced package dimensions.

Flip-chip Interconnection

Flip-chip packaging techniques have also been pursued by academia [13]. The flip-chip approach seeks to eliminate aluminum wirebonds from the package by replacing them with solder bumps that have been deposited onto the chip pads. The die then becomes a surface mount component where the solder ball array acts as a mechanical and electrical connection [15]. However, most commercially available SiC power devices aren't designed for such applications, instead favoring electrical connections via aluminum wirebonds. Researchers have embedded multiple commercially available SiC power devices that were designed for wirebond connections into the package, including SiC Schottky diodes [16], and achieved up to 24% reductions in on-state resistance. Others have achieved as much as a 50% reduction in parasitic inductances [18], again without altering the die's functional properties. These results have demonstrated that the performance of SiC chips can be dramatically improved simply by adjusting the approach to packaging the components.

Chip Embedding

Finally, chip embedding-based packages have made extensive progress [8,20]. Researchers have embedded active, passive, and formed components in layers of organic and inorganic substrates. One chip-embedding process uses sintered silver to attach IGBTs and diodes to a base substrate that has been metallized with copper. Afterward,

the chips are embedded by lamination into a prepreg layer and vias are laser-drilled to the chip pads. The vias are then filled with copper and etched [21]. This process is representative of many chip-embedding techniques, which have flexibility in the order, layout, and species of chip that is embedded. IGBTs, diodes, MOSFETs, and myriad other components have been embedded face-up and face-down to achieve a more efficient module than was possible with traditional surface mount packaging methods [9].

The replacement of wirebonds with interconnects such as TSVs, metal and flip chip solder bumps, and large area solders and die attaches, is a prerequisite for reducing the size of the package. Standard solders, including the lead-free SnAg solder, are incapable of withstanding the thermomechanical stresses induced by the novel packages [22]. Furthermore, traditional wirebonds are bulky and inefficient. As a result, new die-attach methods and materials have been developed as replacements. The methods include high-temperature soldering, transient liquid-phase bonding, and sintered silver or copper [23].

Metal-based Sintering

Metal-based sintering has been developed for large area joints because of its ability to withstand the high temperatures and temperature cycling of power modules. Developing a high-quality connection between the sinter paste and substrate relies heavily on the treatment of the substrate. One report found that sintering on an Au-finished Si_3N_4 substrate gave adhesive strengths of up to 70MPa when applied with a 6MPa pressure [24]. It has also been demonstrated that sintering on an unmetallized but polished DBC substrate at 6MPa yields good adhesive strengths [25]. Furthermore, under thermal cycling, the degradation of these silver-based die attachments has been found to be minimal [26]. Research has also demonstrated that the incorporation of varying levels of molybdenum and silver-coated nickel particles allows for control of mechanical properties such as coefficient of thermal expansion and Young's modulus [27]. After proving the viability of pressure sintering for die attach, one study demonstrated connections with shear strengths in excess of 15 MPa without elevated pressure application techniques [28] to enable less strict manufacturing practices. While these results demonstrate that the pressureless sintering process has some viability, other authors have argued that the reduction in strength is due to a lower quality interface that limits thermal conductivity of the materials [29], making it the less viable option. More research will need to be conducted on this topic to establish the best fabrication processes, but these preliminary results have demonstrated the potential of the materials to reliably replace the traditional aluminum wirebond. Research has moved away from silver sintering to copper sintering owing to the issues of silver migration under high voltage and temperature, along with the high cost of silver paste, especially nanoparticle paste. Low-temperature sintering of copper can provide similar levels of electrical and thermal conductivity at much lower cost. However, it requires sophisticated bonding equipment that allows processing in a reducing atmosphere and has a narrower process window than silver sintering. These aspects require additional work for scale-up and widespread adoption of the technology.

Transient Liquid Phase Sintering

Other promising die attach techniques have also been developed – first, through the diffusion soldering of copper-tin intermetallics. The intermetallic joints created by these techniques have exhibited melting temperatures of 676°C and 415°C (Cu_6Sn_5) with remelting temperatures well in excess of 400°C [22]. Their strength and thermal stability have made them candidates for the future of die attach along with silver-based sintering methods described above. Additionally, metal bumps have allowed further elimination of wirebonds in 3D packaging. A substrate-chip-bump-chip-substrate approach investigated in one paper demonstrated the effects of different bump cross-sections and material compositions on the thermomechanical reliability of the package. The authors used copper-molybdenum solders in a variety of shapes to directly attach the chips to one another. Their method proved to be electrically successful but had limited mechanical reliability under electrical cycling [30]. While the technique has been successful in the lab, there are issues for large scale processing owing to the long curing times, up to 30 minutes, and narrow process window. Furthermore, the high stiffness of the materials can lead to die cracking. The batch-to-batch uniformity is also poor owing to the difference in the particle loading and size between batches, leading to yield issues. Additional work is needed in process development and inspection (e.g. backscattering) to address these scale-up issues.

In summary, heterogeneously integrating the power electronics into the overall system requires the ability to embed the interconnections and stack devices. As such, wirebonds must be eliminated and replaced with through-silicon vias, through-substrate vias, metal bumps, flip chip solder bumps, large-area solders and die attaches, and direct copper interconnect patterning. Each of these technologies has seen extensive development over the last ten years, and continues to be further refined. Flip chip solder and metal bumps must be able to handle the levels of

power they are asked to carry without suffering electromigration. Direct copper interconnect patterning needs to have sufficient adhesion to the devices and sufficient thickness to handle high currents without enduring stress levels that cause fracture. Lead-free solders along with copper and silver sinter pastes are being developed for large-area solder connections to minimize thermomechanical stresses.

Another way to reduce size and promote heterogeneous integration is through combining separate functions into multifunctional components. Through-silicon and through-substrate vias must serve not only as electrical connections but also as thermal conduits. Embedded thermal management systems consisting of fluid-filled conductors can serve not only as coolers but also as power busses. Developments are underway in these areas but they need to be further enhanced.

Thermal management

Embedded thermal management systems will require not only the development of complex integrated microfluidics but also simpler solutions. For example, higher thermal conductivity encapsulants as well as anisotropic conductive materials embedded near the heat dissipating devices can remove heat to the sides of the heterogeneously integrated system where it is easier to remove by external cooling elements. Furthermore, heterogeneous integration requires techniques to cool the power electronic devices without allowing heat from those high-loss devices to migrate horizontally or vertically to warm more temperature-sensitive electronics. Examples of the solutions being developed to address this problem are thermal metamaterials and thermal isolation materials. These materials combine a low thermal conductivity backbone, which minimizes undesirable heat spreading, with high thermal conductivity elements (e.g. traces or vias) that allow the heat to be safely moved along paths past the thermally sensitive components to the cooling units.

Advanced thermal management is critical for power electronics targeting the EV/HEV market with its higher voltage requirement (see chapter 5). A power converter will require an effective thermal conductivity greater than 500 W/mK at a target price around $1/kW in the next 10 years. The accelerated incorporation of WBG technologies using SiC has allowed power modules to achieve better performance and cost targets. Even so, with the larger heat dissipation in power module packaging, increasing thermal conductivity is now of comparable importance.

Inductor cooling is also of high importance, as inductors are often the highest power-loss element in the converter, exceeding the losses of the switching devices, now that the switches utilize the more efficient wide bandgap materials. Research is addressing this issue in three ways. The first is through the development of materials with higher electrical conductivity than the current electroplated or printed copper and silver windings to minimize Joule heating. The second is through the development of substrates with integrated cooling channels. The third is through the development of hollow conductors through which coolant can flow to internally cool the windings.

Current packaging technology with Cu conductors, wire bonds, and solder attachments is evolving better thermal performance materials (e.g. Ag, graphene or diamond conductors with wire-free interconnects and sintered attachments). These changes cause the thermal performance to increase by a few hundred W/mK, but there is an attendant cost increase in dealings with the new material and process technologies as well. Table V below provides an overview of the package development for the next 5 years and beyond. The key challenge in power modules is evolving towards better thermal performance for improved reliability at compatible cost. Currently, there is an extensive focus on using embedding technology for higher power handling. It helps to improve the thermal performance of the package through direct cooling at top and bottom sides of the die. In addition, embedding allows scalable solutions for a more heterogeneously integrated Power Module. Examples of the components to integrate in a package are the power diode, power FET, driver, passive components and sensors. There have been significant innovation activities to date allowing the embedding of a few components in a power module. Nevertheless, innovation is continuing to enhance integration by introducing more components (e.g. sensor or RF) in the power modules as a system solution. Further embedding is one of the key challenges in the development of future power modules with more functional integration that achieve better thermal conductivity with comparable cost.

Table V – Interconnect and Thermal Management Developments Needed and Timeframes

	5 years	**10 years**
Interconnect	Ribbon bond, Flip-chip	Embedding, Direct Bond, Flexible Foil
Die Attach	Cu/Ag Sintering, Brazing	TLPS, double side direct cooling
Substrate Material (DBC)	Si_3N4	Elimination of substrate with die on baseplate
Thermal Interface Material (TIM)	TIM with higher Thermal conductivity	Elimination of TIM for direct cooling (die embedding on base plate)

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