HETEROGENEOUS INTEGRATION ROADMAP

2019 Edition

Chapter 17: Test Technology

Section 00: Executive Summary

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Chapter 17: Test Technology

Executive Summary and Scope

This bi-annual update to the heterogeneous integration testing roadmap contains our best estimates of key trends influencing this industry over the next 15 years. This roadmap includes trends in semiconductor device technologies and their impact on test, as well as roadmaps for key test enablers (Device Handlers, Test Interfaces, and Test Methods). The resulting Cost of Test is also analyzed and discussed.

Key Implications per Device Technology

RF Devices: The ramp of 5G devices is going to challenge the test industry in terms of frequency, port-count, and lower noise margins. Additionally, production test methods for confronting beam-steering are of concern.

High-Speed Digital Devices: Signal delivery through clean traces and a test interface (probe or socket) is becoming a major concern as speeds move past 16 Gbps (today) to more than 60 Gbps during this roadmap timeline. Deployment of multi-level technologies (PAM4) challenge noise margins and instrument designs. The large quantity of high-speed digital interfaces per part is another challenge lacking an obvious solution.

Photonic Devices: The large number of photonic standards together with an ever-increasing number of ports, while geometries continue to shrink, is going to be a significant challenge for the industry to address in a cost-effective manner.

Logic Devices: Growing device complexity is having a big impact on the industry today. This trend is expected to continue with pattern depths and structural test times doubling every three years over the roadmap period. Higher complexity also drives up the device cooling requirements during test.

Specialty Devices: The trend for tighter-pitch displays and cameras is resulting in a need for probing contacts of finer pitch and smaller size. At the same time, higher volumes are driving the need for more test parallelism. The large volume of inexpensive IoT sensor devices of various types will continue to challenge the industry.

Memory Devices: NAND Flash device test times will continue to scale with higher densities. The introduction of high-speed serial memory interfaces may change the test approach. Achieving Known-Good-Die (KGD) and Known-Good-Stack (KGS) for memory devices destined for 2.5D and 3D integrations will continue to be of growing importance.

Analog/Mixed Signal Devices: Technology advances are expected to challenge mixed-signal devices in about five years as speeds and resolutions increase while voltage swings continue to drop.

Key Implications per Device Handling and Contacting

Device Handlers: Wafer probe and component test handling equipment face significant technical challenges in each market segment. Common issues on both platforms include higher parallelism and more capable and flexible thermal solutions, which result in increasing capital equipment and interface cost.

Probes: The probe complexity roadmap continues to accelerate at challenging rates. Pad size and pitch are expected to keep compressing with site counts increasing. With the manufacturing of super-high-speed serial and 5G devices, probe technology is being forced to provide cost-effective 40-80 GHz bandwidth solutions.

Key Implications for Test Methods

System Level Testing (SLT): A resurgence in functional/SLT testing, especially at the module level, is a major industry trend. The system-level boot-up test remains the critical acid test for most electronic systems. Efforts continue to pinpoint the faults responsible for structural test failures. In the meantime, SLT deployments are expected to rise.

Adaptive Testing: This technology continues to ramp in many ways throughout the industry. Expansion will be challenged by the explosion of data, the need for effective analysis, and response tools, which critically need a universal data model/format to enable “Big Data” analysis independent of the source Further challenging this methodology is multi-vendor integrations and data security concerns.

Concurrent Testing: Expanded usage of concurrent test techniques is constrained by limitations in device access (pins) as well as a lack in standardized tools and methods. A breakthrough for this technology will come when efficient and standard test interfaces are implemented for analog and RF testing. Analog scan is one technology starting to show progress.

2.5D/3D Testing: Known-Good-Die (KGD) are very important today and will become even more important in the future (larger parts with more gates, more devices per assembly). Achieving KGD will push test content earlier in the manufacturing flow, challenging wafer- and/or die-level testing. Testing the multi-chip assembly is expected to be done by traditional approaches including boundary-scan and system-level testing.

Reliability Testing: Increased quality and reliability needs of the automotive and mobility integrated circuit markets are driving additional test and burn-in requirements, including system-level test. Packaging innovation, including the need for KGD, drives additional test fixturing and testing challenges, as does multi-die packaging.

Design-For-Testability (DFT): Ongoing use of pattern compression and the use of hierarchical design techniques is continuing to have a positive impact on pattern depths and device test times. The quest for higher compression ratios is proving to be a difficult one.

Yield Learning: Improvements are needed in resolving cell-internal defects. Achieving this goal will generate significant amounts of data requiring careful analysis. Automotive reliability requirements are driving a change of mindset away from structural test coverage being adequate to functional, system level, and in-situ testing techniques becoming the new focus.

Key Implications for Cost of Test

The cost of consumable products in device testing is starting to have a dominant impact on the industry moving forward. The result is many anecdotal comments that moving to a new transistor geometry node has cost more in terms of consumable products (probes, sockets, interface boards) than the cost of the test instrumentation to do the new level of testing. Compounding this problem is the requirement for ongoing maintenance of these components as well as their limited lifetime.

Another major trend having a significant impact on the cost of semiconductor testing is longer test times. Increased device complexity drive up the pattern depths and test times at a rate significantly faster than the rate of complexity increases (exponentially). We no longer talk about test times of a few seconds and often end up with test times of a few minutes. Without a breakthrough in scan testing speeds, this trend is expected to continue for monolithic devices during this roadmap period.

Heterogeneous integration will allow the large devices to be split up into smaller chips with the test time impact now being exponentially reduced. Additionally, multiple smaller devices can usually be tested concurrently for additional savings of test costs.

Many efforts are expected to try and reduce test costs moving forward including higher parallelism, reduced test time overhead, reduced equipment and consumable costs, etc. Despite these efforts, increased complexity and demands for higher performance testing will likely cause the cost of leading-edge test solutions to increase significantly.

Detailed Discussion of the Trends

Each of the topics highlighted above as key implications for test moving forward are explored in precise details in the next sections.

Acknowledgments

This update to the test roadmap is output from a team of more than 120 test experts hailing from more than 50 companies world-wide. The leadership team for this effort is shown below:

Dave Armstrong:	Chairman, Test Technology Working Group, Heterogeneous Integration Roadmap

2.5D/3D device test	Bill Eklow	Photonic Test	Dick Otte
Adaptive test	Phil Nigh	Probe Cards	Dave Armstrong (Acting)
Analog and Mixed-signal	Don Blair	Prober	Yoichi Shimizu
Concurrent Test	Kenichi Anzou	Radio Frequency	Don Blair
Cost of Test	Ken Lanier	Reliability Testing	Carl Buck
DFT & SOC Device Testing	Kenichi Anzou	Specialty Device Testing	Wendy Chen
Handlers	Masahito Kondo	System Level Test	Harry Chen
High Speed IO Testing	Yi Cai	Test and Yield Learning	Anne Gattiker
Logic device test	Marc Hutner	Test Sockets	Rick Marshal
Memory Test	Dave Armstrong (Acting)		

Test Technology Working Group Contributors:

Stacy Ajouri, Lionel Kimerling, Mike Alfano, Craig Kirkpatrick, Kenichi Anzou, Leo Kluger, Takenori Aoki, Masahito Kondo, Jeff Arasmith, Hiroshi Kurosaki, Dave Armstrong, Greg Labonte, Keith Arnold, Ken Lanier, Roger Barth, Lenny Leon, Brady Benware, Ira Leventhal, Keren Bergman, Clark Liu, Paul Berndt, John MacWilliams, Mark Berry, TM Mak, Anil Bhalla, Yiorgos Makris, Don Blair, Adriano Mancosu, Shawn Blanton, Peter Maxwell, Daniel Bock, Fabio Morgana, Bill Bottoms, Franco Motika, Carl Bowan, Nilanjan Mukerjee, Carl Buck, Chris Nigh, Ken Butler, Phil Nigh, Yi Cai, Peter O'Neill, John Caldwell, Richard Otte, John Carulli, Sule Ozev, Krishnendu Chakrabarty, Gilles, Wendy Chen, Jayson Park, Harry Chen, Mike Peng Li, Wu-Tung Cheng, Jan Peters Weem, Vivek Chickermane, Robert Pfahl, Tim Cleary, Robert Polster, Chris Coleman, Chris Portelli, Zoe Conroy, Dieter Rate, Adam Cron, Jeff Rearick, Al Crouch, Graham Reed, Robert Daasch, Herb Reiter, Dirk de Vries, Joseph Reynick, Rao Desineni, Jason Rivers, Makoto Eiki, Mike Rodgers, Bill Eklow, Jeff Roehr, Dan Evans, Pete Rogan, Ira Feldman, Mark Roos, Shawn Fetterolf, Rajiv Roy, Derek Floyd, Sam Salloum, Bert Gab, Ben Sarpong, Michael Garner, Philip Schofield, Anne Gattiker, Michael Schuldenfrei, Xinli Gu, Rene Segers, Richard Hanvey, John Shelley, Ian Harrison, Yoichi Shimizu, Don Hartman, Mustafa Slamani, Kazumi Hatayama, Wesley Smith, Klaus-Dieter Hilliges, Stephen Sunter, Andy Hsu, Aoki Takenori, Tom Hsu, Steve Tilden, Marc Hutner, Srikanth Venkataraman, Shuichi Ito, Li-C Wang, Erik Jan Marinissen, Thomas Williams, Rene Jonker, Scottie Wyatt, Matthias Kamm, Tian Xia, Rohit Kapur, John Yi, Brion Keller, ChuHui Yu