HETEROGENEOUS
INTEGRATION ROADMAP

2019 Edition

Chapter 17: Test Technology

Section 03: Logic Device Testing

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Section 3: Logic Device Testing

The focus of this section is the testing of CMOS digital logic portions of highly complex digital logic devices such as microprocessors, and more generally the testing of logic cores that could stand-alone or be integrated into more complex devices. Of primary concern will be the trends of key logic test attributes assuming the continuation of fundamental roadmap trends. The “high volume microprocessor” and the “consumer SoC” devices are chosen as the primary reference because the most trend data are available for them. Specific test requirements for embedded memory (such as cache), I/O, mixed-signal, or RF are addressed in their respective chapters and must also be comprehended when considering complex logic devices that contain these technologies.

Key Logic Device Testing Trends

The trends in Table 1 are extracted from other parts of the roadmap and are reproduced here to form the foundation of key assumptions used to forecast future logic testing requirements. The first two line-items in the table show the trends of functions per chip (number of transistors) and chip size at production. Chip size in terms of area is held relatively constant aside from incremental yearly reductions within a process generation. The next line item reflects a trend toward multiple core designs to address, in part, what has become the primary microprocessor scaling constraint – the diminishing returns of clock frequency increases. There is a trend to greatly increase the number of cores within each process generation and these will include multiple cores of a particular instruction set, but also include other types of cores, such as graphics units (GPUs), Specialized I/O units (e.g. USB) and various other cores not necessarily specific to a microprocessor.

The internal scan data rate of a device is the rate at which ATPG data can be shifted across the scan latches between test sequences. These are commonly known as load/unload sequences. In the ITRS roadmap this was assumed to be increasing by a percentage increase per year (15%). There are several reasons why this trend has a fundamental limit. The toggle rate for scan, which translates to power utilization of the device under test, is much higher than for functional operation of the device. The device would consume significantly higher power during test, which translates to power degradation of supply levels, higher temperature of operation and a shift in operating point of the logic elements under test. As devices move to finer-pitch geometries, the voltage levels required are also reducing, which further impacts the effects mentioned. In addition to power demands, the timing closure of scan paths is also more difficult at higher frequencies, resulting in a significant amount of work to ensure high speed operation. As a result, the HIR roadmap projects that as devices reach frequencies of 125-150MHz for internal scan rate, the rates will no longer increase compared to historical rates.

The effective scan compression rate will continue to increase, but the increase is accounted for in a different way. The Logic Assumption sheet reflects the effectiveness of compression of a single IP block or subsystem. Effectiveness of compression at this level of the design is slowing. Several years ago, the concept of hierarchal scan was introduced by the EDA community. This is accounted for in the Logic Test Data Volume requirement, Table 2, and realized with the number of identical IP blocks, where the same patterns could be applied at the same time.

In recent years, the fault models used for logic test have also improved. The shift was from a fault model based on a Boolean equation to one based on transistor configuration. This has been accounted for in the models by starting the projections from a transistor count rather than equivalent gates/functions. Presently the increased pattern count has been counterbalanced by improvements in compression and scan-rate increase. As new fault models are introduced to reach enhanced quality goals, the data volume may increase beyond what is projected in our model. This will be addressed in a future revision of the HIR roadmap.

Table 1: Logic Assumptions

Year of Production	2018	2019	2020	2021	2026	2031
Design Related Backgound Data						
Chip size at production (mm²)						
MPU-HP - High Performance MPU (Server)	261	261	261	261	261	261
MPU-CP - Consumer MPU (Laptop/Desktop)	140	140	140	140	140	140
SOC-CP - Consumer SOC (Consumer SOC, APU, Mobile Processor)	140	140	140	140	140	140
# of Transistors (M) [T]						
MPU-HP - High Performance MPU (Server)	15306	19284	22495	26241	56684	122447
MPU-CP - Consumer MPU (Laptop/Desktop)	5768	7268	8478	9890	21363	46147
SOC-CP - Consumer SOC (Consumer SOC, APU, Mobile Processor)	2756	3438	4291	5357	16372	50448
% Logic Transistors						
MPU-HP - High Performance MPU (Server)	35%	35%	35%	35%	35%	35%
MPU-CP - Consumer MPU (Laptop/Desktop)	63%	63%	63%	63%	63%	63%
SOC-CP - Consumer SOC (Consumer SOC, APU, Mobile Processor)	81%	82%	83%	83%	87%	88%
% Memory Transistors						
MPU-HP - High Performance MPU (Server)	65%	65%	65%	65%	65%	65%
MPU-CP - Consumer MPU (Laptop/Desktop)	37%	37%	37%	37%	37%	37%
SOC-CP - Consumer SOC (Consumer SOC, APU, Mobile Processor)	19%	18%	18%	17%	13%	12%
% Random Transistors						
MPU-HP - High Performance MPU (Server)	0.2%	0.2%	0.2%	0.2%	0.2%	0.2%
MPU-CP - Consumer MPU (Laptop/Desktop)	0.3%	0.3%	0.3%	0.3%	0.3%	0.3%
SOC-CP - Consumer SOC (Consumer SOC, APU, Mobile Processor)	0.4%	0.4%	0.4%	0.4%	0.4%	0.4%
VDD(V)						
MPU-HP - High Performance MPU (Server)	0.78	0.77	0.75	0.74	0.66	0.64
MPU-CP - Consumer MPU (Laptop/Desktop)	0.78	0.77	0.75	0.74	0.66	0.64
SOC-CP - Consumer SOC (Consumer SOC, APU, Mobile Processor)	0.57	0.55	0.53	0.51	0.43	0.41
Test Related Assumed Data						
Maximum Power Consumption at Test (W)						
MPU-HP - High Performance MPU (Server)	400	400	400	400	400	400
MPU-CP - Consumer MPU (Laptop/Desktop)	250	250	250	250	250	250
SOC-CP - Consumer SOC (Consumer SOC, APU, Mobile Processor)	40	40	40	40	40	40
Effective Number of External Scan Pins (TDI+TDO) [1]						
MPU-HP - High Performance MPU (Server)	256	256	256	256	256	256
MPU-CP - Consumer MPU (Laptop/Desktop)	256	256	256	256	256	256
SOC-CP - Consumer SOC (Consumer SOC, APU, Mobile Processor)	64	64	64	64	64	64
Effective External Scan data rate (Mbps) [1]						
MPU-HP - High Performance MPU (Server) [2]	131	137	144	150	150	150
MPU-CP - Consumer MPU (Laptop/Desktop)	131	137	144	150	150	150
SOC-CP - Consumer SOC (Consumer SOC, APU, Mobile Processor)	86	92	98	105	147	150
% Scan Chains Shared Btwn Homgeneous Logic (all device types) Homogeneous logic refers to logic contained in IP cores.						
MPU-HP - High Performance MPU (Server)	66%	67%	68%	70%	75%	80%
MPU-CP - Consumer MPU (Laptop/Desktop)	59%	61%	62%	64%	71%	76%
SOC-CP - Consumer SOC (Consumer SOC, APU, Mobile Processor)	37%	40%	42%	44%	55%	63%
Target Compression Ratio (all device types) [3]	134	143	154	165	251	410

[1] The external scan pin count and scan data rate are intended to suggest a scan bandwidth (BW=Pins*Data Rate). Since some devices use higher external data rates (via a SerDes) these terms are indicated as "effective" in order to normalize the results.

[2] slow growth rate maxing out at 150MHz [3] Was 10% per year growth, changed to base growth + acceleration

Table 2: Logic Test Data Volume

Year of Production	2018	2019	2020	2021	2026	2031
Worst Case (Flat) Data Volume (Gb)						
MPU-HP - High Performance MPU (Server)	6802	9256	11366	13957	38973	108829
MPU-CP - Consumer MPU (Laptop/Desktop)	4130	5620	6901	8475	23664	66079
SOC-CP - Consumer SOC (Consumer SOC, APU, Mobile Processor)	2133	2907	3964	5406	25444	116008
Best-Case Test Data Volume (Hierarchal & Compression) (Gb)						
MPU-HP - High Performance MPU (Server)	10.3	12.0	12.6	13.1	15.3	17.0
MPU-CP - Consumer MPU (Laptop/Desktop)	8.5	9.8	10.2	10.7	12.3	13.0
SOC-CP - Consumer SOC (Consumer SOC, APU, Mobile Processor)	7.0	8.4	9.6	11.5	24.2	45.5
Best-Case Compression Factor (Hierarchal & Compression) (Compression rate)						
MPU-HP - High Performance MPU (Server)	658	770	905	1069	2547	6388
MPU-CP - Consumer MPU (Laptop/Desktop)	488	571	675	795	1924	5084
SOC-CP - Consumer SOC (Consumer SOC, APU, Mobile Processor)	303	347	414	472	1050	2551

Table 3: Logic ATE Requirements

Year of Production	2018	2019	2020	2021	2026	2031
Minimum Required ATE Scan Pattern Depth (Relative to 2016 Pattern Depth)						
MPU-HP - High Performance MPU (Server)	X 1.34	X 1.54	X 1.60	X 1.64	X 1.84	X 1.97
MPU-CP - Consumer MPU (Laptop/Desktop)	X 1.34	X 1.55	X 1.58	X 1.63	X 1.80	X 1.81
SOC-CP - Consumer SOC (Consumer SOC, APU, Mobile Processor)	X 1.41	X 1.68	X 1.87	X 2.19	X 4.32	X 7.76
Maximum Required ATE Scan Pattern Depth (Relative to 2016 Pattern Depth)						
MPU-HP - High Performance MPU (Server)	X 1.85	X 2.52	X 3.09	X 3.80	X 10.61	X 29.63
MPU-CP - Consumer MPU (Laptop/Desktop)	X 1.85	X 2.52	X 3.09	X 3.80	X 10.61	X 29.63
SOC-CP - Consumer SOC (Consumer SOC, APU, Mobile Processor)	X 1.85	X 2.53	X 3.45	X 4.70	X 22.12	X 100.84
Typical Test Time (Relative to 2016 Pattern Depth) [1]						
MPU-HP - High Performance MPU (Server)	X 1.68	X 2.17	X 2.54	X 3.00	X 8.36	X 23.34
MPU-CP - Consumer MPU (Laptop/Desktop)	X 1.68	X 2.17	X 2.54	X 3.00	X 8.35	X 23.30
SOC-CP - Consumer SOC (Consumer SOC, APU, Mobile Processor)	X 1.62	X 2.06	X 2.62	X 3.33	X 11.15	X 49.87

[1] Test times assume that all the ATE Patterns are executed once without any looping or repetition

Trends impacting roadmap 2017-19

The model presented in this roadmap was generated in 2017, it is fair to ask about the impact of Artificial Intelligence (AI) and Automotive devices. Both of these markets are emerging as important drivers to our industry. What is known is that present AI devices best fit into the SOC category in 2019. While the number of compute elements are highly replicated, the way the designs are partitioned in the DFT tools do not take advantage of the hierarchy as do GPU device types. Over the near term we expect this to continue as there is a push for new architectures and product validation in the marketplace. As the AI segment matures, the effective compression rate and ATE Scan Pattern Depth will more closely track the MPU-HP segment for the large AI training and inference device types. Automotive also provides additional demands on this roadmap with the need for additional self-test coverage as well as increased quality which may drive further test intensity. Both topics will require further study for the next update.

Summary

The tables reflect the continuation of the trends that are known and that are accepted by industry. Historically, innovation in digital test has been driven by the economic need to keep the cost of test relatively flat. If Moore's Law scaling continues, it can be seen in the 2025 projections that an economic need for innovation is emerging. The cost problem may be further compounded by emerging automotive desire for part-per-billion (PPB) failure rates on leading semiconductor process nodes. These projected trajectories may be affected by alternative scan loading methodologies using high speed IO, redundant multi-core systems and the adoption of inline diagnostics. In addition to the test data increases which we are projecting, the team has been observing a category of "system level" faults in

digital systems that are not caught by BIST or traditional coverage techniques. Since these faults could lead to a negative user experience, some product companies are augmenting traditional test coverage with a System Level Test insertion, or crafting System Level Tests at ATE wafer/package test. This group will continue to monitor future areas of growth and adjust the roadmap as they become generally accepted methodologies.