HETEROGENEOUS INTEGRATION ROADMAP

2019 Edition

Chapter 17: Test Technology

Section 11: 2.5D and 3D Device Testing

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Section 11: 2.5D & 3D Device Testing

This section will address six key test challenges, based on the evolution of 2.5D/3D, from complex die stacks through SiP. These test challenges include: test flows, cost and resources; test access; testing heterogeneous die individually and in a single stack/package; debug and diagnosis of failing stacks/die; DfX (Design for Test, Yield, Cost); and power. It is important to note that 2.5D/3D is not yet a mature and mainstream technology, and, because of that, it is difficult at this time to make any predictions regarding 2.5D/3D test flows. 2.5D and 3D technologies are characteristic of a system, and because of that, should be tested like a system: testing the complete package at an application level and diagnosing failures at the die and interconnect level.

Memory die stacks (Wide I/O, High Bandwidth Memory and Hybrid Memory Cube) were precursors to 2.5D and 3D. Both of these technologies have provided insights to requirements and challenges associated with 3D and 2.5D test. The best that can be gleaned from these technologies at this time is that reliance on BIST and boundary-scan based technologies, and use of fault tolerance with simple configurations, tends to produce relatively high yields at the stack level. As these adjacent technologies become more mature and as more 2.5D/3D-TSV applications emerge, more and better data will enable better predictions and decision making, with respect to 2.5D/3D-TSV test processes.

Executive Summary

2.5D and 3D/TSV are the next evolution beyond SiP/SoC. There have been significant advances from both academics (research) and industry (standards and working models/test chips) to identify and resolve challenges to testing 3D/TSV devices. In the medium to long term, as TSV-based die stacking becomes more prevalent and more complex/exotic die stacks appear, test challenges will also become more difficult. It is certain that new and additional Design-For-Test features will be needed to mitigate increased tester resource and time requirements, as well as increased test complexity, due to large numbers of different die in the same package. This section will discuss challenges for testing, including cost (dollars, resources and yields); design for test; test access; debug and diagnosis; and heterogeneous device testing.

Difficult Challenges for Test: 5 years

While the current state of 2.5D/3D seems to be maturing, new enabling and supporting technologies will require advances in test access, capabilities and costs. These emerging technologies will provide significant challenges for testing 2.5D and 3D technologies, in addition to supportive technologies. The challenges below represent potential impacts to test, including increased costs, test times, and reduced yields and reliability.

2.5D Test Challenges (Short Term)

- **Known Good Die Test**: While logic blocks in the die can be partitioned and effectively tested, testing interactions between the logic blocks requires an application-based test.
- **System level test/diagnosis/repair**: Emulating a system-level test environment can be considerably costly and time consuming. Complex integration can produce new and challenging defects for test.
- **Access to the individual die in the 2.5D assembly**: Access may include multiple protocols: IEEE-1149 based (including IEEE 1687.1 and IEEE P1838 proposed standards), photonics, various component and system-level protocols, including I2C and SPI.
- **Interposer testing**: Point to Point testing can be accomplished primarily by probing (see the probing section). Multipoint interposer testing requires significantly more probing (more time and higher costs) and requires embedded logic to coordinate point-to-multipoint connections. Academic research from Duke University[1] has proposed solutions to point-to-multipoint connections on the interposer.
- **High speed interconnects (photonics)/signal integrity**: while testing photonics interconnects is mature, the cost of test is significant, primarily due to equipment and knowledge.
- **Discrete components**: more specific to high speed interconnects through the interposer. Point to point, high speed interconnects may compromise probe-based connectivity test.
- **Impact of emerging technologies with respect to test**: New technologies can impose new defects on the 2.5D. A table presented by Li Li at ECTC describes the relationship to the new technologies (Die thinning, TSV, C2C connection, BS-RDL, micro-bumps, Large volume of copper, increased power density and large thermal gradients, removal of IO structure) and the failure/defect mechanisms. See Table 1 below.

- **Innovations in Wafer Level Packaging/Wafer Level Fan Out**: similar to the statements above: advances in Wafer Level Packaging open the door for new defects and new requirements for test. Aspects of wafer level packaging impinge on interposer technologies.

3D Test Challenges (Short Term)

- **Known Good Die test**: Known good die testing becomes more important in a stack integration, where a defective logic die could compromise the entire die stack. System/application level testing at the die level has significant challenges. Significant Design-for-Test and Built-in Self-Test features are required to complement and simplify system/application level test. Cost of test ($$ and time) are significant.
- **System level test/diagnosis/repair**: System and application level test of a 3D die stack may require significant test/tester resources in order to emulate the component/test environment. These resources may consume significant time and money.
- **Diagnosis of system level failures** on the stack will have significant challenges. On a positive note, a diagnostic die may be added to the stack without significant effort. Redundant die may help as well.
- **TSV/interconnect testing**: TSV testing can be done pre-bond, microvoid and pinhole defects. Mid-bond testing becomes quite challenging. Some probing could help. A boundary-scan stack architecture may be a possibility. An IEEE standard is in the works (IEEE P1838 – this will be covered later as part of "technical issues"). Application and/or system test most likely will not be feasible or practical with part of the stack still missing. Test results may not be informative.
- **Probing 3D die stacks**: This area seems to be maturing. Companies like Tezzaron have probing figured out, since microbumps also seem to be maturing.
- **Stack repair**: While stack repair is now possible, cost for stack repair and re-test would be prohibitive. Redundant die may simplify stack repair.
- **High speed signaling/signal integrity/interconnects**: Signal integrity measurements from die to die are challenging. Design for Signal Integrity Test, at the edge of the die, may be a solution for SI measurement. Costs could be significant at the die level and higher at the stack level. There may be impact to stack level power.
- **KGD/KGS**: Known Good Die is critical from a supply chain perspective. Known Good Stack also requires a stack level system/application test.
- **Wafer Level Packaging** – uncertain if there will be an impact to test.

Difficult Challenges for Test: 10, 15, 25 years

Over the next 10 to 25 years, it is expected that requirements for speed and power will be significantly higher than the current state. Significant advancement to the integration of massive, high performance, low power die will be required for the future versions of application specific integrated devices. Test will be significantly challenged.

2.5D Test Challenges (Long term)

- **Known Good Die Test**: From ITRS predictions, the number of flops per KGD are significantly higher (exponential) over time. Speed, power and thermal scale with logic. Device cooling during test will become critical. Timing may be an issue through the stack. Test time may be significant.
- **System level test/diagnosis/repair**: System test requires higher speeds. Longer test times due to significantly more logic in the die. IEEE 1149 protocols will be obsolete or antiquated at best. Optical protocols using IEEE P1838 test access protocols will replace current test protocols.
- **Access to the 2.5D assembly**: Photonic protocols, more in line with P1838. Protocol objective is access to interposer of multiple-die stacks. Multiple-die stacks create a significant, interconnected logic pool.
- **Interposer testing**: Testing becomes logic based. Probing becomes more challenging, from Point-to-Point to Large Multipoint.
- **Cost of test** (equipment/resources/time): Cost of test increases as high-speed interconnects pass through the optical interposer. Signal integrity adds cost and time.
- **Testing MEMS- and Sensor-based die**: technology is somewhat analog. Testing is not conventional and requires an active motion, light, sound source. Significant setup and test times while income/prices are low and volumes are extremely high.

3D Test Challenges (Long term)

- **Known Good Die(s):** similar to the 2.5D section, logic per die is increasing over time. Speed, power and thermal are scaling with increasing logic/flops. Heterogeneous die become more and more exotic, making test more challenging, and determining when the die becomes "known good".
- **System level test/diagnosis/repair**: Test equipment cost increases significantly with respect to dollars and time. High speed signaling increases test costs and the possibility for errors/failures. Potential impact on the supply chain.
- **Carbon Nanotubes** replace TSV, CNT test replaces TSV Test: Carbon nanotubes help to sustain logic, speed, power, thermal characteristics. CNT is still academic; however, more prognostication exists for short- to mid-term replacement of TSVs with Carbon Nanotubes. External interfaces convert protocols to CNT interface.
- **Mega Stack testing**: Mega Stacks address the need for high performance data processing. Stacking multiple die becomes feasible as advances in die to die bonding minimize the stack size, while adding more die to the stack. Future Mega stacks may potentially have the same structural integrity as initial die stacks. Multiple redundant die may be necessary for more probable defective die in the stack, or mis-connections between die in the stack.
- **Probing die and stacks**: Advanced Probing technology will be needed as TSVs and micro-bumps become significantly smaller.
- **Stack repair**: Primary repair will come from redundant die. Dis-assembly of the die stack becomes significantly challenging and could potentially destroy the pre-bonded die.
- **Testing MEMS- and Sensor-based die**: technology is somewhat analog. Testing is not conventional and requires an active motion, light, sound source. Significant setup and test times while income/prices are low and volumes are extremely high.

Discussion of Key 3D Test Technical Issues

Future of 3D Integration (Test and DfT focus, Academic Perspective)

The semiconductor industry has been able to meet the demand for high-performance integrated circuits (ICs) with added functionality by relentlessly scaling device sizes. However, it is becoming increasingly difficult to sustain device scaling in an economically viable manner.

A promising way to achieve high-performance ICs with more functionality and reduced die footprint is through 3D integration. Today's 3D integration process is primarily based on die/wafer stacking, as it does not require substantial changes to the existing fabrication flow. In this process, separately manufactured dies/wafers are integrated onto the same package, and through-silicon-vias (TSVs) are used to connect dies to each other. Considerable research efforts have therefore been directed toward the development of TSV-based 3D stacking technology, and products based on this technology have been successfully introduced into the market, e.g., the AMD Fiji chip. However, the keep-out-zone (KOZ) required for TSVs and limitations on the die alignment precision impose limits on the device integration density that can be achieved using TSV-based 3D stacking. A minimum KOZ of 3 μm is required for ICs fabricated at the 20 nm technology node [Kannan et al. 2015], and the die alignment precision is currently limited to 0.5μm.

Monolithic three-dimensional (M3D) integration is receiving considerable interest as a technology for the future, as it has the potential to achieve higher device density compared to TSV-based 3D stacking. In this technology, transistors are processed layer by layer on the same wafer. Sequential integration of transistor layers enables high-density vertical interconnects, known as the interlayer vias (ILVs). Typically, the size and pitch of an ILV is one to two orders of magnitude smaller than those of a TSV [Batude et al. 2012]. To realize such high-density vertical interconnects, the interlayer dielectric (ILD) thickness is being aggressively scaled [Batude et al. 2012; Lee and Lim 2013], and such scaling has been shown to lead to electrostatic coupling between device layers. This is a challenge for test researchers.

Researchers have recently analyzed electrostatic coupling between device layers in M3D ICs and quantified its impact on circuit timing [Koneru 2017]. Device simulations have been carried out to understand the impact of coupling on the threshold voltage of a top-layer transistor for both transistor- and gate-level integration. To realize a new silicon layer over the bottom layer without damaging the underlying interconnects and degrading the properties

of the bottom-layer transistors, several layer-transfer techniques are being explored [Batude et al. 2015; Ishihara et al. 2012].

Low-temperature wafer bonding is a key processing step in these techniques. The condition of the bonding surfaces plays a crucial role in achieving a defect-free bond. Oxide layers are the prime candidates for bonding surfaces due to the presence of hydroxyl (OH) groups that lead to high bond strengths. These oxide layers also act as the ILD. Therefore, defects that arise during the wafer-bonding step can impact the top-layer transistors, as well as the ILVs. It is important to understand and analyze wafer-bonding defects, and develop methods to test for these defects. Research is needed to study the impact of bond defects on the threshold voltage of a top-layer transistor and on the ILVs. In addition, advances in test access and debug/diagnosis for M3D will also be of growing interest as this technology advances.

It has been shown thus far that the impact of coupling and wafer-bonding defects on the threshold voltage of a top-layer transistor is significant, and cannot be ignored, when thickness of the ILD is less than 100 nm. In such scenarios, the paths through the top layer in a gate-level-integrated M3D IC can change depending on the size of the defect and the voltage on the metal lines in the bottom layer. The presence of defects at the bond interface can lead to a change in resistance of an ILV and in some cases lead to an open in the ILV or a short between two ILVs. A resistive open in an ILV or a resistive short between two ILVs can have a significant impact on the path delays. Due to these challenges, existing test-generation methods for small-delay defects are of limited effectiveness when the ILD is less than 100nm.

There is also a paper which includes a discussion regarding supply-chain capability requirements for test and reliability: see [Alfano].

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