HETEROGENEOUS INTEGRATION ROADMAP

2019 Edition

Chapter 17: Test Technology

Section 13: Test and Yield Learning

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Section 13: Test and Yield Learning

In the normal sorting function, test provides the essential feedback loop for yield-learning. Product-based diagnostics, product-like test chips and parametric-sensitive test structures all play a key role.

Key Cost of Test Trends

Value derived from diagnostics of actual product hardware is driven by systematic defect mechanisms that are now increasingly complex functions of neighboring shapes, local pattern densities, etc. As a result, some failure mechanisms may be visible only on product. In addition, product-based diagnostics automatically places focus on key yield-limiting failure mechanisms. Volume-based diagnostics are important since individual occurrence of any given systematic defect mechanism may be rare. The pooling of data across many failing die can be important to identify true systematic defect mechanisms.

Product-like test chips can provide some of the same insight for yield-learning, but have the advantage of being available earlier, even when design is on-going. Specifically, rapidly designable, scalable and 100% testable & diagnosable test chips, with and without embedded memory and other key IP blocks, including fast automated design methodologies, are required to accelerate yield ramps and first-time yield success of complex SOCs. Such test chips should play the role of "send-aheads" and be designed on early foundry testsites even while the product design is ongoing. The test chip should be scalable, in that a complete SOC-style (optionally, timing-closed) design is possible with tens or hundreds of standard cells and with a small or large compiled memory and other IP blocks. The test chip should enable both logical and physical layout diversity in order to capture layout topologies found on real product chips. Finally, the test chip must be able to maintain a stable test and diagnosis infrastructure, meaning the same set of ATPG, diagnosis and failure analysis capabilities should be enabled whether the test chip is tiny ($<1mm^2$) or huge ($>100mm^2$).

In addition, parametric-related feedback is needed for (1) device and interconnect parameters and (2) design-process interactions. Measurement of device and interconnect parameters have traditionally relied upon test structures, especially scribe-line FETs and interconnect resistance and capacitance monitors. Increasing across-chip variation (intra-die variability) increases the negative impact of scribe-line-to-chip offsets. Moreover, test structures are limited by the number of configurations they can cover. Variations in configurations include both physical variations and electrical variations, such as different gate types and differences in load characteristics. As circuit parametrics are increasingly affected by such configurations, including within-standard-cell and transistor-layout configurations, it becomes necessary to base learning on product test or test of product-like layout configurations. Embedded, distributed monitor circuits such as thermal and VDD sensors, process-monitoring ring oscillators and critical path proxies are now standard on microprocessor-class ICs and can be used to help diagnose parametric fails and understand variability. Understanding variability includes unraveling the structure of variations into spatial and cross-parameter components (variation in transistor length, V_t, source-drain resistance, etc.) The spatial component includes both die-to-die and within-die components.

Cross-parameter variations, potentially including a spatial component, are important to analog/RF circuits, as well as digital. Methods for understanding/characterizing the manufacturing process and operating environment that are sufficiently sensitive for analog/RF are needed. Moreover, product test is uniquely well-suited to provide feedback on design-process interactions, including those leading to noise-related fails, such as power-grid droop and crosstalk fails.

Top challenges for test-based yield-learning include:

- Better resolution for cell-internal defects. Latest advances in structural testing and scan-based logic/layout-aware diagnosis methods are adequately addressing interconnect and via defects. Statistical approaches built into volume-based diagnostics are able to predict interconnect-related defect modes without an over-dependence on Physical Failure Analysis (PFA). Innovation is required, however, for cell-internal-defect-targeted diagnostics to be able to identify systematic fail modes inside standard cells. Observations derived from production silicon suggest a shift toward a larger percentage of the defect distribution being cell-internal defects, as opposed to interconnect-related. Current best methods for cell-internal defect diagnostics are cell truth-table and gate-exhaustive model-based, with the truth tables established via SPICE simulations of modeled cell-internal parasitics. These methods suffer from aliasing issues and over-reliance on potentially inaccurate modeling of cell-internal defects used in SPICE simulations. In addition, diagnosis resolution needs to be better due to limitations in the PFA process.

- Managing design data for yield learning. A tremendous amount of design data can be brought to bear for yield learning purposes, but it is often not organized effectively for this purpose. In addition, with hierarchical design and DFT flows, the overall management of this data at most companies today is ad-hoc, limiting its effective use.
- Inadequacy of LEF/DEF as the basis of layout-aware diagnosis. LEF/DEF suffices for the purposes of layout-aware ATPG but is too early in the design cycle to be used effectively for layout-aware diagnosis. LEF/DEF is less likely to closely resemble the final mask shapes due to complex OPC, boolean and retargeting steps.
- Yield-Learning in an OSAT/Fabless/Foundry environment. Yield-learning capabilities must be cognizant of the environment that has become the dominant model for our industry. If the technology cannot deal with the security and logistical concerns of this environment, it cannot be effective. Factory integration issues must be addressed. Data capture and management capabilities must support increasing reliance on statistical analysis and data mining of volume production data for yield-learning. Secure mechanisms for yield-data flow for distributed design, manufacture and test, including fabless/foundry and 3rd party IP, are needed. Standard test data formats, such as STDF-V4-2007 for scan fail data, and infrastructure to support their transmittal are needed to support automation and sharing of data. Specifically, data exchange standards are needed between the Fabless and the OSAT/Foundries to share system-level test feedback and correlation to wafer-level test and measurement data to (1) improve IC quality and reliability, (2) correlate process variations and parametric variability, and (3) reduce overkill. Distributed design, manufacture and test also creates an emerging role for methodologies and tools to help determine which areas that problems reside, e.g., design house, foundry or OSAT.
- Test for ZERO DPPM/Automotive in advanced node technologies. A change of mindset away from structural test coverage only is required to guarantee functional safety for automotive ICs. Mission-mode in-situ MBIST and LBIST and Design Failure Mode and Effects Analysis [DFMEA] are already part of ISO26262 (an automotive-specific set of standards for designing and testing electronics that focuses on safety critical components), but test architecture research is required to minimize the die-footprint increase due to added circuit redundancy. Moreover, Automotive may require root cause reports to be produced quickly for field failures. This requirement is another driver for rapid diagnosis and root cause analysis.
- Test and data-collection time increases due to longer scan chains. These increases drive a need for focus on LBIST methodologies and scan compression for both test and diagnosis.
- Faster Memory BIST bitmapping.
- Guidance for trading off test and data collection time against improved failure diagnostics.