HETEROGENEOUS INTEGRATION ROADMAP

2019 Edition

Chapter 17: Test Technology

Section 14: Cost of Test

http://eps.ieee.org/hir

The HIR is devised and intended for technology assessment only and is without regard to any commercial considerations pertaining to individual products or equipment.

We acknowledge with gratitude the use of material and figures in this Roadmap that are excerpted from original sources. Figures & tables should be re-used only with the permission of the original source.

IEEE ELECTRONICS PACKAGING SOCIETY · ELECTRON DEVICES SOCIETY · IEEE Photonics Society · ASME SETTING THE STANDARD · semi

Section 14: Cost of Test

Minimizing costs are a key part of the semiconductor manufacturing process. Test is no exception, although steady improvements in efficiencies over the last 15 years have lowered the typical cost of test as a percentage of IC revenue to less than 2-3%. The primary drivers of increased efficiency have been reductions in capital costs per resource and test times, coupled with increases in parallelism and Built-In Self-Test (BIST) capability. Most SOC device are tested 2 to 16 at a time, and memory devices can have more than 1,000 devices tested at once. Measured as the cost to use capital equipment for test (in terms of cost per hour per device), these decreases in test cost will continue at a relatively consistent rate per year. The figure below shows the historical rate of capital investment in test, interface (consumables) and handling equipment.

It is notable that, in 2015 for the first time, the cost of consumable material has become the leading capital expenditure relative to ATE-based test. This has to do with the increased cost of interface material (primarily influenced by probe cards and relative items) and the decreasing depreciation period for materials utilized for the production of devices used in the mobile device space where devices have a shorter life span. In this case, material is typically discarded not because it has ceased to function, but rather because the devices it is used to test are replaced by newer versions for end devices like mobile phones.

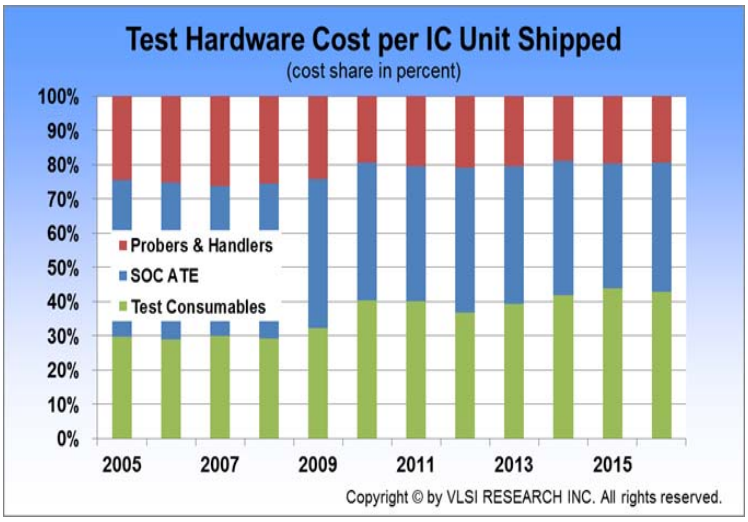

Figure 1: Test Costs as a percentage of device ASP (Used by permission of VLSI Research)

Key Cost of Test Trends

Looking forward, there are several trends which will counterbalance equipment efficiency and serve to cause cost increases:

- Increases in transistor count that outstrip compression technology will increase the amount of external data which must be supplied to the Device Under Test (DUT). Coupled with scan shift rates that are limited by power and thermal concerns, the overall effect will be longer test times. This will be addressed primarily with increased parallelism.
- Device configuration and one-time programming during test is causing more time to be spent during test to perform initial device calibrations or to reconfigure devices based on defects or electrical performance. As silicon geometries shrink and defect densities drive circuit redundancy, repair functions will also add to test costs.
- The eventual drive to multi-die packages will add a requirement for more System Level ("mission mode") testing owing to lack of access to individual die. Without significant Design For Test (DFT) improvements, this type of testing can take much longer than conventional structural test. This will also drive more exhaustive test processes at wafer probe in order to improve the yield of multi-die packages.
- Site count increases at probe test are not able to increase owing to the attendant increase in the cost of consumable material (discussed above) and the limitations of Touch-Down Efficiency (TDE). This is discussed in more detail below.

- An increasing reluctance on the part of IC manufacturers to dedicate silicon area and power to circuitry used exclusively for test.
- The continuing increase of silicon content in automotive applications, especially for safety systems, which drives additional test insertions for fault coverage and temperature-related test.

Even though continuous improvement in equipment efficiency will be offset by new device test requirements, the overall cost of test will continue to decrease. The major contributors to that cost are described below.

Cost of Test as a Part of Overall Manufacturing Cost

While the cost to own and operate test equipment has been reducing, other semiconductor manufacturing costs have been significantly increasing with new silicon technology. Specifically, fab costs for leading-edge processes have increased to about 70-80% of the overall cost of producing a large-scale SOC device. It now costs far more to fab a device than to test it, and that trend will accelerate as new fabrication technologies are deployed.

The figure below represents third-party analysis of the capital and service costs of equipment used in device fabrication, packaging and test.

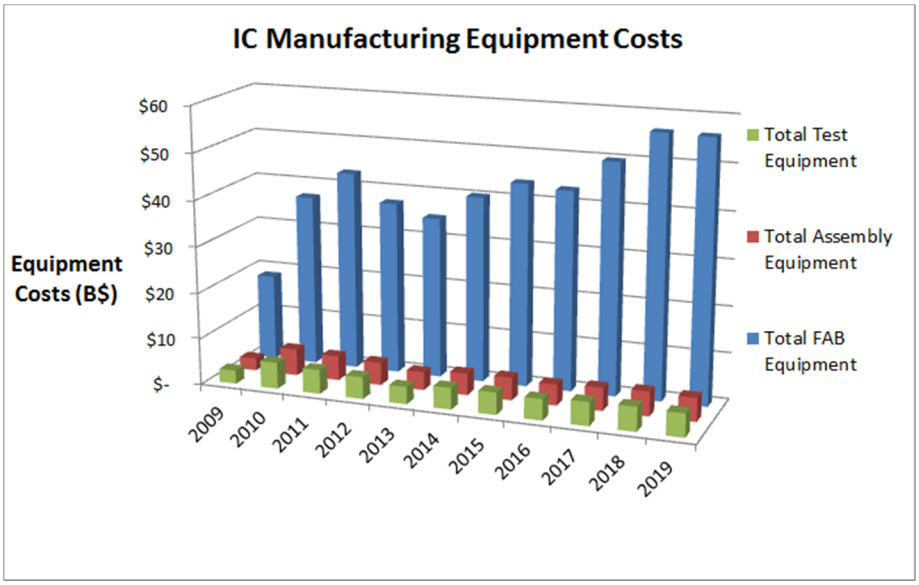

Figure 2: Relative cost of Fab, Packaging and Test Equipment

While it is helpful to focus on the cost of test itself, the overall contribution to a manufacturer's profitability from lower test costs will be very small since test is a small part of the device cost overall. The highest avoidable costs in test are devices that are good but are rejected at test for some reason.

Consider the following, simplified example.

- A device costs $1.00 to manufacture, including Fabrication, packaging, etc.
- Test constitutes 5% of that cost, or $0.05

Reducing the cost of test by 10%, will reduce overall costs by $0.05 X 10% = $0.005 per device

Improving yield by 1% reduces overall cost by $1.00 * 1% = $0.01 per device

While the 10% Cost of Test reduction is good, the yield improvement is better.

The figure below shows the effect on cost of test of traditional cost reduction techniques:

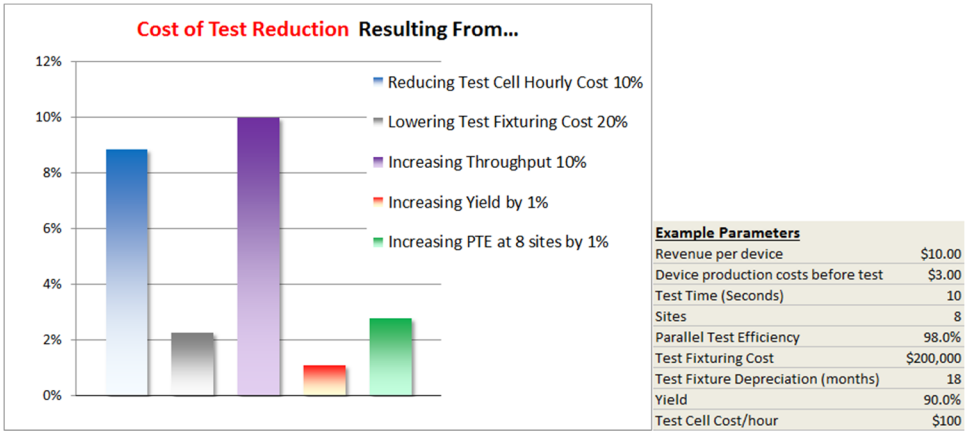

Figure 3: Cost of Test Reduction realized by traditional cost reduction techniques

If one considers the effect on total manufacturing costs, including the cost to scrap devices that are actually good, the cost savings due to improved yield becomes far more significant.

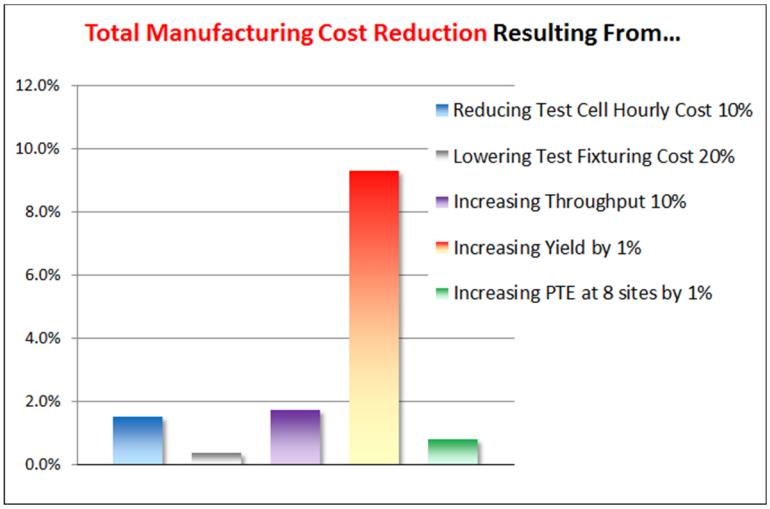

Figure 4: Total Cost of Manufacturing Reduction realized by traditional cost reduction techniques

The risk of yield loss is increasing over time for several reasons:

- Trends such as the reduction of power supply voltages and more complex RF modulation standards will drive higher accuracy requirements for test equipment. Test equipment accuracy is typically added as a "guardband" in testing, reducing the range of acceptable measurements. If measured DC and AC values become smaller and there is no improvement in test accuracy, this guardband will cause more marginal (but good) devices to be scrapped.
- As noted earlier, many devices, especially for mobile applications, require some sort of calibration or trim during the test process to improve DC and AC accuracy. This dramatically increases both the number of measurements made and the accuracy required of the test equipment. The requirements increase the chance of discarding devices that would otherwise have been good.
- Faster production ramps and short IC product life cycles will reduce the amount of time available to optimize measurements for the majority of devices produced.

The remainder of this section will examine Costs associated with owning and operating test equipment. It must be stressed that reducing these costs must be done in the context of the overall cost to produce devices and balance reduction in test costs with potential reductions in product yield.

Test Cost Models and Cost Improvement Techniques

The cost of semiconductor test has many drivers, which is further complicated for multi-die SiP precuts as shown in Figure 5.

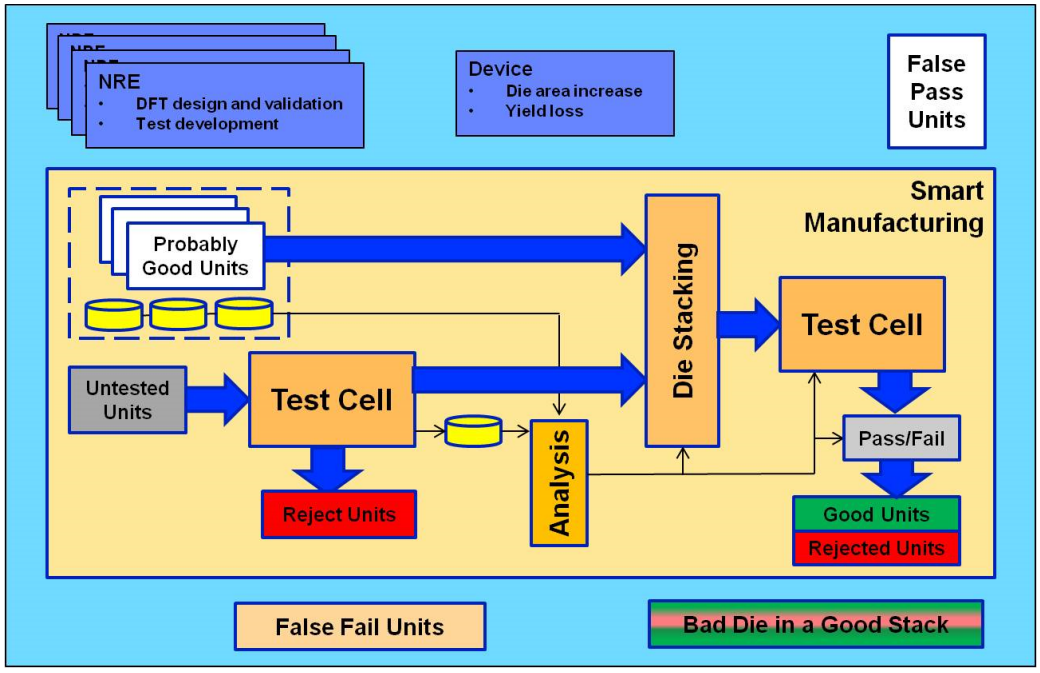

Figure 5: Multi-die Flow

Current Top Cost Drivers

The traditional drivers of Test Costs typically include (In rough order of impact to Cost)

- Device Yield
- Test Time, site count and Parallel Test Efficiency (PTE)
- Overall Equipment Utilization
- ATE Capital & Interface Expenditures
- Facility/Labor costs
- Cost of Test Program Development
- Cost of die space used for Test-only functions

Future Cost Drivers

- Increased test time due to larger scan patterns
- Increased testing at wafer to produce Known Good Die (KGD)
- Addition of system-level testing
- Increased cost of handling equipment to support high site count or singulated die
- Increasing use of device calibration/trimming at test or device repair with redundant components

Currently Deployed Cost Reduction Techniques

- Multi-site & reduced pin-count
- Structural Test and Scan
- Compression/BIST/DFT and BOST
- Yield Learning & Adaptive Test
- Concurrent Test
- Wafer-level at-speed testing

Cost Reduction Techniques that may be Deployed in the Future

- Advanced embedded instruments
- New contacting technologies
- In-system level testing to detect latent defects and potentially repair
- Built-in fault-tolerance

Multi-site Trend

As discussed in the previous sections, the most important way to reduce cost of test is increasing the number of sites. The effectiveness of increasing the number of sites is limited by (1) a high interface cost, (2) a high channel and/or power cost, and (3) a low multi-site efficiency M:

$$M = 1 - \frac{(T_N - T_1)}{(N-1)T_1}$$

where N is the number of devices tested in parallel (N>1), T_1 is the test-time for testing one device, and T_N is the test time for testing N devices in parallel. For example, a device with a test time T_1 of 10 seconds tested using N=32 sites in T_N =16 seconds has a multi-site efficiency of 98.06%. Hence, for each additional device tested in parallel there is an overhead of (1-M) = 1.94%.

Typical site counts for various device types are shown in the ITRS "Site Count Table 2017". We also looked at the roadmap plans from 2013 and compared them to 2017 ("Site Count Comparison 2013 to 2017"). This clearly shows how increased device complexity as well as device interface complexity and costs have constrained efforts to expand site counts as quickly as desired.

Minimizing costs are a key part of the semiconductor manufacturing process. Test is no exception, although steady improvements in efficiencies over the last 15 years have lowered the typical cost of test as a percentage of IC revenue to less than 2-3%. The primary drivers of increased efficiency have been reductions in capital costs per resource and test times, coupled with increases in parallelism and Built-In Self-Test (BIST) capability. Most SOC devices are tested 2 to 16 at a time, and memory devices can have more than 1,000 devices tested at once. Measured as the cost to use capital equipment for test (in terms of cost per hour per device), these decreases in test cost will continue at a relatively consistent rate per year. The figure below shows the historical rate of capital investment in test, interface (consumables) and handling equipment.

It is notable that, in 2016, for the first time, the cost of consumable material had become the leading capital expenditure relative to ATE-based test. This has to do with the increased cost of interface material (primarily influenced by probe cards and relative items) and the decreasing depreciation period for materials utilized for the production of devices used in the mobile device space where devices have a shorter life span. In this case, material is typically discarded not because it has ceased to function, but rather because the devices it is used to test are replaced by newer versions.

Figure 6: Importance of Multi-Site Efficiency in Massive Parallel Test

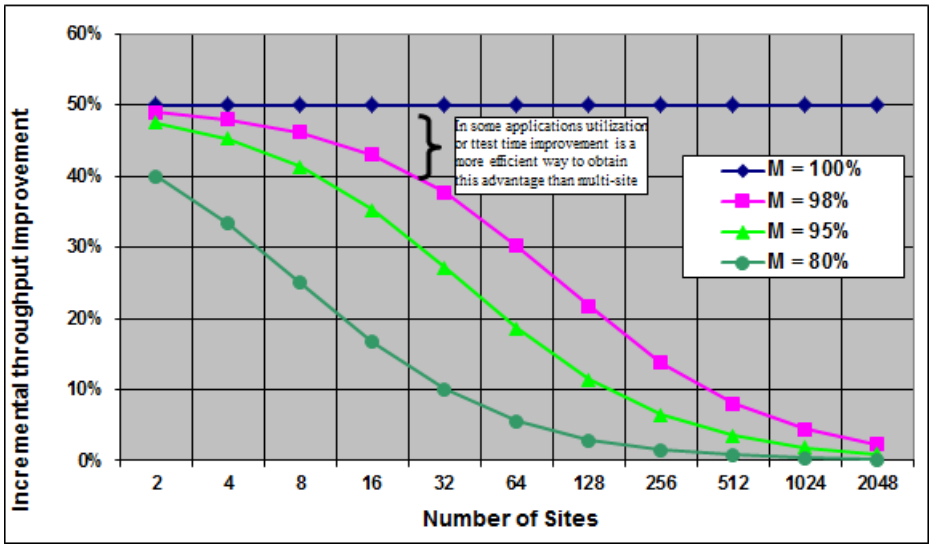

Table 1: Multi-site Test for Product Segments

		2018	2019	2020	2021	2026	2030	Drivers
High Performance MPU, ASIC (1)								
Wafer test	Number of sites	8	8	8	8	8	8	
Package test	Number of sites	16	16	16	16	16		MPU
SoC (2)								
Wafer test	Number of sites	8	8	8	16	32	32	SoC
Package test	Number of sites	16	16	16	32	64		SoC
Low Performance - MCU, MPU, ASIC (3)								
Wafer test	Number of sites	64	64	128	128	256	256	MCU
Package test	Number of sites	16	16	32	32	64	64	MCU
Mixed-signal, & Communications								
Wafer test	Number of sites	16	16	16	16	32	32	Mixed
Packaged Test	Number of sites	16	16	16	16	32	32	Mixed
DRAM Memory								
Wafer test [note 4]	Number of sites	3000	3000	3000	3000	3000	3000	DRAM
Packaged Test	Number of sites	1024	2048	2048	2048	2048		DRAM
At Speed DRAM Memory								
Wafer Test Parallelism	Number of sites	128	128	128	128	128	128	DRAM
3D Stacked Memory (Wide I/O, HBM, HMC)								
Wafer test	Number of sites	3000	3000	3000	3000	3000	3000	DRAM
Packaged Test	Number of sites	1024	2048	2048	2048	2048		DRAM
Commodity Flash Memory (NAND)								
Wafer test	Number of sites	2048	2048	2048	2048	2048		NAND
Packaged Test	Number of sites	2048	2048	2048	2048	2048		NAND
Stack test [note 6]	Number of sites	4	4	4	4	4	4	NAND
LCD Driver								
Wafer test (Small panel) (5)	Number of sites	6	6	8	8	8	8	LCD
Wafer test (Large panel) (5)	Number of sites	12	12	16	16	16	16	LCD
RF								
Wafer & Packaged test [7]	Number of sites	**32**	**32**	**32**	**32**	64	64	RF
CIS								
Wafer test	Number of sites	64	96	96	128	256	512	CIS
MEMS - Inertial Sensor (Consumer)								
Wafer test	Number of sites	64	64	64	128	512	1024	MEMS
Final test	Number of sites	98	128	256	256	512	1024	MEMS
MEMS - Inertial Sensor (Automotive & Industrial)								
Wafer test	Number of sites	4	4	8	8	16	32	MEMS
Final test	Number of sites	8	8	8	8	16	32	MEMS
MEMS - Microphone								
Wafer test	Number of sites	16	16	16	32	64	128	MEMS
Final test	Number of sites	49	144	144	144	256	512	MEMS

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

Notes for Table 1:

1. Assumes I/O count of 250 for MPU and 1000 for ASIC
2. Assumes I/O count of 300
3. Assumes I/O count of 100
4. Wafer test uses Reduced Pin Interface
5. Assumes define Small panel as hand-held display application with one LCD device per each set and Large panel as TV display application with multiplex LCD devices per set
6. Engineering Testing
7. Maximum according to # active RF ports/device

As one continues to increase the number of sites, a low multi-site efficiency has a larger impact on the cost of test. For example, 98% efficiency is adequate for testing two and four sites. However, much higher efficiency is needed for testing 32 sites. At 98% efficiency, going from testing a single site to testing four sites will increase a 10s test time to 10.8s. However, going from testing a single site to testing 32 sites will increase a 10s test time to 16.4s, that is, significantly reducing the potential advantage of multi-site as shown in Figure 6. There are more efficient ways to reduce overall cost of test than going to the next setup with more sites in certain cases. Especially for high-mix, low-volume applications, there are many tester utilization challenges. In these setups, frequently, lower degrees of multi-site is preferable because test time improvement of techniques to improve utilization have a higher impact on the overall cost of test.

Touch-Down Efficiency (TDE) is defined as the number of wafer touch-downs required to test all devices on a wafer, relative to the theoretical minimum. TDE is influenced for the most part by the die size (and therefore the number of die per wafer) and the pattern used to probe. For example, if a device is tested 10 sites at a time, and there are 1,000 die per wafer, then ideally a probe card would have to touch down 100 times in order to tester the wafer and be 100% efficient. If, due to the mismatch between the round shape of the wafer and the linear or rectangular pattern of the probe card, the probe card must touch down 110 times to test the 1,000 devices, then the TDE is closer to 90%. This is shown in the figures below.

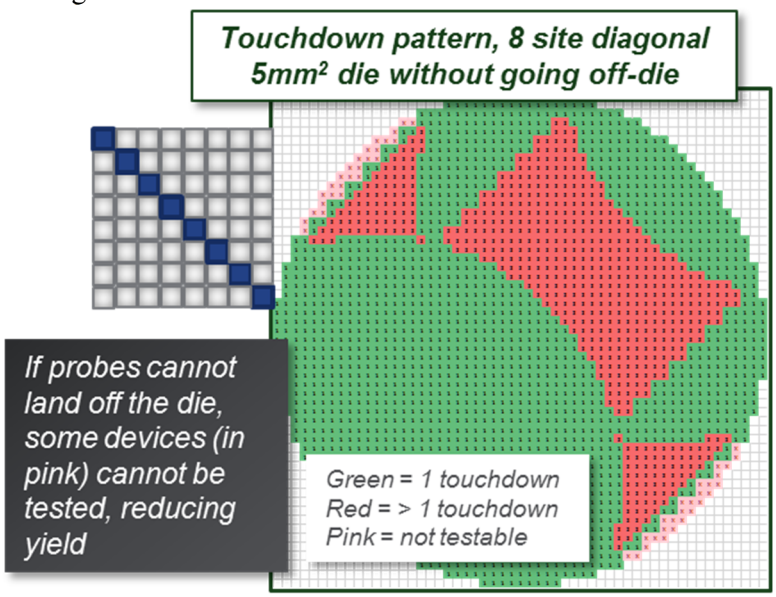

Figure 7: Probe Pattern of 5mm2 die using 8-site probe pattern

As die size of complex device increases, the TDE will continue to degrade as shown below in Figure 8. This degradation of efficiency will negate any advantages of increased site count and will eventually increase Cost of Test as shown in the example below. In this case, there are gaps in the probe pattern to allow for the inclusion of electrical components on the probe card required for the proper operation of the Device Under Test.

TDE inefficiencies will primarily be address by the development of singulated die testing technology. There is significant work underway to allow die to be reassembled in silicon panels that have a rectangular shape as opposed to the round shape of the original silicon wafer. The deployment of this technology will re-start the increase in site count at probe that is currently stalled due to interface costs and TDE limitations.

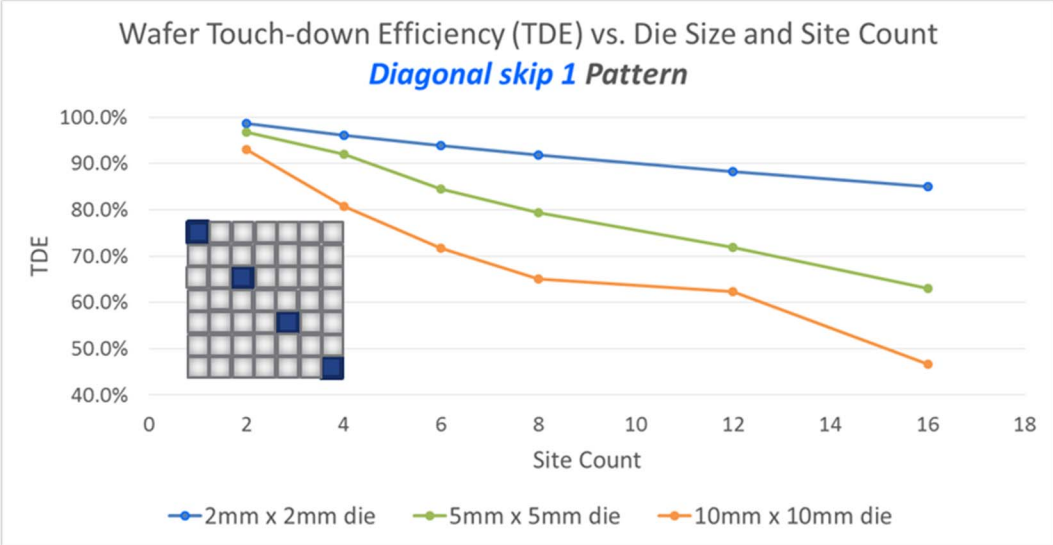

Figure 8: Touch-Down Efficiency as function of die size using a 4-site probe pattern

Summary

Major conclusions are:

- Cost of test has been declining for some time, but the rate of reduction has slowed down.
- Major reason for the slower rate of cost reduction are:
  - Packaging trends that drive more test at the wafer probe insertion where site counts are lower.
  - Increased cost of consumable material, which now dominates tester capital cost in terms of test cell costs.
  - Desire for higher yield, which has a much larger impact on overall device production costs than test costs alone.
  - Desire for higher device quality, especially for automotive applications, which necessitates more test.
- Potential solutions to decrease test costs are:
  - New probing technology which allows test of singulated die.
  - New PCB and Interposer technology to lower the cost and complexity of consumable material.
  - Factory automation.
  - Cost reduction of system-level testing.

Edited by Paul Wesling