HETEROGENEOUS INTEGRATION ROADMAP

2019 Edition

Chapter 20: Thermal

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Chapter 20: Thermal

1.0 Introduction and Scope

Heterogeneous Integration poses several significant challenges for thermal management at multiple length scales ranging from heat extraction from hot spots, heat transfer through multiple layers of materials, different target temperatures for specific devices/materials, to heat rejection to a system cooling solution or the ambient. This Thermal Working Group (TWG) will consider three areas for thermal management:

- Die level;
- Package integration/System-in-Package (SIP)/module level;
- System level (limited to board level).

In addition to the taxonomy of the physical categories listed above, this chapter will focus on articulating the following in quantitative (wherever possible) and qualitative terms:

- Canonical problems with thermal challenges;
- Cooling limits for known solutions;
- Advanced concepts and research.

2.0 Canonical Problems with Thermal Challenges

The canonical thermal problems and challenges presented in detail herein are:

- 2D chip with stacked memory on a silicon/glass interposer
- 3D stacked die with conduction interfaces
- 3D stacked die with embedded liquid cooling
- Optics/photonics-based heterogeneous package
- Harsh environment (military, aerospace, automobile)
- Mobile application chipset (package-on-package, fan-out, bridge)
- Voltage regulators in a heterogenous package

2.1 Thermal challenges in 2D Packages

Figure 1 shows the 2D enhanced architecture (2D-EA) as a part of the overall 2D-3D packaging taxonomy. It is divided between 2D Organic (2DO) and 2D (passive) Silicon (2DS), further divided between without and with through-silicon vias (TSVs).

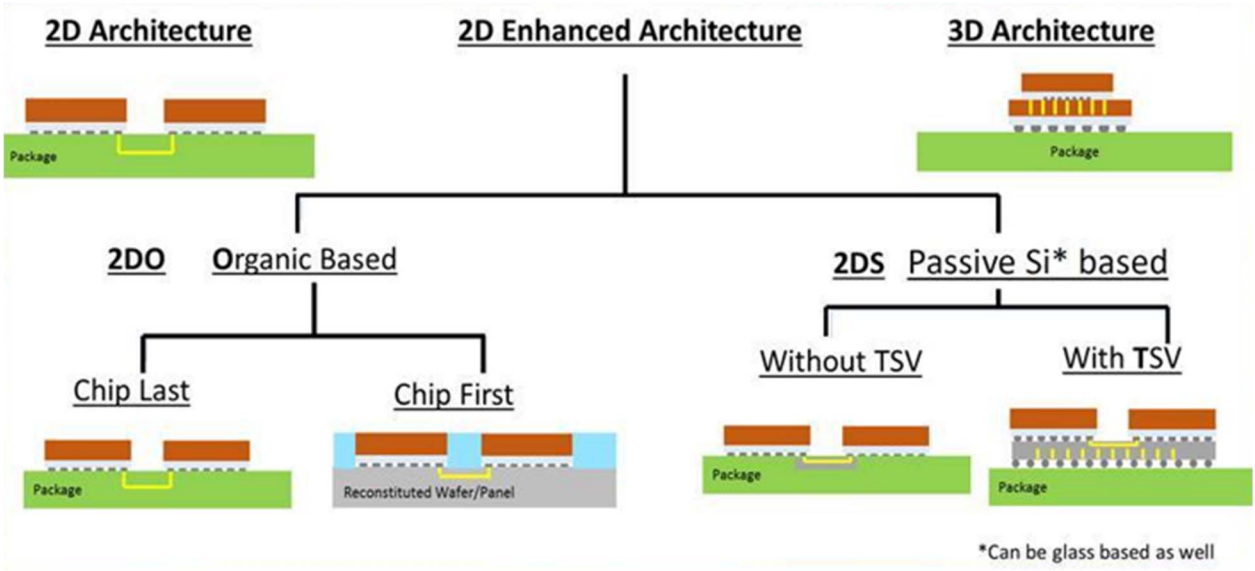

Figure 1: 2D-3D packaging taxonomy [1]

2D-EA is a side-by-side heterogeneous integration of two or more functional components (ASIC, FPGA, CPU, GPU, single or 3D-stacked memory, etc.) using an organic or inorganic interposer or an embedded high-density

interconnect-enabling connector (e.g. Embedded Multi-die Interconnect Bridge (EMIB[JYK1])), as shown in Figure 2.

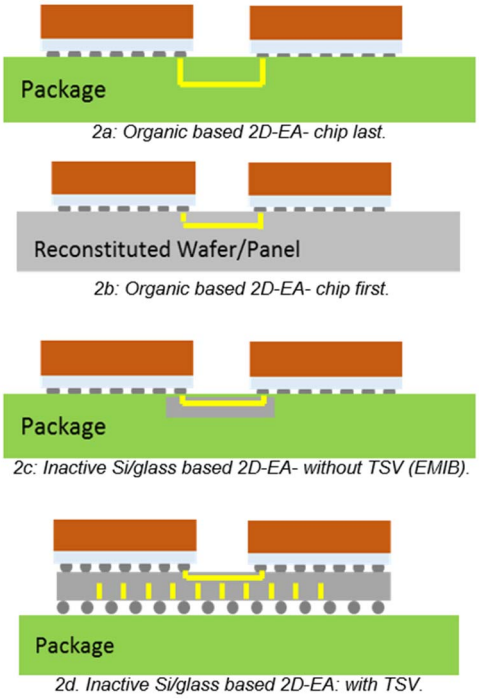

Figure 2: Schematic of 2D-EA [1]

In summary, the thermal challenges for the 2D heterogeneous-integrated packages are listed below:

- Increasing package power density;
- Increasing total package power dissipation;
- Thermal cross-talk, including the need for thermal isolation;
- Different thermal (Tj) requirements and sensitivities;
- Thermal interface material (TIM1 or TIM1.5) thermal insulance (K-mm2/W) uncertainty from increasing form factor and Si surface flatness and overall warpage impact;
- Thermo-mechanical enabling;
- Interposer thermal properties (glass/Si/organic) (see Figure 3) including anisotropy;
- Interposer thermal conductivity has a strong impact on chip thermal resistance;
- Glass and Si interposer performance can be made comparable, by appropriate enhancements;
- Interposer heat spreading and heat removal.

Figure 3 depicts several different cases that are analyzed, with the thermal results mapped in Figure 4.

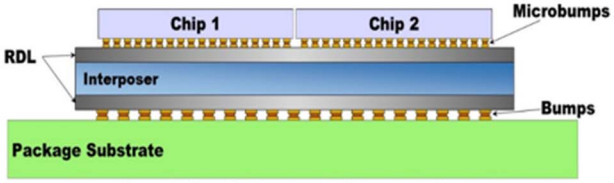

Figure 3a: Schematic for case 1.

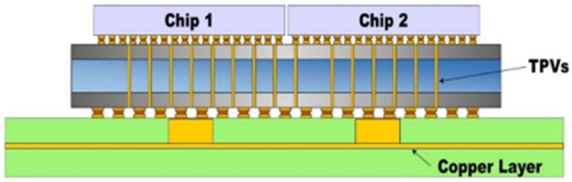

Figure 3b: Schematic for case 2.

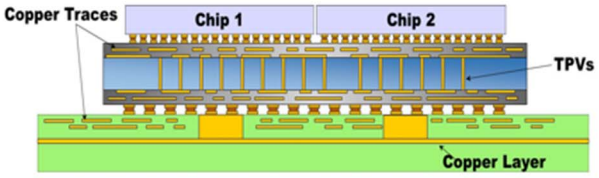

Figure 3c: Schematic for case 3.

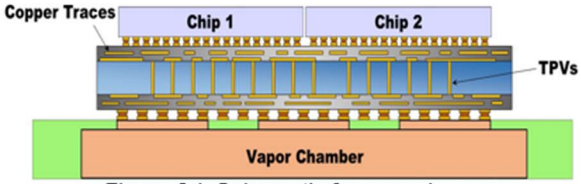

Figure 3d: Schematic for case 4.

Figure 3: Multiple different 2D configurations for thermal assessment [2]

Figure 4 displays the results from analyzing the cases 3a - 3d depicted in Figure 3 and illustrates the reduction in junction-to-case thermal resistance (K/W).

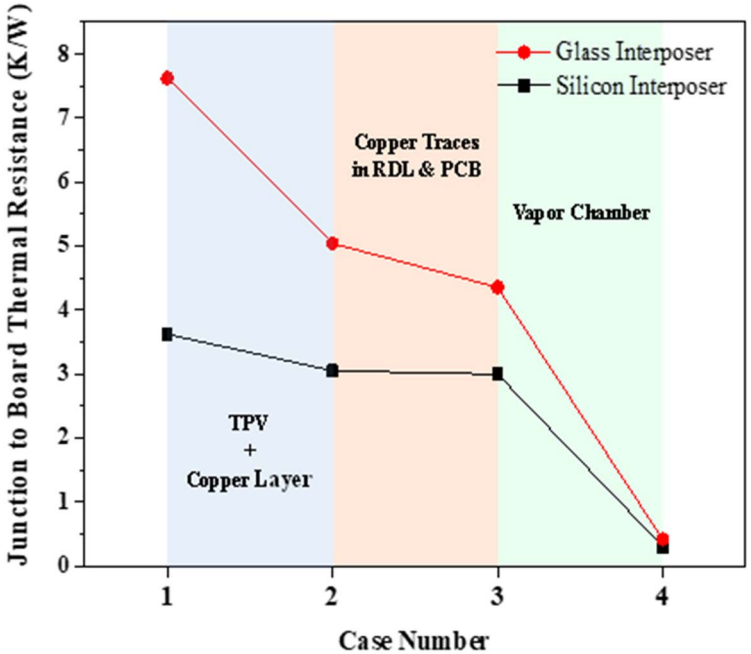

Figure 4: Impact of interposer and substrate thermal conductivity on package thermal resistance [2]

2.2 3D Stacked-Chip Packages with Conduction Interfaces

Thermal management is critical in the design of high-power 3D stacked-chip packages which enable high-bandwidth and low-latency communications. By stacking chips, as shown in Figure 5, the effective power density increases because the power generated in the 3D stack has to be dissipated over the "footprint" area of a single chip.

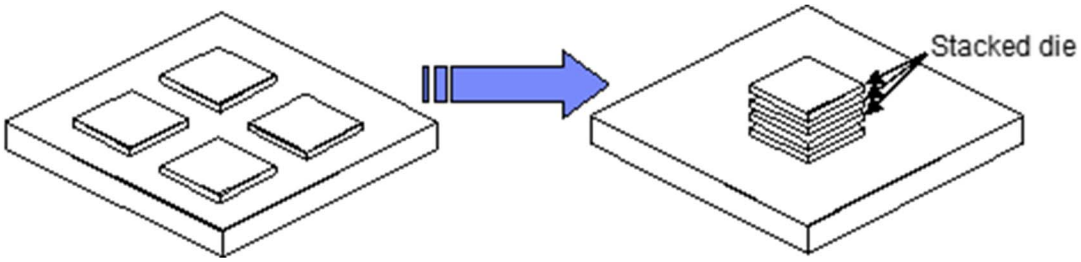

Figure 5. Effective power density increases in a 3D stacked package

In a high-power 2D package, shown in Figure 6, most of the heat generated in the chip conducts through a thermal interface material into a metal lid and then externally to a heat sink.

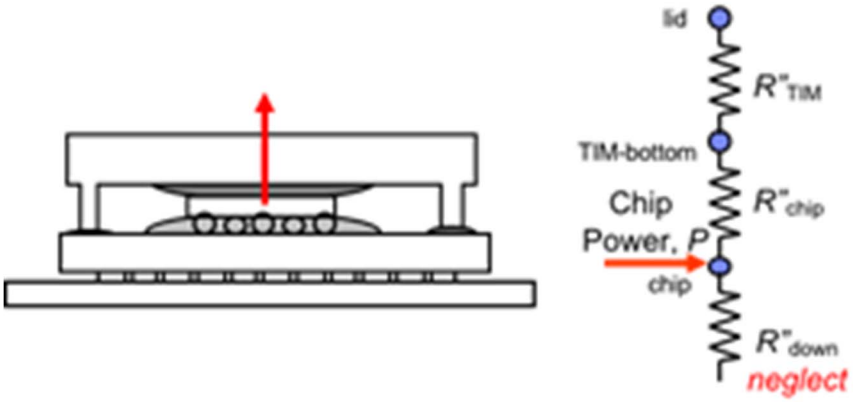

Figure 6. Conduction paths in a high-power 2D package

In a high-power 3D package, heat from the bottom chips in the 3D stack has to conduct through additional materials that form the interconnect/underfill layers, the back-end-of-the-line (BEOL) layers, and the bulk silicon above the BEOL layers. This causes additional thermal resistances in the heat conduction path as depicted in Figure 7.

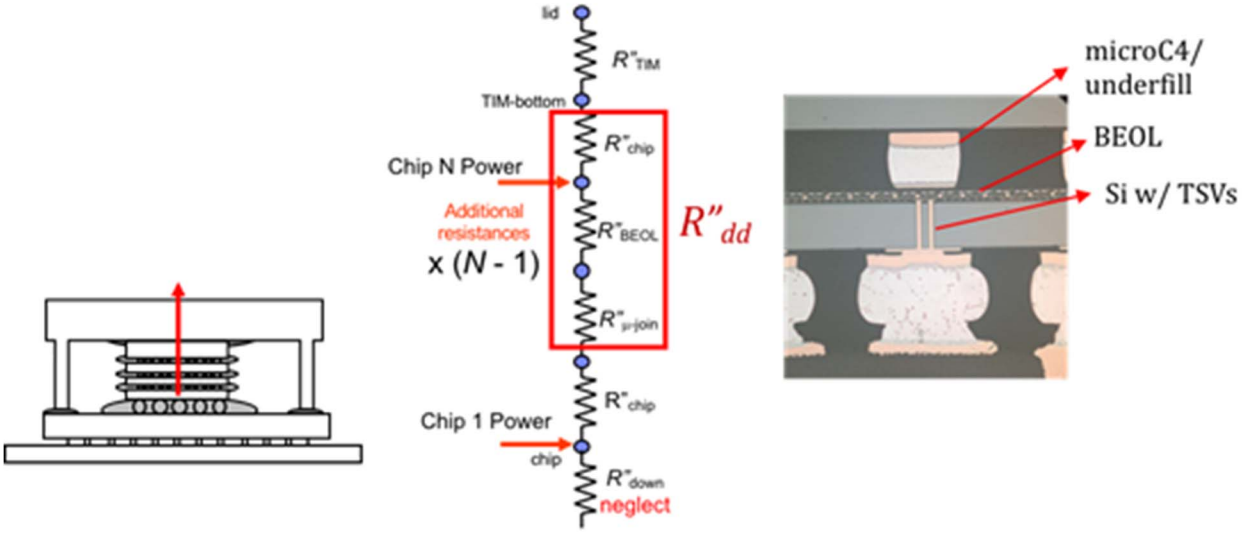

Figure 7. Conduction paths in a high-power 3D package

Additional increase in temperature in a 3D chip package can occur due to vertical alignment of high-density computing cores and different-sized stacked chips. Alternatively, such a chip stack can be cooled from both top and bottom, offering a 2x improvement in cooling capacity but at the cost of a far more complex design.

2.3 3D Stacked Die with Embedded Liquid Cooling

To continue scaling computer performance as Moore's Law transistor scaling slows, the IT industry has turned to 3D chip stack interconnect technology, which both increases the bandwidth between chips and enables heterogeneous integration to improve computing performance. However, the stacking of chips presents new thermal challenges as heat generated by multiple chips within a chip stack results in higher heat density which must be effectively removed.

The traditional approach of 2D chip thermal management is to conduct the heat from the active devices through the silicon die to a heatsink or cold plate which is attached to the top (or backside) of the chip with a thermal interface material as shown in Figure 8(a). The conduction of heat through a 3D chip stack as shown in Figure 8(b) creates a thermal challenge, since the heat must conduct through multiple dies within the stack. Heat generated by the Nth die in a chip stack will conduct heat through N-1 dies to reach the heatsink or cold plate placed upon the top of the first die in the chip stack. It is important to note that the dies include complex structures including the Front-End-of-the Line (FEOL), Back-End-of the-Line (BEOL) with multiple wiring levels, and Through-Silicon-Vias with uC4 interconnects between them, as also shown in Figure 8b. These structures, when stacked and assembled with the usual placement and alignment tolerances, dramatically increase the thermal resistance between the dies in the stack and the heatsink or cold plate placed on the top die in the stack.

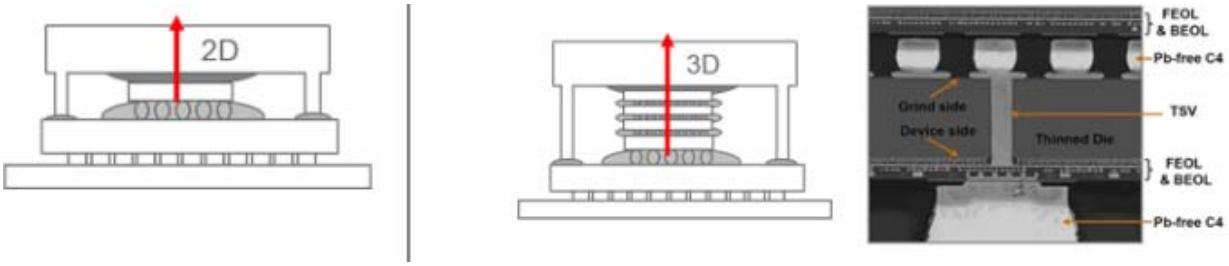

Figure 8: 2D vs 3D Thermal Path

While conducting heat through a chip stack can provide effective thermal management for stacks of low-power chips, when stacks include one or more high power chips within the stack, the conduction of heat through the dies and interconnects in the stack can produce high gradients in the chip junction temperatures across the stack.

A method to address the challenges of cooling 3D chip stack structures described in this section is embedded cooling, where coolant flows either within (intrachip) or between (interchip) the stacked high-power chips as shown in Figure 9 below.

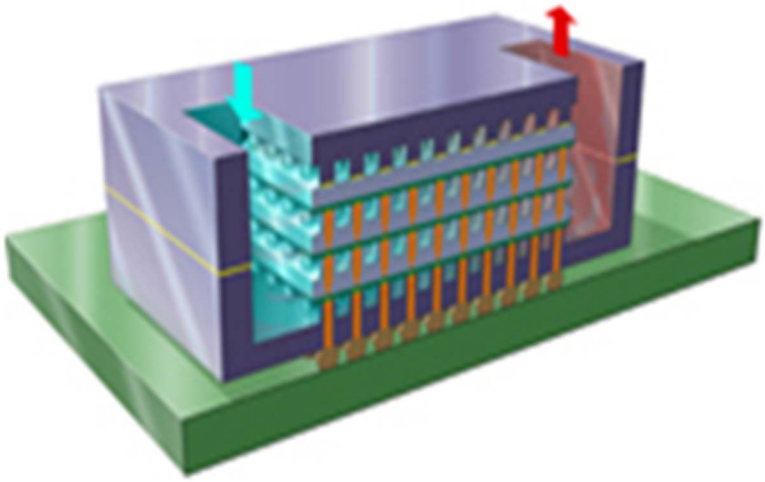

Figure 9 Embedded cooling with liquid flow internal to a 3D stacked chip package

Embedded cooling creates new requirements for 3D chip stack co-design, including placement and dimensions of fluidic channels, coolant properties, and compatibility with chip stack power and signal electrical interconnects. The fluid channel heights may be guided by compatibility of fabrication processes to create electrical interconnects between dies in the stack layers. For example, parallel channels with dimensions which meet the electrical requirements can create substantial pressure drop when using a single-phase liquid to flow across 20 mm (or more) for large processor dies. Use of the most conventional liquid coolant, water (which is conductive), requires the need to isolate the fluid from power and signal electrical interconnects and also consider dielectric losses associated with transmitting high frequency signals nearby. These challenges are part of the electrical, mechanical and thermal co-design of embedded cooling into a 3D chip stack.

2.4 Thermal challenges in Photonic devices

Photonic devices as shown in Figure 10 can have high power density and require novel approaches to thermal solutions. Thermal challenges associated with photonic devices pertain to both the temperature swing and the absolute operating temperature of a given device. Depending on the component and use conditions, either one or both criteria may limit its performance. For example, optical modulators often depend on interference and resonant effects. Resonant modulators, which are useful to reduce the energy per bit, are mainly limited by the temperature swing (typically < 30°C), whereas oscillators such as laser sources are limited by both the temperature swing (typically < 30°C) and the absolute operating temperature (typically < 100°C) [3]. In addition, photonic devices can be integrated with other functional IC components at the chip and/or package/system level. These components may have different thermal specifications which require both package and system thermal solution optimization.

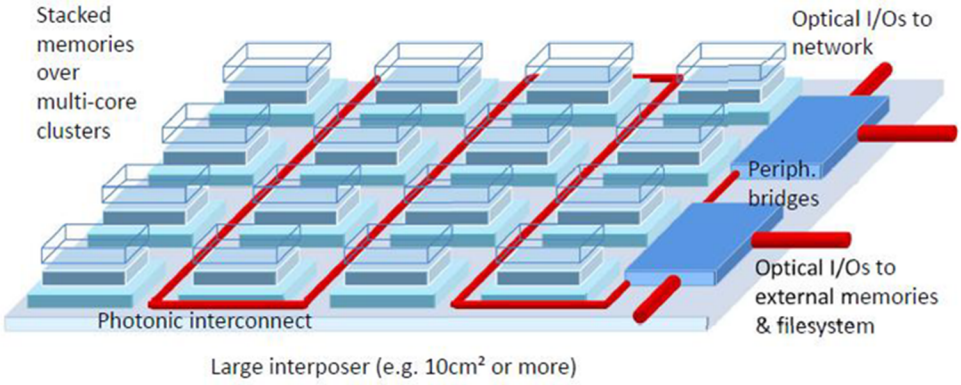

Figure 10: Heterogenous packaged photonics with stringent temperature control challenges [4]

2.5 Heterogeneous Integration for Harsh Environments

2.5.1. Aerospace, Automotive and Space Harsh Environment Requirements

As the world is getting more digital – through such trends as IoT, autonomous vehicles, AI and electric drive – safe and reliable operation of electronics in harsh environments such as aerospace, automotive, and space are becoming more and more critical.

In order to let compute systems take control of assets that can impact the safety of persons and/or cost millions of dollars, strict standards of hardware and software system safety must be taken into account. Harsh environment electronic applications must typically satisfy stringent requirements to operate safety-critical applications in extreme temperature, dust, vibration, and, corrosive environments for operational periods of 10 to 30 years. In an example of harsh environment electronics, aerospace class I electronics need to operate in a continuous ambient environment of -54°C to 55°C and survive a temporary 30-minute ambient environment of 71°C, without cooling air supply, simulating a cooling air supply fault condition.

In the automotive environment, burn-in and test of heterogeneous or multichip systems is a particular challenge. Test temperatures are extreme because of the harsh environments that these systems must operate in, sometimes ranging from -55°C to 175°C. For automotive power electronics, the research focus and target is to increase the power density to 100 kW/L and double the reliability from 150,000 to 300,000 miles, while lowering the cost of power electronics, electric motor and the overall traction drive system by 2025 [5]. This power electronics power density increase to 100 kW/L represents a factor of 5 to 10 increase with respect to the state-of-the-art electric-drive vehicle power electronics.

Satellites are increasingly using power-hungry devices such as earth observation detectors operating in new or multiple frequency bands. The higher frequency bands currently under consideration for next-generation transmission systems offer higher bandwidths than the longer-range bands currently in use. At the same time, those shorter-wavelength bands by nature have larger propagation losses. Challenges in space requirements involve the impact of solar heating and space radiation with the potential of significant thermal cycling of the electronics package, which is especially challenging for heterogeneously integrated packages.

Application of heterogeneous integration to harsh environments is challenging due to the 3D top-side contour of heterogeneous packages, the dissimilar junction limits of heterogeneous components in a system, and the extreme thermomechanical challenges imposed by the extreme temperature cycles. However, due to the superior performance, it is likely only a matter of time before these challenges are overcome and heterogeneously integrated chips make their way into the harsh environment space.

2.5.2 Heterogeneous Integration Top Side Cooling Solution needs

Rugged harsh-environment electronics rely predominantly for heat rejection through a thermal interface layer and a heat spreader mounted over the flip-chip package. This thermal interface layer serves to thermally connect components of dissimilar coefficient of thermal expansion (CTE) such as silicon (chip) and aluminum or copper (heat spreader). As ruggedized electronics typically are produced in moderate volumes (100s-1000s), chip height, chip warpage and other non-planarity variations batch to batch of several hundreds of microns can be typical due to ball grid array (BGA) and silicon variations. The thermal interface material also serves to compliantly compensate for these differences by filling gaps and ensuring good thermal contact between these components.

As heterogeneous integration introduces 3D non-planar and large silicon structures, challenges can be envisioned in connecting to a top-side heat sink using current thermal interface materials. It can also be expected that as multiple micro-BGA connections are used to create vertical stacks, height and planarity variations will accumulate, resulting in amplified variance in the eventual location of the top-side chip interface as illustrated in Figure 11.

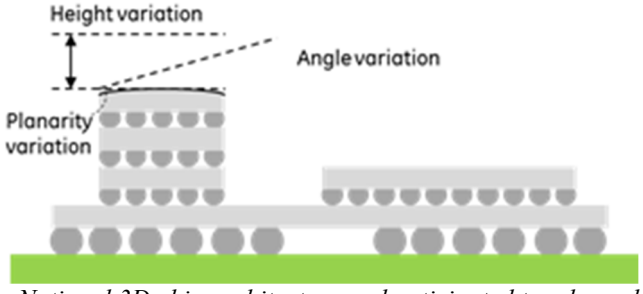

Figure 11: Notional 3D chip architecture and anticipated topology challenges

To manage this, novel 3D thermal interface material systems are envisioned. De Bock et al. [6] describes such a thermal interface system that uses a thicker layer of low melting point (LMP) solder, encapsulated by an ultra-thin layer micro layer of a high-temperature polymer. When pressure is applied during heating, the LMP solder flows conformal to the chip shape while being contained by the thin polymer "bag" as illustrated in Figure 12. When the containment layer polymer is sufficiently thin, its detrimental contribution to the TIM thermal resistance can be sufficiently small, outweighed by the superior thermal conductivity of LMP solders like Indium (k ~ 70 W/m-K), which exceeds common thermal interface materials.

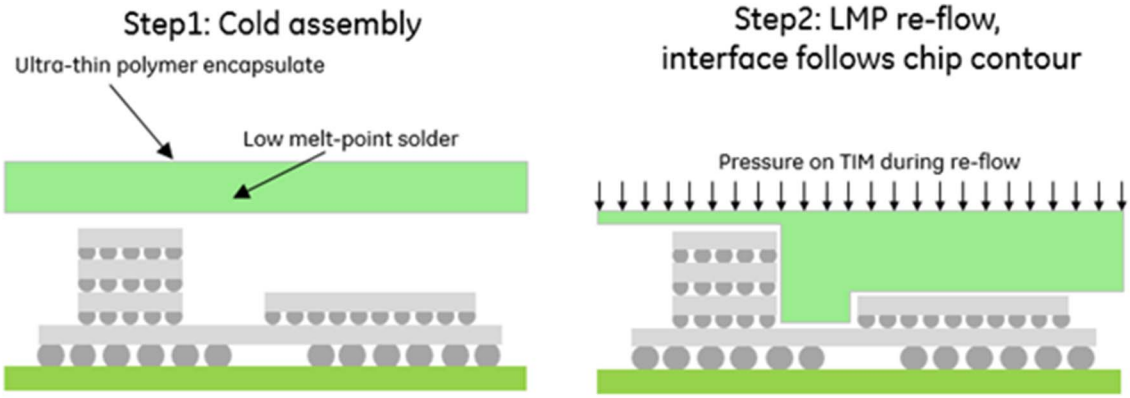

Figure 12 Encapsulated LMP solder thermal interface system with the potential to conform to 3D chip topology

As LMP solder never comes in full contact with the silicon chip, no intermetallics are formed, eliminating the need for barrier coatings and allowing for re-workability. The benefits of such a concept are the ability to compensate for chip height and angle variation, non-planar chip warpage, and 3D topologies.

2.5.3. Dissimilar heterogenous component systems solutions

In automotive power conversion, a target of power density increase to 100 kW/L are envisioned to be achievable by downsizing the components and managing device heat fluxes on the order of 1000 W/cm^2. In addition, increasing the temperature of the wide-bandgap (WBG) devices up to 250°C is an important enabler towards meeting the goals of downsizing the components. This is a heterogeneous integration thermal management challenge since multiple components with different functionalities and temperature limits (transistors, diodes, capacitors, gate drivers, other passives) need to be packaged within a small volume. Hybrid silicon and WBG technologies and configurations are also of interest – and this is another heterogeneous integration challenge or problem.

Figure 13 shows a schematic of an inverter in which the different components are in a stacked, multilayered, compact configuration. A power module or package incorporating WBG devices is desired that can operate at device junction temperatures up to 250°C. This will require significant advances in WBG device technology, circuit boards, advanced interface materials and interfaces (likely bonded interfaces), electrical interconnects, encapsulants, electrically-isolating substrates, as well as novel baseplate and heat exchanger materials that can withstand the higher temperatures, give good thermal performance and also have mechanical properties that ensure good reliability for the system (the target numbers have been listed above).

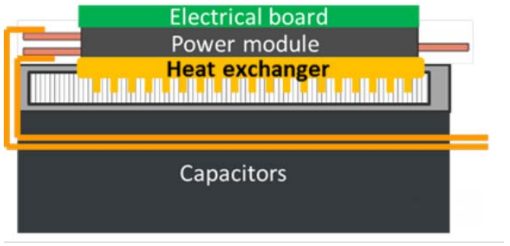

Figure 13: Inverter in a multi-layered board or stack-up configuration

Some components such as gate drivers and capacitors have lower temperature limits – as the state of art stands in terms of materials capabilities – of approximately 125°C or lower. In order to package these passive components – utilizing in-board, stacked 2- or 3-D packaging concepts – in close vicinity of the higher-temperature (e.g. 250°C) semiconductor device or package, advanced thermal management techniques will be required. These include fluid-based cooling technologies, and also concepts such as manipulation of heat flux lines (e.g. metamaterials) so as to divert or block the heat flow to lower-temperature-rated components. There is scope for innovation in the fluid-based cooling technologies; two-phase cooling through passive/pool boiling or forced convective boiling, vapor chambers, heat pipes, and perhaps even fluid-cooling utilizing dielectric fluids within the transistor and diode need to be investigated.

Thermal management of electrical interconnects is an important way to keep the capacitor temperatures within limits [7]. Heat typically flows to the capacitors from the packages/devices/power modules via the electrical interconnects (Figure 13) and thermally managing the interconnects is important for inverter/converter system-level thermal management as well.

Higher voltages are also being considered as a means to downsize the footprint and increase the power density of the power electronics. This will require development of appropriate electrical isolation for the higher voltage, which could have thermal management implications as well. Either the material or the thickness/footprint of the electrical isolation will have to change, and thermal solutions will have to be developed or adjusted accordingly to ensure good thermal performance and reliability as well as to maintain a compact footprint.

2.5.4. Heterogeneous integration thermo-mechanical solutions

Satellite phased-array antenna-in-package solutions offer increased efficiency for higher power applications; however, heat dissipation remains a challenge. Materials in the signal propagation path must be dielectric to minimize signal losses, limiting the applicability of topside cooling strategies. Penetrations in the PCB, and heat sinks with pedestals, have been proposed to bring cooling to the package for these high-power applications [8]. However, in the vacuum environment of space where convective cooling is not available, the need for compliant interface

materials that can make contact with an array of discrete components while not suffering performance losses due to the lack of convective enhancement remains a critical need.

In addition to AiP challenges in the space environment, satellites in low earth orbit (LEO) may deploy onboard FPGA system-in-package solutions to enable services such as on-board signal or image processing and 5G internet. Because their orbit is not geosynchronous, these devices typically operate intermittently and dissipate a large amount of heat locally for a short amount of time. Sizing a radiator of the small-LEO satellites for peak heat loads results in excessive area requirements and results in components becoming too cold in non-operating conditions. Furthermore, these components are generally located in the interior of the satellite, without direct access to a radiator. Over time, thermal fatigue also becomes a significant challenge, especially with CTE-mismatched heterogeneous structures. When coupling high-power components to the radiator via heat pipes is not an option, local thermal storage using phase change materials or other high specific-heat-capacity solutions that minimize required system launch weight may become attractive solutions.

At the same time traditional interfacing strategies for test, including the use of liquid thermal interfaces or dry interfaces, are no longer viable because the varying die heights would result in components with no contact to the thermal control unit (TCU). To fill the gaps between the multiple die and the TCU, durable, compliant, low-compression-set interfaces are required. Silicone-based materials offer the mechanical properties that these applications demand (wide operating temperature range, forgiving compressive mechanics); however, the risk of silicone contamination of the device under test drives the need for new solutions. Aligned, conductive, nanosprings, such as carbon nanotube arrays impregnated with polymers, may offer a path forward [9], if they can offer the long-range compressibility (on package die height variations on the order of 100s of microns) as well as low compression set (to address variation in package to package height driven by manufacturing tolerances) that these emerging technologies demand.

2.5.5 Heterogeneous integration in harsh environment: conclusion

As with most electronics lifecycles, operation of new technology often starts in highly competitive applications with limited operational life, of which some can be consumer electronics. As these technologies mature and gain more pedigree, more and more application for critical electronics in harsh environments can be considered. This study identified three areas of technology research that can be focused on to further aide this progression. These are the development of 3D thermal interface technology, application of CTE matched heat spreaders, and active transient thermal hot spot management. It is anticipated that with time and development support, these technologies will further advance allowing one day for safe and reliable operation of heterogeneously integrated electronics in the transportation, industrial and other safety-critical systems of tomorrow.

2.6 Thermal challenges in mobile platforms

The shrinking form factor of mobile electronic devices in conjunction with significantly increasing performance and functionality have resulted in substantial thermal challenges. Nelson and Galloway [10] report reduction in thickness of Smart Phones from about 25 mm to less than 10 mm while power has increased from below 3 W to about 7 W for the latest devices. The total number of packages inside such SmartPhones have also grown over several product generations to about 70 [10].

Figure 14 [10] shows the external surface temperature profile for a commercial SmartPhone and illustrates the presence of a significant hotspot at the location of the processor.

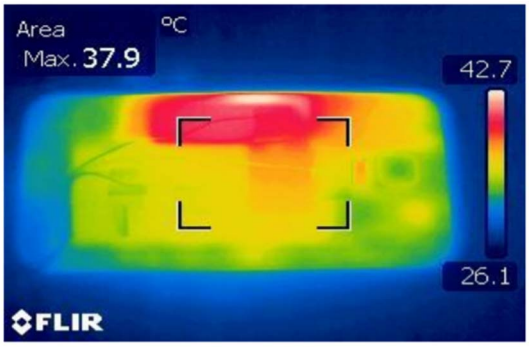

Figure 14: Temperature contour data for the external surface of a SmartPhone [10]

Steady state and transient thermal characteristics and spreading from hot spots primarily through conduction (copper, PCB, silicon, TIM) are reported to be key drivers for thermal design [10] with dynamic thermally-aware power throttling being an effective control technique for thermal management.

Figure 15 provides an inside view of a State-of-the-Art Smart Phone [10] and shows a micro heat pipe spreader attached to multiple devices and packages to promote heat spreading from multiple heat sources. Graphite sheets and copper "straps" have also been harnessed to this task.

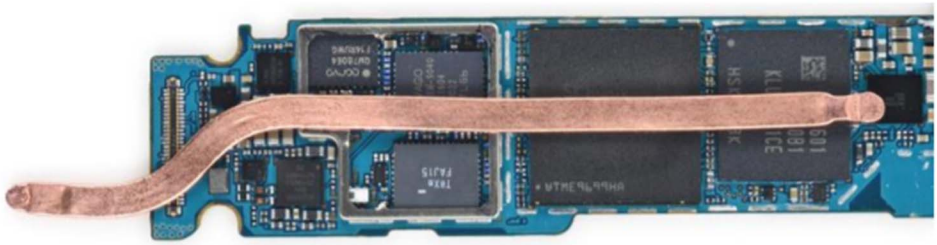

Figure 15: Micro heat pipe in a modern smartphone [10]

2.6 Thermal challenges in voltage regulators

Scaling trends and device refinements indicate gradual and steady transition to lower threshold voltage regulator devices, driving up package-level current to several 100s of amps. Ohmic losses on power delivery connections tend to dominate the power dissipation. However, local decoupling needs exacerbate the challenges associated with higher voltage DC distribution and down conversion to required DC levels with regulator on/near die (and on-die) within package. Thus, one of the power devices that can be part of a heterogeneously integrated package is a VR (Voltage Regulator) such as what is depicted in Figure 16. Such power devices inside the package are potential hot spots and create a significant cooling imperative. For example, even at 95% efficiency, a 200W VR (Voltage Regulator) will dissipate 10 Watts, mostly within the power switching devices with a small footprint inside the package.

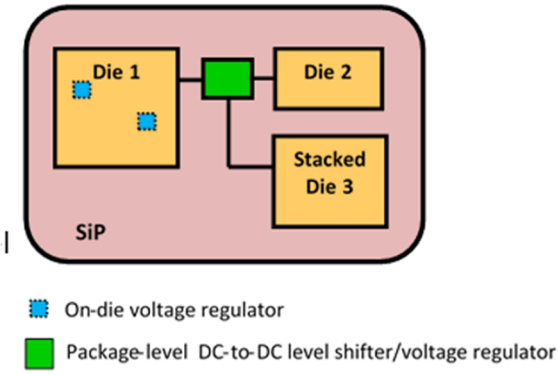

Figure 16: Package level DC to DC VR schematic

3.0 Advanced Technologies and Research Innovations

3.1 Thermal interface materials

Electronic device performance is constantly improving, but with this evolution comes greater power consumption and heat generation. It is imperative to effectively transfer heat from semiconducting materials (any hotspot surfaces in the computing system: e.g., integrated circuit chips, a central processing unit, and a graphics processing unit) to the metals used for heat spreading and exchange through the interface materials. Thermal interface materials (TIMs) provide a low-resistance thermal pathway between two surfaces by filling the interfacial volume created when two microscopically rough surfaces are in contact [11, 12]. An ideal TIM is both thermally conductive, to facilitate heat transfer across the interface, and mechanically compliant, to conform to the surface roughness and to maintain the interface's integrity despite thermomechanical stresses imposed by temperature gradients, thermal cycling, and thermal aging. However, these two properties often scale dichotomously, where high thermal conductivity materials are typically dense and stiff, while soft materials are generally poor thermal conductors [11-13]. As a result, most commercially available TIMs are either thermally conductive (e.g., solder) or mechanically compliant (e.g., thermal paste), but rarely both.

Two strategies are commonly used to create TIM composites that pursue the combination of high thermal conductivity and mechanical flexibility, as illustrated in Figure 17.

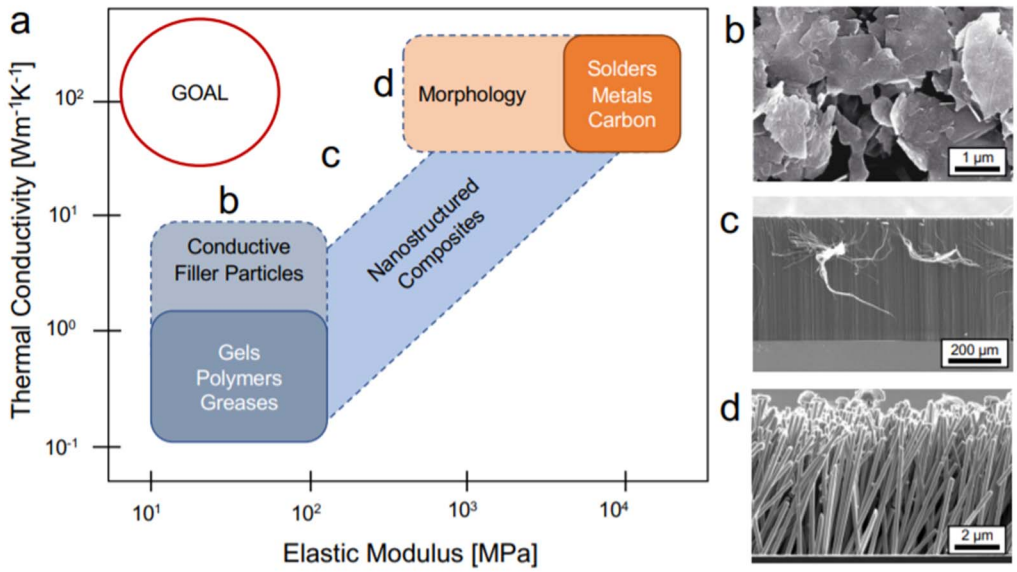

Figure 17 (a) Two common strategies can be employed to create high-performance TIM composites [14], (b) an example of graphene-polymer composite [15], (c) vertically grown nanotubes [16-17], (d) vertically electrodeposited nanowires [14, 18]

One strategy is to begin with an intrinsically soft material and add fillers to increase the thermal conductivity, such as an example of graphene-polymer composite in Figure 17 (b). The second strategy is to form a nanostructure from an intrinsically conductive material into a mechanically compliant morphology, such as Figure 17(c) vertically grown nanotubes [16-17], and (d) vertically electrodeposited nanowires [14, 18].

For the first strategy described above the method of manufacture would be to begin with an intrinsically soft material, such as a polymer, and add conductive fillers (e.g., metal nanoparticles, carbon nanoparticles, and graphene nanomaterials) to increase the effective thermal conductivity by creating a conduction network [19].

For the second strategy, the fabrication process would be to build the nanostructured conductive material (e.g., metals and graphite) into a mechanically compliant morphology. Aligned arrays of continuous, conductive elements improve the effective thermal conductivity by providing out-of-plane heat transfer pathways. Recent approaches have focused on synthesizing carbon nanotubes (CNTs) into vertically aligned arrays [16-17]. However, the CNT arrays show lower thermal conductivity values (of 10-50 W/m-K) than theoretical estimates, due to the material's uncontrollable morphology during the growth process, nanotube-nanotube contact resistances, and defects [16-17]. More recent work has explored the use of templated electrodeposition to design metal architectures (i.e., aligned metal nanowires [14], porous metal structures [20], and nanosprings [21]) in a controlled manner, in order to precisely engineer mechanically compliant TIMs.

To address various challenges of current TIMs, a new class of compliant and ultrathin TIMs can be developed consisting of copper nanosprings embedded in a polymer layer by using the templated electrodeposition method. The proposed nanosprings with 200 nm diameter and > 25% volume fraction will result in an effective thermal conductivity of 100 W/m-K, leading to conduction thermal resistances smaller than < 0.5 mm2 K/W with < 50 µm thickness. The installation of elastic nanosprings will help to minimize the boundary thermal resistances between nanostructures and the surface, by accounting for a surface roughness tolerance, resulting in a value of < 0.5 mm^2 K/W. The temperature- and pressure-dependent thermal characterizations for varying TIM morphology and bonding methods can be followed to advance the understanding of the material's structure-related properties [18].

Besides CNT arrays and metal nanosprings that yield anisotropic thermal conductivity of the TIM, progress as illustrated in Figure 18 [22] is being made in the synthesis of porous continuous ultrathin graphitic foam (UGF) structures and in using them to achieve an isotropically high thermal conductivity. Methane chemical vapor deposition (CVD) on sacrificial sintered nickel powder has yielded UGF structures with a micrometer-scale pore size, macroscale lateral dimension, and effective thermal conductivity approaching 20 W/m-K at a porosity larger than 90%. The nickel powder can be recycled with an electrochemical etching and deposition process to lower the

manufacturing cost. Besides electrically conducting UGF, electrically insulating, semi-transparent, thermally conducting porous foam architectures of hexagonal boron nitride (h-BN) can also be grown with a similar CVD process. Both the UGFs and h-BN foams can be explored further to serve either as high-thermal conductivity fillers of polymeric TIMs or polymeric substrates for future-generation flexible electronics.

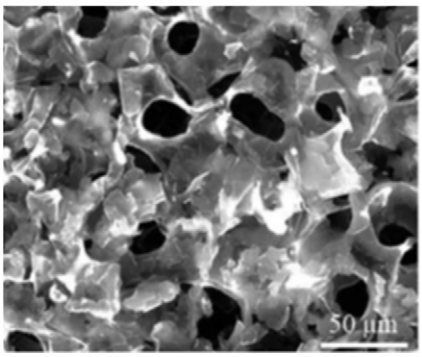

Figure 18: SEM image of a porous ultrathin graphite foam structure [22]

3.2 System thermal limits for HPC multi-chip modules

Thermal management of multi-chip heterogeneously integrated systems poses additional constraints and limitations beyond those for single chip modules or vertically integrated systems. Applications related to HPC systems tend to be high power and have strict reliability and availability requirements. The major thermal concerns are hot spot junction temperatures and transient excursions. They may also have multi-chip modules in close proximity and possibly with different thermal requirements, non-uniform device heights off of the substrate, hot spots on different devices, and transient excursions in workload and power. The emphasis here is on HPC applications, and the intent is to summarize either commercially available or demonstrated system solutions, cooling limits for air, single-phase liquid cooling, or two-phase cooling. Establishing heat flux limits is not a simple matter since the maximum possible heat flux limit depends on many application-specific factors, including the number of devices, the spatial device power distribution (i.e. power non-uniformity), the allowable junction temperature, the allowable pressure drop, the volume and weight limitations for the cooling solution and acoustic constraints, among others.

3.2.1 Air cooled heat sinks

For multi-chip modules a typical high heat flux thermal solution may look like the schematic diagram shown in Figure 19 (adapted from [23]). The total thermal resistance from junction to air will depend on the TIM used, the efficiency of the vapor chamber, and the heat sink design. The air flow velocity is limited by the acoustic system specs and the allowable pressure drop in the system. Within these practical limitations and assuming a uniform heat flux at the devices, the maximum possible device heat flux is estimated to be about 84 W/cm^2 [24]. Higher heat flux levels may be possible through refinements of the heat sink and/or vapor chamber design and the TIM thermal resistance, or through the opening up of the practical limitations such as the allowable heat sink volume or air flow.

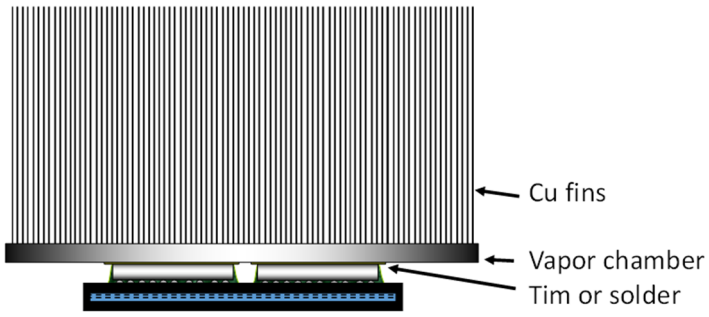

Figure 19: Figure adapted from [23] showing a schematic diagram of a heterogeneously integrated multi-chip module with a Thermal Interface Material (TIM) or solder attachment and a vapor chamber

3.2.2 Liquid and two-phase cooling

There are several approaches to liquid cooling of electronic systems. These can be broadly classified into indirect and direct liquid cooling. In direct (immersion) systems the coolant comes into direct contact with the devices and therefore the cooling material needs to be a dielectric. This could exclude water as the cooling medium and is

therefore a significant limitation in terms of achieving very high heat flux levels. To make water as a medium work for such configurations would require electrically insulating technology (e.g. plated ground planes, sufficiently thicker chips) to isolate the devices from the water. It is also a challenge to have the cooling fluid come into direct contact with the electronic devices, since any organic materials in the system pose the risk of degradation and leaching into the coolant over time. The advantages of direct liquid cooling are primarily the reduction of thermal resistances such as heat spreaders and TIMs. Chip-scale cold plate designs with fluorocarbon cooling can be used with heat flux levels of up to 100 to 300 W/cm^2 [25-28]. The range depends on specific designs and system considerations. Even higher heat flux levels may be achieved if cost and space limitations are expanded.

Indirect cooling is distinguished by the presence of a physical barrier between the devices and the coolant, thereby eliminating concerns about chemical interactions between the coolant and the devices and also making the usage of water (with additives) a possibility. Direct and indirect liquid cooling both single-phase or two-phase, can be used, with distinct advantages and disadvantages to each approach. Single-phase cooling systems are easier to design and operate. However, when single-phase systems are used to cool multiple devices in series, the incoming coolant keeps rising in temperature, which may be a limitation depending on the application. Two-phase systems, if well controlled, have the advantage of operating at nearly uniform temperatures even when used serially to cool multiple modules. Indirect water cooling can achieve significantly higher heat flux levels of up to 300 to 450 W/cm^2 for chip-scale water jet impingement solutions.

It is also noteworthy that off-the-shelf single- and two-phase rack-level cooling solutions have significantly lower heat flux cooling levels than those shown in Table 1 below. Table 1, adapted from [23], provides a summary of cooling limits for air, FC and water as well as the thermal resistance (air cooled module) and thermal insulation (water and FC). A pragmatic approach to accelerating the implementation of advanced thermal management solutions that can be fairly quickly standardized is to start with existing commercial solutions that may be suboptimal, and to redesign them (cold plate, TIM selection, assembly process) to reach much higher heat flux levels, and to meet specific heterogeneous integration requirements. This can be done in collaboration between industry and academia.

Table 1: Comparison of system cooling capabilities

Thermal solution	High end chip scale heat flux	R_{int} Chip to heat sink/cold plate	R_{ext} heatsink/cold plate
Advanced multi-chip air cooling with integrated vapor chamber	85 W/cm^2	Vapor chamber 0.267 °C/W (w/ Grease) 0.2 °C/W (with solder) for Chip to fins	0.1 °C/W for Al .069 0C/W for Cu [20]
Water cooled separable module level cold plate	250 W/cm^2	35 mm^{2}K/W Lid +TIM	12.8 mm^{2}K/W
Water cooled integral module level cold plate	325 W/cm^2	10 mm^{2}K/W (TIM)	12.8 mm^{2}K/W
Water cooled chip scale cold plate	390 W/cm^2	10 mm^{2}K/W (TIM)	°mm^{2}K/W
Water jet impingement [31]	460 W/cm^2	N/A	2.5 mm^{2}K/W
Fl. Carbon chip scale heatsink [30]	300 W/cm^2	10 mm^{2}K/W (TIM)	15 mm^{2}K/W
Micro channels in the device with single phase water flow [32]	About 790 W/cm^2 71 °C temp rise	0	Depends on the microchannel design.
Radial Microchannels in the device, using two phase dielectric cooling [50]	Core Area > 350 W/cm^2 Hot Spots > 2000 W/cm^2	0	Depends on microchannel design

3.2.3 General design guidelines with currently available materials and infrastructure

The current best-case TIM is solder (e.g. Indium). Having chip-level cold plates allows for the elimination of the caloric resistance. Water has a high thermal conductivity and specific heat capacity and therefore outperforms FCs. From Table 1 above the best-case scenario is direct water jet impingement with a thermal performance of about 2.5

mm^2K-W. Further reduction in thermal resistance would require etching microchannels or fins in the silicon directly as demonstrated by Tuckerman and Pease [32] who demonstrated a heat flux of 790 W/cm^2 at a maximum temperature rise of 71°C. Although this approach has not been commercialized, it may be considered to be close to the best achievable ultimate heat flux level for silicon devices with longitudinal microchannels. Manifold-based microchannel configurations discussed subsequently in this chapter outperform single-pass longitudinal arrays. This would be approximately true for 3D stacks with cooling liquid through the stack as well. For this case, the internal thermal resistance is 0 and the external resistance will be a function of the microchannel design.

3.2.4 Summary

- For air, the use of vapor chambers with large optimized heat sinks may be able to attain a heat flux in the range of 80 to 100 W/cm2 within pragmatic constraints.
- For single-phase cooling, direct water jet impingement [31] has been demonstrated to deliver up to 460 W/cm2, which may be thought of as close to the limit of water jet cooling.
- Fluorocarbon materials with chip-scale cold plates can deliver up to about 300 W/cm2.
- The ultimate limit of direct water cooling at the device level may have been demonstrated by [32] to be in the range of 790 W/cm2. This limit may be crucial for true 3D stacks with 3D cooling.

3.3 Embedded liquid cooling of chips and chip stacks

Embedded cooling [33] represents a third generation ("Gen3") thermal management technology for electronic circuits and was the focus of DARPA's recent Near Junction Thermal Transport [34] and Intra/Interchip Enhanced Cooling [35-36] thermal packaging programs. The DARPA Near-Junction Thermal Transport (NJTT) program, initiated in 2011, was the first program to develop thermal management for the region within 100μm of the electrical junction of a GaN transistor, to enable heat fluxes of greater than 10 kW/cm^2 while maintaining reliable junction temperatures. Through technology developed in this program, specifically the transfer of GaN epitaxy to high thermal conductivity diamond, the power handling capability of GaN HEMT devices was increased by greater than a factor of 3 [37-42].

While the NJTT program made significant gains using high thermal conductivity substrates to spread the heat close to the junction, it did not address the next link in the thermal resistance chain, i.e. extracting the heat from the diamond and transferring that dissipated heat to an available coolant. The DARPA ICECool program [43], which began in 2013 and is now nearing completion, combined embedded microfluidics with high thermal conductivity substrates to reduce the thermal resistances in the entire package. The successful demonstration of embedded cooling by three of the participating research teams is described in this section.

3.3.1 2D chip direct contact liquid cooling with hierarchical manifolds

Electronic devices have traditionally been cooled through the attachment of separate heat sinks. In this 'remote cooling' architecture, the performance of the thermal management solution has become increasingly governed by interfacial, conduction, and spreading thermal resistances incurred by the package and the mechanism of heat sink attach. Trends in heterogeneous integration call for the development of transformative cooling strategies that embed the thermal management solution directly within the device to alleviate hotspots. 'Intrachip cooling' strategies deploy coolant channels directly in the electronic device, eliminating interfacial resistances but leaving little material thickness available for heat spreading; this exposes the embedded microfluidic heat sink directly to the high heat fluxes generated from the device. Dielectric working fluids are preferred for such systems because they minimize the threat for electrical shorting.

As part of the DARPA ICECool Fundamentals program [43], researchers at Purdue University have demonstrated dissipation heat fluxes exceeding 1000 W/cm^2 by feeding an array of high-aspect-ratio, intrachip microchannel heat sinks in parallel with a dielectric coolant via a manifold for fluid distribution. The fabrication of suitably high aspect ratio microchannels etched into the silicon test chip provides the necessary surface area enhancement to dissipate high heat fluxes at an allowable surface temperature rise; the microchannels are imbedded directly into the heated substrate to reduce the parasitic thermal resistances due to contact and conduction resistances. Parallelization of the flow across an array of short-flow-length microchannel heat sink elements serves to minimize the pressure drop across the heat sink. This allows for flow boiling operation in the microscale channels, which would otherwise be prohibitive due to pressure drop constraints.

A hierarchical manifold microchannel heat sink array test vehicle, with all flow distribution components heterogeneously integrated, was fabricated to demonstrate thermal and hydraulic performance of this technology (Figure 20, [44-45]). A silicon chip, with resistive heaters and local temperature sensors fabricated directly on the

opposite face, is cooled by a 3 × 3 array of microchannel heat sinks using dielectric HFE-7100. The heat sink performance is characterized over a range of channel mass fluxes and channel geometries. At a mass flux of 2100 kg/m²s and for microchannel channel cross sections with widths of 33 µm and depths of 470 µm, uniform heat fluxes up to 1020 W/cm² are dissipated over a 5 mm × 5 mm heated area, at chip temperatures less than 69°C above the fluid inlet and at pressure drops less than 120 kPa. Experiments are also conducted for heat fluxes generated up to 2,700 W/cm² from a 200 µm × 200 µm hotspot heater overlaid on the background heat flux. This work demonstrates the fabrication, integration, and characterization of hierarchical manifold microchannel heat sinks operating in the two-phase regime.

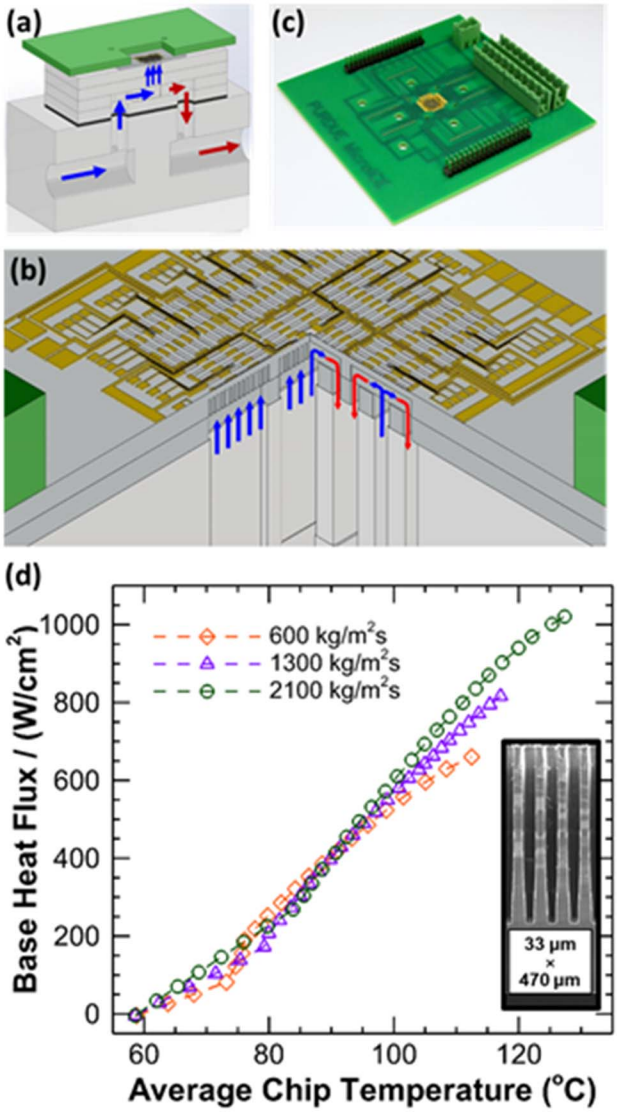

Figure 20: Hierarchical manifold microchannel heat sink array: (a) three-dimension drawing of the test vehicle with a half-symmetry section removed and fluid inlets (blue) and outlets (red) shown; (b) zoomed-in view of the test vehicle with a quarter-symmetry section removed showing the fluid flow paths in the test chip; and (c) photograph of the test chip mounted to the PCB with heaters and sensors face up. (d) Experimental characterization of the base heat flux as a function of average chip temperature for a heat sink with 33 µm ×470 µm cross section microchannels at three different mass fluxes.

3.3.2 Extreme heat flux micro-cooler for direct contact 2D chip liquid cooling

Thermal-power challenges and increasingly expensive energy demands pose threats to the historical rate of increase in processor [49] and power electronics performance. Energy-efficient computing [50] and heterogeneous integration [51] promise substantial reduction in energy demand for emerging and growing computing needs. However, these conflicting trends have resulted in a substantial increase in both heat flux >350 W/cm² and power density, which reduced the efficacy of conventional cooling technology solutions.

Figure 21 depicts the thermal resistance (cm²-K/W) versus chip area for the state-of-the-art high heat flux (~1 kW/cm²) cooling technologies, which indicates it is extremely challenging to reject heat from large area devices using single/two-phase µ-channel coolers (2D and 3D manifold) [46-56]. This originates for the presence of long traverse paths for liquid delivery and vapor extraction as well as the finite thickness of the liquid evaporation film (or thermal boundary layer), which result in a large pressure drop and increased junction temperature (or thermal resistance); note the trend shown by the yellow band, depicted in Figure 21.

A potential solution could be in the form of an Extreme Heat Flux µ-Cooler (EHFµ-C), depicted in Figure 22, that simply "scales up" a high heat-flux thin-wicking structure, either copper inverse opals (CIOs) [46] or silicon pin fin arrays, to a large area EHFµ-C using 3D manifold liquid delivery and vapor extraction conduits [47-48]. Two of the state-of-the-art technologies [46-47] have been developed at Stanford [46-49,55] since 2010 through collaborations with Toyota, Ford, Google and IBM, and with funding from DARPA's IceCool program and the NSF-Center for Power Optimization of Electro-Thermal Systems (POETS). Currently, Stanford is working on the next generation of high performance EHFµ-Coolers (ARPA-e funded). The proposed EHFµ-C (Fig. 22) is produced by bonding a 3D-manifold to a silicon substrate electro-plated with a copper inverse opal (CIO) wick. Liquid channels deliver liquid to the CIO wick, where it is pulled in by capillary forces, and evaporates due to the high heat flux ~1kW/cm² at the substrate.

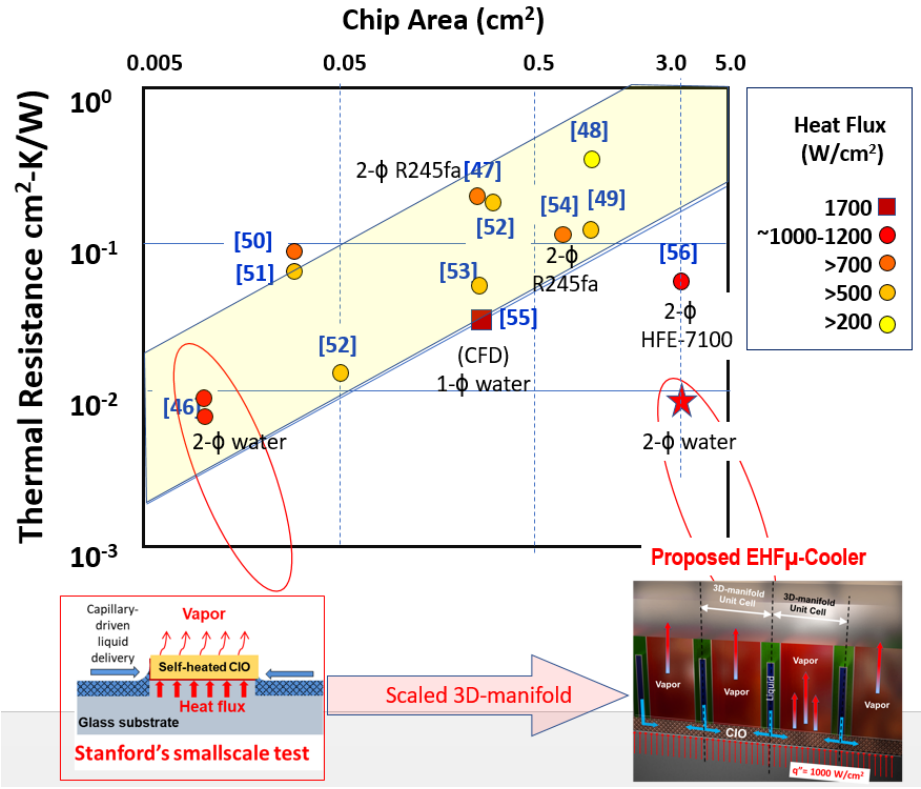

Figure 21: The expected performance targets for EHFµ-Cooler, and that of the state-of-the-art devices including Stanford's previous work [46-47]. Critical heat flux levels are from 200 to 1000 W/cm². The EHFµ-Cooler represents more than 10× reduction in thermal resistance, an unprecedented CHF >1 kW/cm² for water as working fluid, and can be scaled up to large areas >10cm².

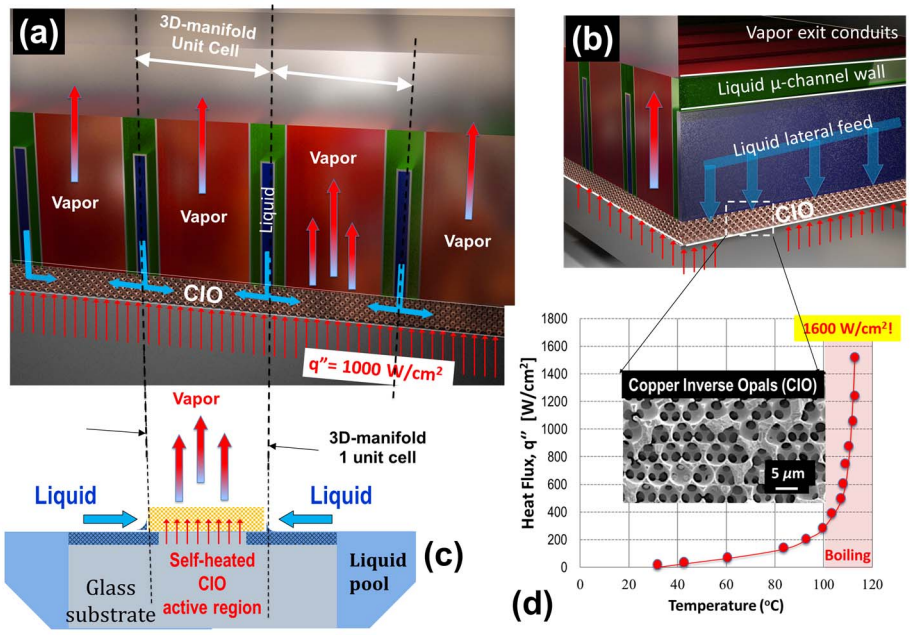

Figure 22: Schematic of the EHFμ-C concept: (a,b) front & sides cross section views. The EHFμ-Cooler is produced by bonding a 3D-manifold to a silicon substrate electro-plated with a copper inverse opal (CIO) wick. Liquid channels deliver liquid to the CIO wick, where it is pulled in by capillary forces, and evaporates due to the high heat flux ~1kW/cm² at the substrate. (c) A schematic of Stanford's "small-scale" test structure [46], (d) capable of removing 1600 W/cm², inset SEM image of CIO with pore diameter ~ 5 μm.

3.3.3 Embedded interlayer cooling for chip stacks with two-phase refrigerant

Embedded interlayer cooling technology provides a solution for cooling 3D chip stacks where a heat sink or cold plate is inadequate for thermal management of 3D stacking of high-power chips because of their inability to cool chips in the middle and bottom of the stack. This chip-embedded cooling technology circumvents that problem by pumping a heat-extracting dielectric fluid into microscopic gaps, some no wider than a single strand of hair (~100 μm), between the chips at any level of the stack. The dielectric fluid used can come into contact with electrical connections, so is not limited to one part of a chip or stack. This ability benefits chip stacks in terms of materials and architecture, such as putting memory and accelerator chips on top of high-power chips in the stack as shown in Figure 23 which includes a fluid port to deliver fluid between the stacked dies.

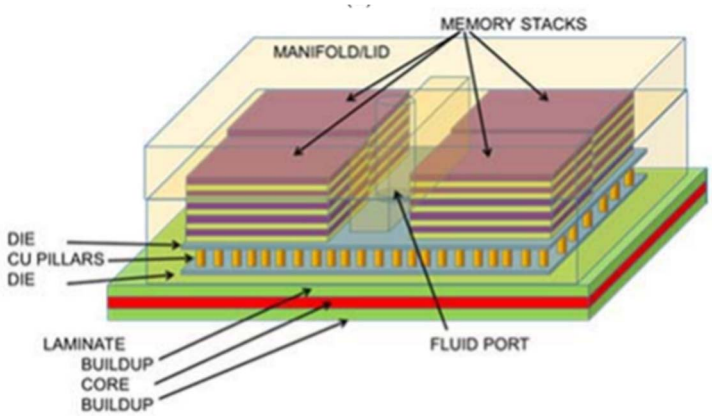

Figure 23: High power 3D package with interlayer cooling [57]

The coolant is pumped into the chips, where it removes the heat from the chip by boiling from liquid-phase to vapor-phase. It then re-condenses, dumping the heat to the ambient environment where the process begins again, as shown in Figure 24. As this cooling system doesn't need a compressor, it can operate at much lower power compared to typical refrigeration systems.

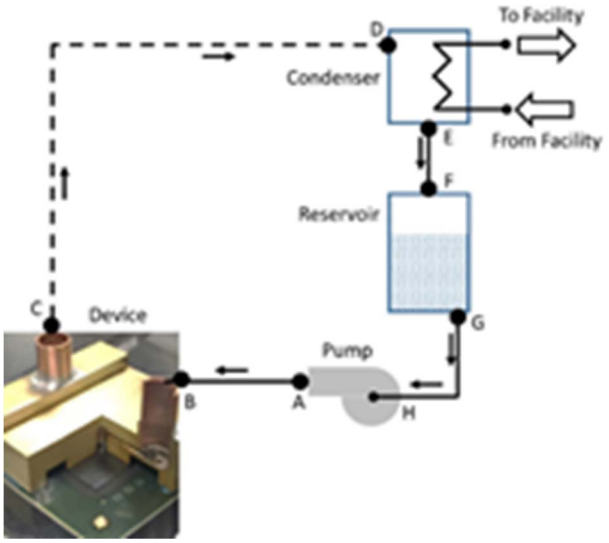

Figure 24: Two Phase Pumped Cooling System

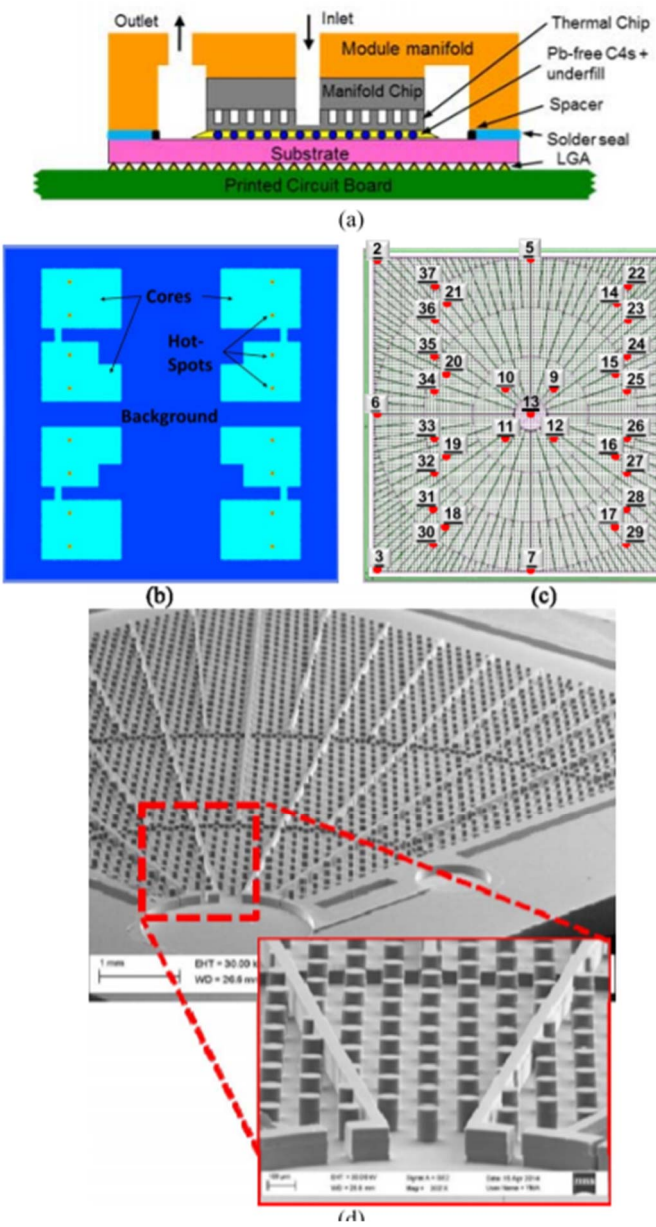

Figure 25; Prototype for Embedded Refrigerant based Interlayer cooling [57] (a) Packaged thermal test Vehicle. (b) Representative power map, (c) RTD numbers and relative locations. (d) SEM image of the orifices and radial expanding channels

Two-phase flow boiling has long been proposed as a potential method for cooling high performance computer systems. A large body of work investigating and developing technologies appropriate for cooling electronics with two phase flow boiling in parallel micro/mini-channels exists, but parallel channel two-phase flow is challenged by instability issues, particularly with non-uniform power maps. We utilize a significantly different approach to embedded cooling. Rather than moving coolant from one edge of the die to the other through long parallel channels, a dielectric coolant (R1234ze or similar) is fed in at the center of the die, moves through radially expanding channels, and exits at the edges of the die. This approach provides better energy efficiency and maximum critical heat flux with the resulting reduced flow path. The cooling capability was demonstrated on a specially constructed thermal test vehicle (Figure 25 a,b,c,d) designed to mimic the heat generation capability of real microprocessors without requiring actual transistor-based circuitry. In these studies, power densities of 350 W/cm² within an area measuring 3.6 mm x 4.8 mm representing a microprocessor core and 200 µm x 200 µm hot-spot power levels of more than 2 kW/cm² were shown to be effectively cooled with chip junction temperatures of < 60C as shown in Figure 26 [57. 58].

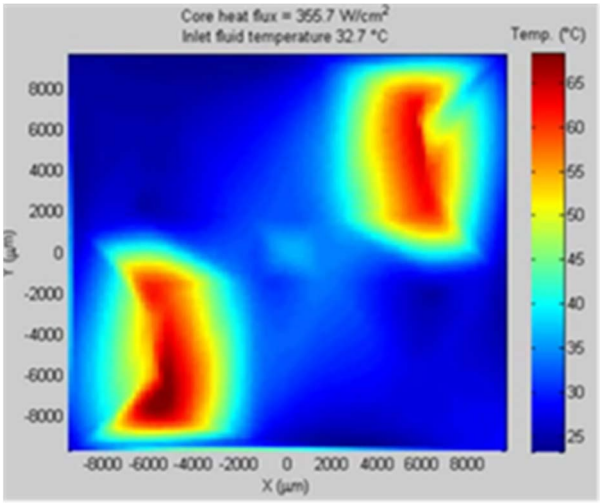

Fig 26: Interpolated visualization of the temperature profile of the thermal test vehicle [58], with two diagonal quadrants powered at 350 W/cm², Hot Spots 2000 W/cm² and Background 20 W/cm² heat flux. Total Power ~300 W.

3.4 Advanced thermal materials for thermal management

Several new materials are being explored from a research and development standpoint for enhancement of heat spreading, thermal interfaces, and underfill materials as described in [59-61], for the various conduction layers of heterogeneously integrated (and other) packages. Examples of such materials include cubic crystals, two-dimensional layered materials, nanostructure networks and composites, molecular layers and surface functionalization, and aligned polymer structures.

Figure 27 [59] depicts a 3D chip stack using advanced materials in the conduction heat flow path. The construction in Figure 27 includes details such as the front-end-of-line (FEOL) and back-end-of-line (BEOL) device and interconnect layers as well as controlled collapse chip connections (C4) and smaller µ-C4 features. Of special note is typical epoxy-based underfill materials that fill up the gaps between the 3D stacked dies. With low intrinsic thermal conductivities of 0.1–0.2 W/m-K [59] they yield a significant thermal resistance to the heat flow as also discussed previously in Section 2.2 (3D Chip Stack with Conduction Interfaces). Thus new underfill materials or composites need to be developed [59] with higher isotropic thermal conductivities to promote cross-plane heat conduction and die-to-die heat dissipation, while also enhancing in-plane (2D) heat spreading to mitigate hot spots in the power sources.

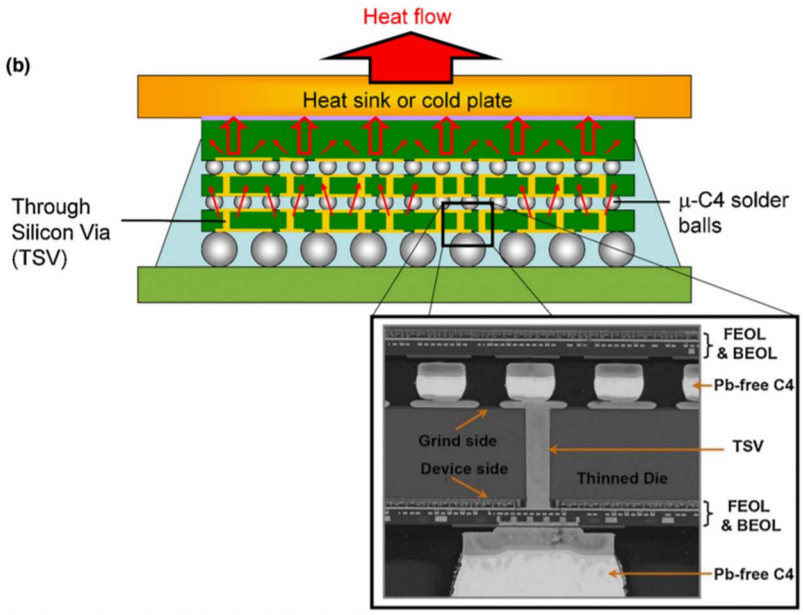

Figure 27: 3D chip stack with advanced materials in conduction heat flow path [59]

While Figure 27 is a valid example of a high-performance package, this opportunity for new materials is very much present for the Mobile space as well with inherent heat spreading challenges as discussed previously in Section 2.6 (Mobile Devices challenges). Indium Tin Oxide (ITO) is a material of choice for touch screens [59] in such mobile devices, but more recently materials such as carbon nanotubes (CNTs), graphene, thinSi membranes, and silver nanowires are being actively explored to solve thermal challenges [59].

3.5 Thermomechanical modeling for heterogeneous integration

The power dissipation and power density in future 2D-3D packages is expected to increase and the cross-talk between different components of the package will further aggravate the thermal management challenges. This will necessitate development of a multi-physics simulation tool with closely coupled thermal, mechanical and electrical models to enable iterative simulations and robust design. This tool should allow coupling between different scales, e.g., die to package and package to system (board), to consider the effect of design at these different scales. High heat flux components of packages will require single- or two-phase liquid cooling. The models for accurate prediction of two-phase fluid flow have not been developed yet. Physics-based models in combination with machine learning tools will be needed for high fidelity prediction of performance and design of these cooling technologies.

We discuss the needs and possible approaches for next-gen modeling and simulations tools. The vast majority of thermal/thermomechanical design rules in electronic design and packaging are based on finite element simulations post-electronic design. Robust thermomechanical models are not present in the electronic design and reliability flows, thus necessitating significant margins from the designers. Here we suggest a paradigm shift to better model, optimize and design for die and package level thermomechanical effects. The primary aim of this framework is to use a repository of finite element simulations packaged through a neural network engine and abstracted into usable design models. The following workflow (Figure 28) is proposed to enable this early absorption of thermal and mechanical models into design tools:

- Definition of the design space and execution of FEM simulations with combinatorial and probabilistic input parameters spanning geometrical descriptions, material properties and interface/boundary conditions across domains.
- Training Data: Output FEM state distributions and fields (electric field, power density, temperature, stress, strain etc.). Training and validation using an artificial neural network with feed-forward deep autoencoders (DAE).
- Deployment of the validated DAEs generated in (2) to accurately predict the non-linear and statistical behavior of a design with minimum computational and setup overhead.

Figure 28: Thermal/Multi-Physics Modeling for Heterogeneous Packages

Glass/Si based interposers or 3D packages with stacked die will allow integration of different functionalities with a wide range of power dissipation in both space and time. The efficient thermal management of hot-spots will require development of novel phase change materials, along with high-conductivity materials with anisotropic thermal properties. In addition, next-generation packages will need novel dielectrics, insulators and conducting materials. The accurate estimation of thermal properties of these materials and their interfaces will be necessary to develop predictive models. First-principle simulations in combination with machine learning tools will be beneficial in predicting properties of these materials with specification of uncertainty, which can be input to multi-physics modeling tools to understand their effect on packages, e.g., Design Space Definition shown in the workflow above.

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5.0 Thermal Technical Working Group Contributors

Madhusudan Iyengar	Avi Bar-Cohen	Ali Merrikh	Amr Helmy
Azmat Malik	Bahgat G. Sammakia	Baratunde Cola	Baris Dogruoz
Benson Chan	Bill Bottoms	Craig Green	Dhruv Singh
Gamal Refai-Ahmed	Jamal Yagoobi	Justin A. Weibel	Kamal Sikka
Kanad Ghose	Kenneth Goodson	Kevin P. Drummond	Li Shi
Mehdi Asheghi	Michael Barako	Michael J. Ellsworth	Peter de Bock
Ravi Mahajan	Rockwell Hsu	Satish Kumar	Sreekant.Narumanchi
Suresh V. Garimella	Timothy Chainer	Vadim Gektin	Victor Chiriac
Yoonjin Won	Yogi Joshi	Weihua Tang	William Chen

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