2020 Edition

Chapter 6: Aerospace and Defense

http://eps.ieee.org/hir

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Chapter 6: Aerospace and Defense

1. Executive Summary

Send corrections, comments and suggested updates to the TWG chair, using our HIR SmartSheet:

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The Aerospace and Defense segment of the semiconductor industry has unique needs in terms of technology, security, supply chain, and lifecycle. Heterogeneous integration is a critical technology that intersects all of these challenges, so a Heterogeneous Integration Roadmap (HIR) that specifically targets the unique requirements of Aerospace and Defense is needed. This Roadmap identifies challenges in 5-, 10-, and 15-year horizons and provides guidance on how to meet those challenges. This is, of course, a perpetual work-in-progress and will be updated as capabilities move forward and new requirements arise.

Initial Scope

This initial version of the A&D chapter is focused largely on challenges and requirements for the U.S. Aerospace and Defense Industry. The intent of the Heterogeneous Integration Roadmap is to create a document that provides guidance that is useful to the semiconductor community around the world, so the US-centric viewpoint should be seen as just the starting point for this work. There are certainly many technical challenges that are pervasive throughout the international A&D industry, such as reliability, bandwidth, thermal management, radiation hardening, long product development cycles and lifetime, and supply chain security, so much of the content can be generalized beyond the US Aerospace and Defense Industry. Future revisions of this chapter will reflect that broader scope.

2020 Update

The 2020 updates to this chapter include: 1) updates on government-funded heterogeneous integration programs, 2) recent market data, and 3) the 0.1 version of the A&D roadmap table (Section 12). Populating and refining the table in Section 12 will be the focus for the 2021 version of the Heterogeneous Integration Roadmap.

2. HIR Aerospace and Defense Working Group

2.1 Mission Statement for Aerospace and Defense TWG

The mission of the HIR Technology Working Group (TWG) for Aerospace and Defense (A-D) is to identify challenges, provide guidance, and recommend solutions to the A-D profession (industry, academia, and government) with sufficient lead time that they do not become roadblocks that prevent the continued implementation of leading-edge electronics in Aerospace and Defense systems.

There is the need to address heterogeneous integration technologies for new capabilities for embedded high-speed computing, cyber, sensors, C4ISR, signal processing, radar, and RF/analog, all while addressing unique constraints and requirements, such as security, reliability, small production volumes, and long lifecycle timelines. That progress is essential to the future growth of the industry and the realization of the promise of continued impact on aerospace, defense and security applications.

The approach is to identify the requirements for heterogeneous integration in the A-D electronics industry with 5-, 10- and 15-year horizons, determine the difficult challenges that must be overcome to meet these requirements and, where possible, identify potential solutions and synergies between the greater commercial sectors and the smaller A-D community.

2.2 The TWG for Developing the Heterogeneous Integration Roadmap for Aerospace and Defense

The Goal for the A-D TWG is to develop a roadmap for heterogeneously integrated components for applications in the Aerospace and Defense sector which want to leverage heterogeneous integration technologies that are available in the commercial marketplace but with special needs and challenges.

Specific goals:

- Identify the A-D–specific challenges in the next 5-, 10- and 15- year horizons
- Identify promising solutions and technologies
- Identify any unaddressed challenges and the types of solutions/technologies needed
- Document all of these as a chapter in the overall HIR document
- Continue monitoring and analyzing the A-D semiconductor and packaging space to update the roadmap in the next version of the HIR

Much of the content of this initial version of the A&D chapter is on 2.5D integration technologies, largely because of the industry's progress and focus on 2.5D, as well as significant overlap with commercial 2.5D approaches. We

anticipate that future revisions will add significant content on 3D integration and other approaches such as wafer-level fan-out as A&D requirements evolve and multiple solutions are needed.

3. Introduction and Motivation

For over 70 years, the US government (USG) has worked closely with the semiconductor industry to help foster the semiconductor ecosystem to what it is today. In the early years before the mass proliferation of consumer electronic devices, the government was the primary driver of technology. Many of the available technologies originated in USG-funded research and development (R&D) programs. Prominent examples include printed circuit boards, GaAs devices, micro-electro-mechanical systems (MEMS), the fundamental technology of the internet, global positioning systems (GPS), and much of the technology needed for 5G. Funding for development of transistors and then ICs in the '50's and '60's, with the USG as the primary initial customer, resulted in the moon landing 50 years ago. In recent years, commercial applications such as personal computers, mobile devices, and now the Internet of Things (IoT) have created an enormous production demand and business opportunity that is the primary focus of the semiconductor industry. As a result, microelectronics for A-D needs is a small fraction of the total semiconductor market and therefore has a diminished impact on industry roadmaps. Additionally, R&D investments by the Department of Defense have stagnated recently, as shown in Figure 3-1, although there are signs in 2020 that this is changing for semiconductors.

From an Aerospace-Defense (A-D) perspective, having a continued access to advanced semiconductor technology is important not only for national defense but for the country's economic vitality. In the recent US President's Council of Advisors on Science and Technology (PCAST) report, it states:

> "The global semiconductor market has never been a completely free market: it is founded on science that historically has been driven, in substantial part, by government and academia; segments of it are restricted in various ways as a result of national-security and defense imperatives; and it is frequently the focus of national industrial policies. Market forces play a central and critical role. But any presumption by U.S. policymakers that existing market forces alone will yield optimal outcomes – particularly when faced with substantial industrial policies from other countries – is unwarranted."[1]

3.1 National Defense Strategy (2018)[2]

The USG's National Defense Strategy was published in 2018. Key take-aways that highlight challenges include:

- "Platform electronics and software must be designed for routine replacement instead of static configurations that last more than a decade" and must also "Deliver performance at the speed of relevance."
- "New commercial technology will change society and, ultimately, the character of war. The fact that many technological developments will come from the commercial sector means that state competitors and non-state actors will also have access to them, a fact that risks eroding the conventional overmatch to which our Nation has grown accustomed."

Modern warfare is increasingly dependent on microelectronics capabilities that sense the environment, convert the signals into data streams, process the information, and generate a response. In this sense, A-D systems are quite similar to commercial systems that perform communications and computations, while taking advantage of the advancement of semiconductor density, functionality, and cost reduction due to Moore's Law. There is the ever-increased demand for more data throughput through wired and wireless systems. Cellular systems have migrated from 3G to 4G and now 5G architectures, which improves bandwidth ~10X with each generation. DoD systems for communications, radar, and sensing generally require wider bandwidths, higher dynamic range, and higher transmit power, as well as specialized frequency bands and security requirements that the commercial side does not require. Figure 3-2 highlights the direction of the next generation of warfare and enabling systems for a system-of-systems framework. The challenges in the A-D space overlap those in the commercial world but extend beyond those as noted above.

[1] https://obamawhitehouse.archives.gov/sites/default/files/microsites/ostp/PCAST/pcast_ensuring_long-term_us_leadership_in_semiconductors.pdf

[2] 2018 National Defense Strategy found at https://dod.defense.gov/Portals/1/Documents/pubs/2018-National-Defense-Strategy-Summary.pdf

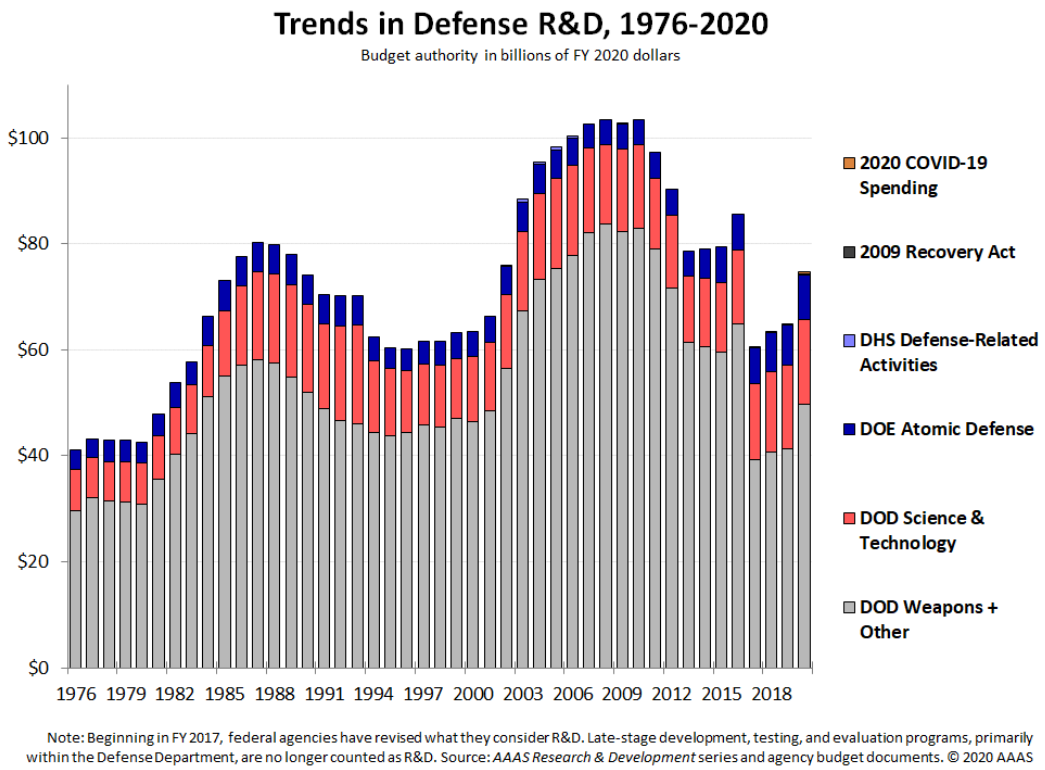


Figure 3-1. US DoD funding historical perspective[3]

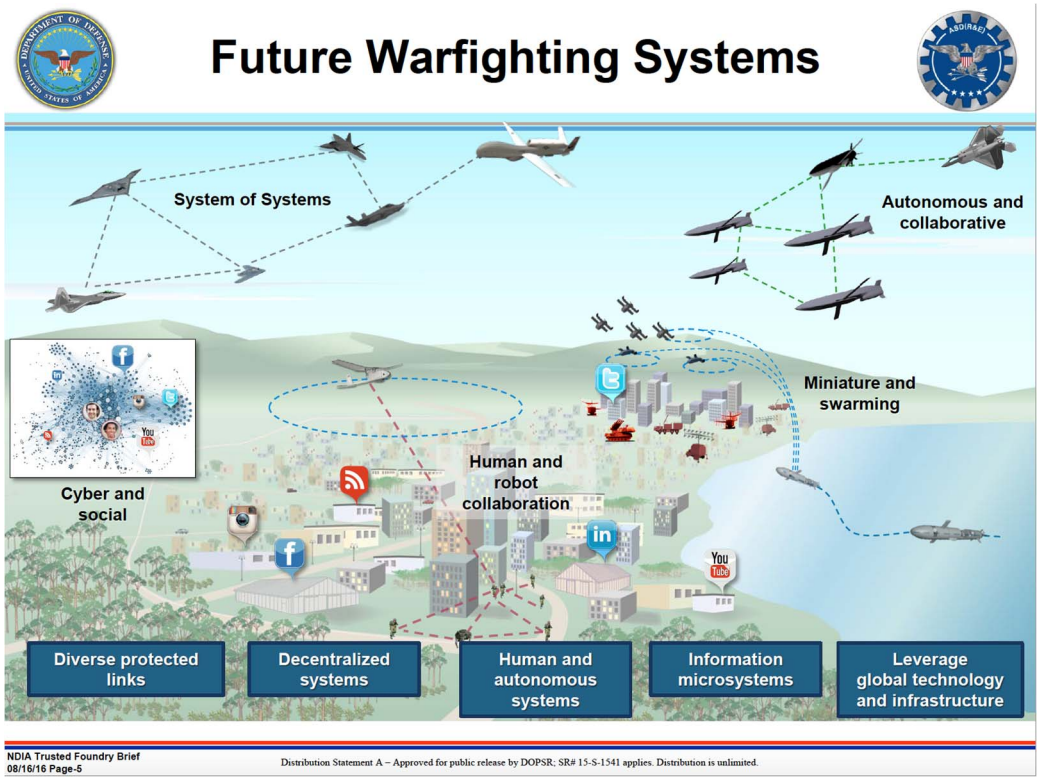


Figure 3-2. Notional future warfighting systems architecture

[3] https://www.aaas.org/programs/r-d-budget-and-policy/historical-trends-federal-rd

3.2 NDIA Trusted Microelectronics Study

In 2017, the National Defense Industrial Association (NDIA) conducted a study of Trusted Microelectronics which resulted in the following recommendations for action.[4]

Create a U.S. National Semiconductor Strategy

"The absence of a comprehensive national semiconductor strategy was viewed … as a major impediment to assuring access to critical national security technologies and to U.S. technological competitiveness."

Adapt DoD Acquisition Practices to Align with Commercial Market

Noting the "differences between DoD's acquisition practices and commercial sales priorities," the report "recommends defense programs be provided new methods to purchase technology on commercial terms after the commercial products have been evaluated for trustworthiness."

Increase DoD Market Influence

Since "the DoD's share of the semiconductor market has dramatically declined to less 1% share of today's semiconductors consumption and the Department's ability to gain access to needed microelectronics capabilities has correspondingly diminished, … increase market influence by exchanging research investment for access to commercial products; and, aggregating demand across DoD programs, other USG offices, and non-USG industries that have similar component and system integrity concerns."

Adopt New Trust and Assurance Models

"Defining the boundaries for assurance spectrums or 'tiers of trust' levels, and would cover component categories beyond ASICs."

Launch R&D to Achieve Trust/Security in Un-trusted Fabs

"Launching near-term research and development to address the security concerns of existing commercial technology capabilities, including Trusted 3D/2.5D integration, to leverage these capabilities for defense systems."

Two of the four NDIA Trusted Microelectronics Joint Working Groups (TM JWGs) studied the microelectronics landscape and made recommendations that relate to heterogenous integration. NDIA TM JWG Team 1 addressed the **Future Needs & System Impact of Microelectronics Technologies**, asking the following questions:[5]

- "What are the future microelectronics capabilities needed by defense contractors to maintain our technical advantage?"
- "Are there new hardware paradigms on the horizon that could be disruptive?"
    - SYSTEMS: System Needs and System Capabilities: What are the future requirements for DoD Systems?
    - ENABLING COMPONENTS: What are the emerging technologies enabling these capabilities at the component level?
    - ADOPTION: What are the risks regarding secure component availability (5-10 years) that enables system capabilities?

The HIR A-D chapter will attempt to ask similar questions and suggest some insight that pertains to Heterogeneous Integration for this community.

4. What is the Aerospace and Defense Sector?

Deloitte in its 2019 Global Aerospace and Defense Industry Outlook white paper[6] makes the following observations:

- The commercial aircraft order backlog is at its peak of more than 14,000, with about 38,000 aircraft expected to be produced globally over the next 20 years.
- Resurgence of global military spending as geopolitical risks increase worldwide.
- Space is becoming an important part of the defense ecosystem as warfare moves into the domain of space assets such as satellites for military operations including surveillance, communications and targeting.
- Changes in international trade agreements are likely to disrupt the global supply chain and increase costs.

[4] http://www.ndia.org/-/media/sites/ndia/divisions/working-groups/tmjwg-documents/tm-jwg-esr-v3.ashx?la=en

[5] http://www.ndia.org/-/media/sites/ndia/divisions/working-groups/tmjwg-documents/ndia-tm-jwg-team-1-white-paper-finalv3.ashx?la=en

[6] Deloitte 2019 Global aerospace and defense industry outlook, found at https://www2.deloitte.com/global/en/pages/manufacturing/articles/global-a-and-d-outlook.html

Although the USA dominates in A-D spending and revenue generation, other key regions are expected to contribute to the sector including China, France, India, Japan, the Middle East and the United Kingdom.

The Aerospace and Defense sector has been at the forefront of digital innovations, leading the way for other industries in the adoption of technologies.[7] The hierarchy can be shown as:

- End Customers (e.g., USG).
- System Primes (OEMs) who provide end-to-end system solution to the end-users.
- Subsystem Suppliers who provide vital subsystems including propulsion, command and control, electronic warfare, and structural subsystems to the Primes.
- Component Suppliers provide component parts including energetic and structural materials, microelectronics, cables, and connectors for prime and major subsystem providers.
- Pure Play Suppliers (materials, equipment, design, manufacturing, services to other supply chain players).

Figure 4-1. highlights the differences between the Commercial and Aerospace-Defense business models. Commercial products have very short lifecycles, whereas A-D products must be supported for decades. The cost of engineering for commercial products can be amortized over millions or billions of units whereas A-D products may be in the thousands, hundreds or lower. A-D Systems are generally insensitive to unit costs but they must operate in extreme environments and have demonstrated pedigree that is tracked over the product lifecycle.

Figure 4-1. Differences between the commercial and aerospace-defense business models[8]

5. Impact of Heterogeneous Integration on Aerospace and Defense Systems

Several characteristics of the A-D sector create unique challenges:

- High Performance – Need access to leading silicon nodes and advanced packaging technologies to maintain advantage in specific technical metrics (e.g., digitization over wide bandwidths and at high dynamic range)
- High Reliability – Need to survive in harsh environments, prioritize human safety in high-risk environment
- Long Product Lifecycles – Need to manage parts obsolescence and upgradability
- Low Volumes – Need access to supply chain that provides high product mix, and business models where NRE is managed without high volumes for amortization
- Security – Need secure domestic supply chain and/or verification technologies

[7] REPORT TO CONGRESS: Fiscal Year 2016 Annual Industrial Capabilities, found at https://www.businessdefense.gov/Portals/51/Documents/Resources/2016%20AIC%20RTC%2006-27-17%20-%20Public%20Release.pdf?ver=2017-06-30-144825-160

[8] NDIA: Trusted Microelectronics Joint Working Group: Future Needs & System Impact of Microelectronics Technologies, found at http://www.ndia.org/divisions/working-groups/tmejwg/final-team-reports

Heterogeneous integration is a factor in all of these challenges, whether by adding new twists to the challenges with multiple device technologies or by solving some of them with modular designs and assemblies. Most specifically, heterogeneous integration directly addresses the high-performance challenge for the A-D sector. Monolithic System on a Chip solutions are becoming increasingly limited for A-D applications. Sustaining Moore's Law by increasing the core count on a die is not feasible as memory access bottlenecks prevail and die size and complexity become prohibitively expensive. Diversity in process nodes and materials are needed (CPUs, GPUs, FPGAs) for enhancing performance, energy efficiency and programmability. Similarly, RF/mm-wave devices and data converters are needed for communications and sensing. Heterogeneous integration offers a way to address these limitations and sustain Moore's Law through interconnect length reductions and optimal combinations of different device technologies. The A-D sector must adapt and adopt innovation and market drivers from the commercial semiconductor industry.

What are the metrics to consider?

There are numerous metrics to consider for heterogeneous integration in the A-D sector, and they can vary by application (communications, radar, EW, etc.). Categorized metrics include:

- Performance: data rate, latency, TFLOPs, insertion loss, isolation, dynamic range
- Energy/Power: energy per bit, TFLOPS/Joule, leakage power
- Interfaces: signaling protocols, error correction, interconnect lengths, ESD
- Thermal: maximum junction temperature, total device power, device power density, hot spot power density, thermal test standards
- Electrical: power distribution losses to components inside package, losses in conversion, peak inductive noise, harmonic noise
- Reliability/Availability: MTBF, radiation hardness, metric related to graceful degradation on component failures, product lifetime (driving component availability)

6. What is Heterogenous Integration

(Refer to other HIR Chapters for the definitions of 2D, 2.1D, 2.5D and 3D heterogeneous integration)

Figure 6-1 provides a definition of heterogeneous integration, noting that heterogeneity arises from the material, component type, circuit type, node, bonding/interconnect method, or source of the devices.

The A-D component and sub-systems can benefit from the well-stated benefits of heterogeneous Integration at all levels. In this chapter, the focus is on 2.5D integration, since many 2D and 2.1D integrations and solutions are already in wide use. Chip-and-wire assembly is a standard process. Wafer-level and fan-out packages, although attractive for high-volume applications and miniaturization, may not be sufficient for high performance and harsh environments. 2.5D technology, which is represented by High Bandwidth Memory (HBM) and other applications with stacked devices on organic substrates or silicon interposers, is attractive for A-D since this approach enables higher performance and high-density integration while leveraging conventional technology building blocks.

In many ways, the A-D users have similar needs as the HPC use case. Therefore, it is recommended that A-D users leverage capabilities and supply chain partners from the HPC ecosystem (Figure 6-2).

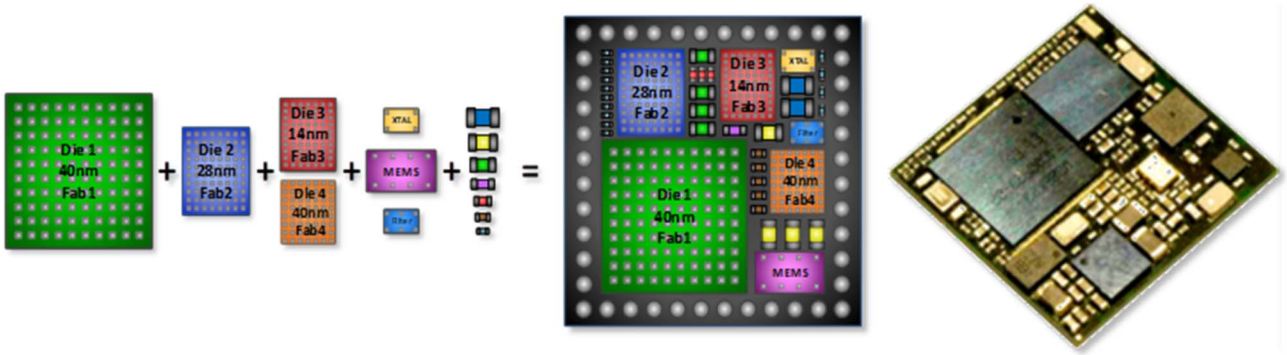


Figure 6-1. Heterogeneous integration can mean heterogeneous by material, component type, circuit type, node, bonding/interconnect method, and sources. (Source: ASE)

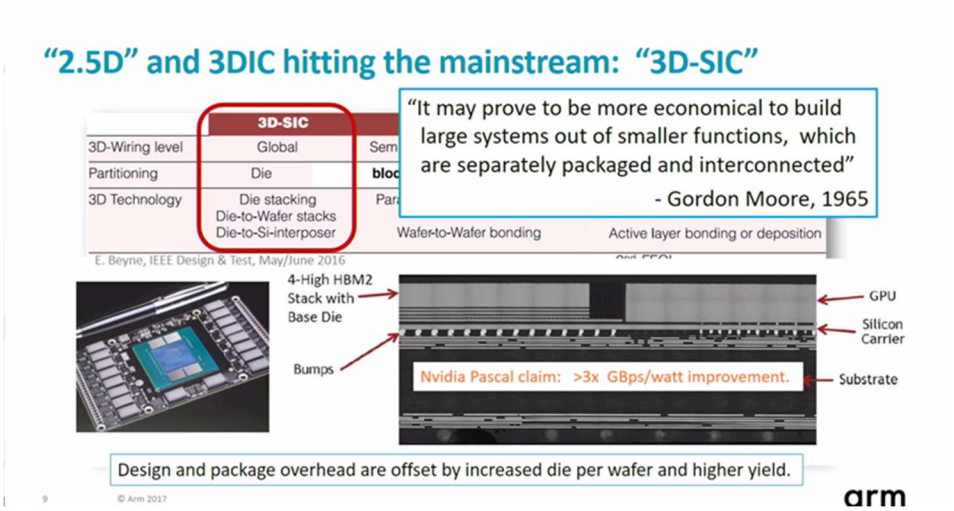


Figure 6-2. "2.5D" and 3DIC are widely used by high performance computing

7. 2.5D Heterogeneous Integration Progress

Heterogeneous integration via 2.5D technology is approaching mainstream status, with industry leaders such as Xilinx, Intel, Nvidia, and AMD using it in their leading products. They have identified the benefits of splitting up silicon functionality, whether to improve yield with smaller chips, as Xilinx did with their pioneering FPGA "slices," or to enable the integration of different types of devices. To summarize:

- Chiplets (smaller pieces of silicon) will enable their silicon architects to ship more powerful processors more quickly.[9]
- Modularity facilitates shorter time-to-market to mix and match different chiplets linked by shorter data interconnections, instead of implementing new complex SOC designs for the entire system.
- 2.5D can reduce design costs and risk by having a larger portion of the design composed of reused IP blocks that are assembled on an interposer rather than integrated in a new IC design.

Notable industry leaders see this trend. AMD's Mark Papermaster said "I think the whole industry is going to be moving in this direction." Similarly, Intel's technologists see that same thing. Ramune Nagisetty, a senior principal engineer at Intel, calls it "an evolution of Moore's law."

DARPA has led the way in advancing Heterogeneous Integration Technology through a number of programs, as shown in Figure 7-1 and Figure 7-2. The DARPA DAHI program demonstrated the feasibility of 2.5D HI for integration of CMOS devices with high-performance III-V devices through both die-to-wafer and wafer-to-wafer bonding techniques. The DARPA CHIPS program (which is still on-going) is developing a 2.5D chiplet ecosystem and a set of standard interfaces for chiplet to chiplet communications.

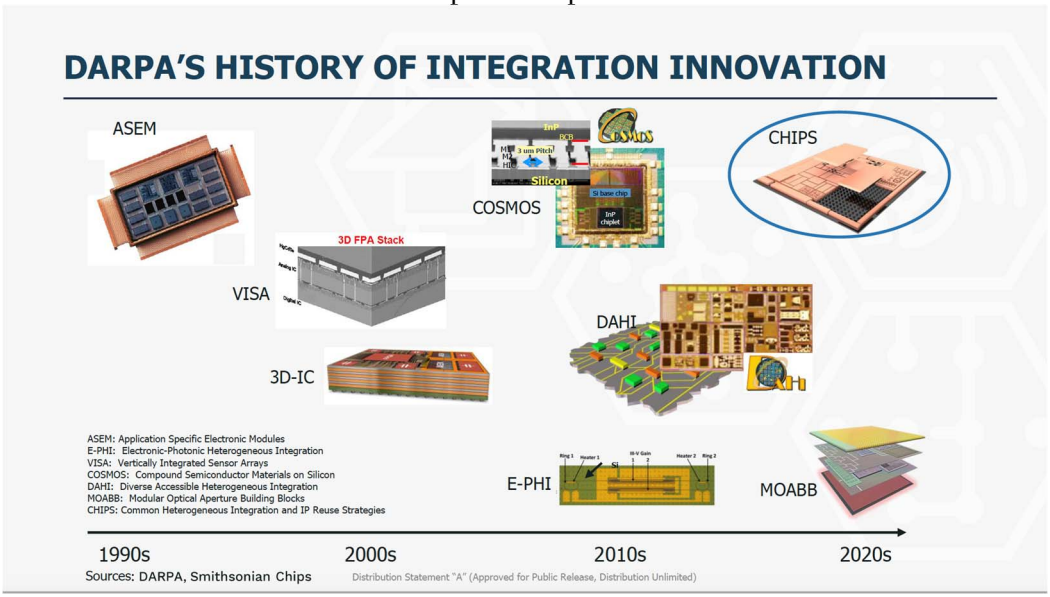


Figure 7-1. DARPA's history of integration innovation

[9] Found at https://www.wired.com/story/keep-pace-moores-law-chipmakers-turn-chiplets/

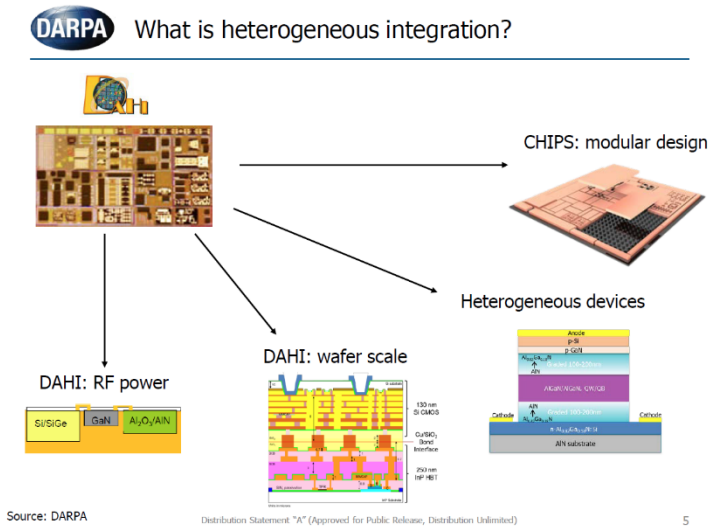


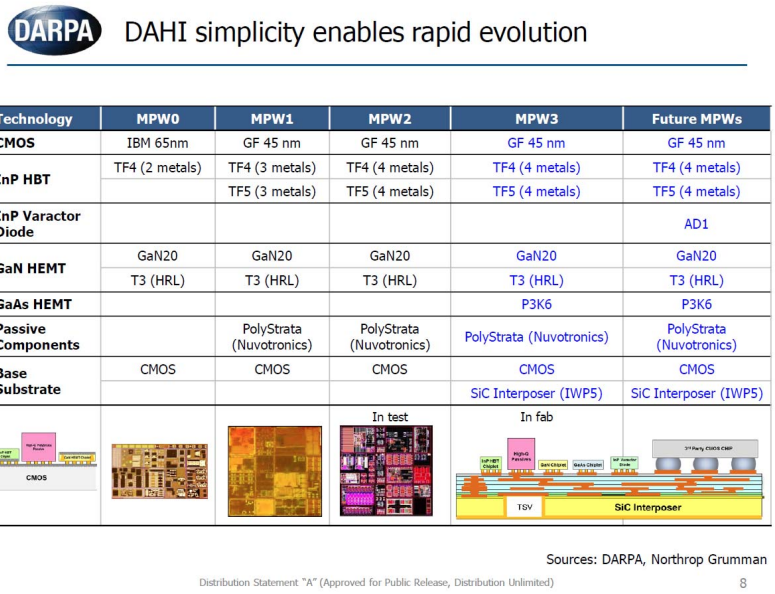
Figure 7-2. DARPA heterogeneous integration[10]

7.1 DARPA DAHI Program

Daniel Green reported on the Progress and Prospects of Heterogeneous Integration at DARPA and summarized the progress made on a number of programs.[11]

The Diverse Accessible Heterogeneous Integration (DAHI)[12] Foundry Technology program was designed to establish an accessible, manufacturable technology for device-level heterogeneous integration of a wide array of materials and devices (including, for example, multiple electronics and MEMS technologies) with complex silicon-enabled (e.g., CMOS) architectures on a common silicon substrate. This program culminated in accessible foundry processes of DAHI technology and demonstrations of advanced microsystems with innovative architectures and designs that leverage heterogeneous integration. By enabling the ability to 'mix and match' a wide variety of devices and materials on a common silicon substrate, circuit designers can select the best device for each function within their designs. This integration would provide DoD systems with the benefits of a variety of devices and materials integrated in close proximity on a single chip, minimizing the performance limitations caused by physical separation among devices.

Some of the key results are summarized in Figures 7-3, 7-4, 7-5, 7-6 and 7-7 below. The program demonstrated capabilities that would not have been possible in monolithic implementations, while uncovering several challenges in design, fabrication, and assembly along the way. The DAHI program has served as the baseline for heterogeneous integration at DARPA and beyond in the DoD.



Technology	MPW0	MPW1	MPW2	MPW3	Future MPWs
CMOS	IBM 65nm	GF 45 nm	GF 45 nm	GF 45 nm	GF 45 nm
InP HBT	TF4 (2 metals)	TF4 (3 metals)	TF4 (4 metals)	TF4 (4 metals)	TF4 (4 metals)
		TF5 (3 metals)	TF5 (4 metals)	TF5 (4 metals)	TF5 (4 metals)
InP Varactor Diode					AD1
GaN HEMT	GaN20	GaN20	GaN20	GaN20	GaN20
	T3 (HRL)	T3 (HRL)	T3 (HRL)	T3 (HRL)	T3 (HRL)
GaAs HEMT				P3K6	P3K6
Passive Components		PolyStrata (Nuvotronics)	PolyStrata (Nuvotronics)	PolyStrata (Nuvotronics)	PolyStrata (Nuvotronics)
Base Substrate	CMOS	CMOS	CMOS	CMOS	CMOS
				SiC Interposer (IWP5)	SiC Interposer (IWP5)

Figure 7-3. DAHI demonstrates CMOS to III-V IC integration using 2.5D techniques

[10] Daniel Green, "DARPA's CHIPS Program and Making Heterogenous Integration Common," 3D-ASIP 2017, 6 December 2017

[11] Daniel Green, "Progress and Prospects of Heterogeneous Integration at DARPA," found at http://www.meptec.org/Resources/6%20-%20Green.pdf

[12] DARPA DAHI Program: https://www.darpa.mil/program/dahi-foundry-technology

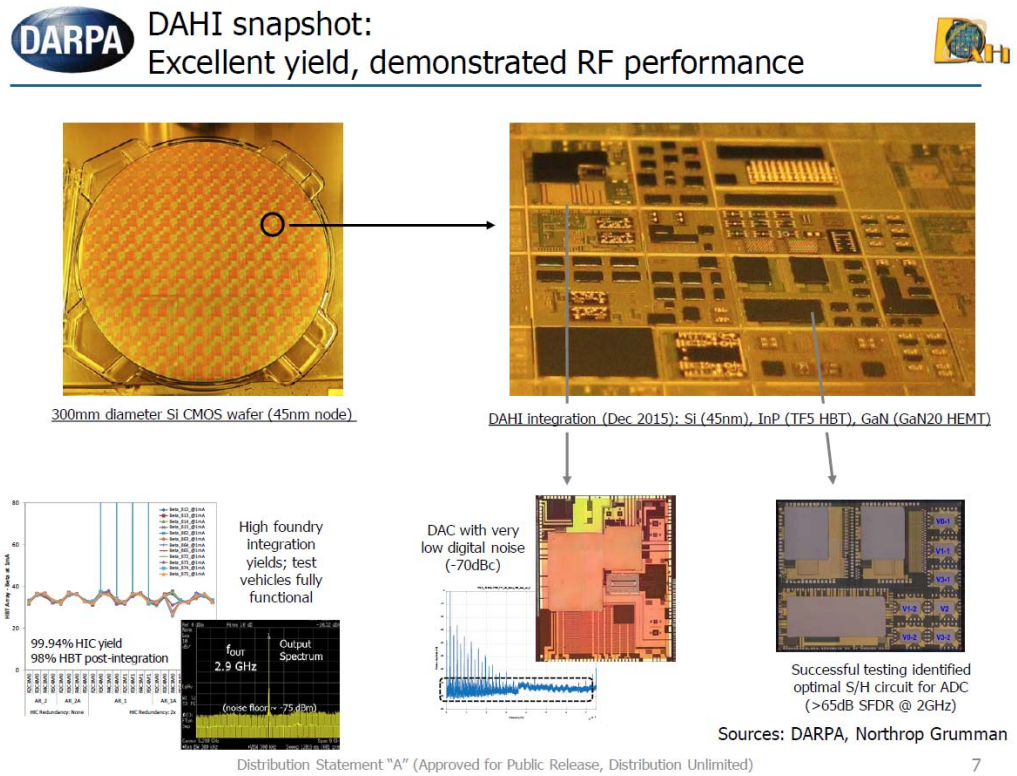


Figure 7-4. DARPA DAHI technologies addressed high-performance RF performance and integration of CMOS digital functions

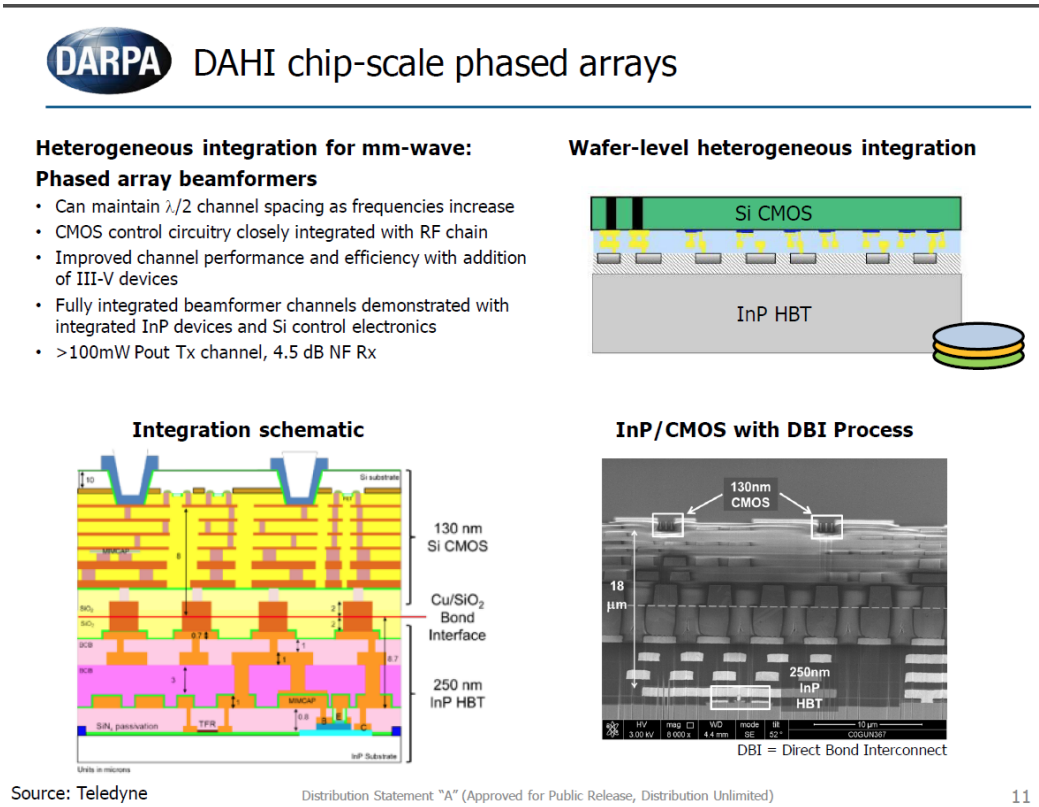


Figure 7-5. DARPA DAHI used DBI process to achieve transistor-level integration with Si CMOS and InP HBT devices

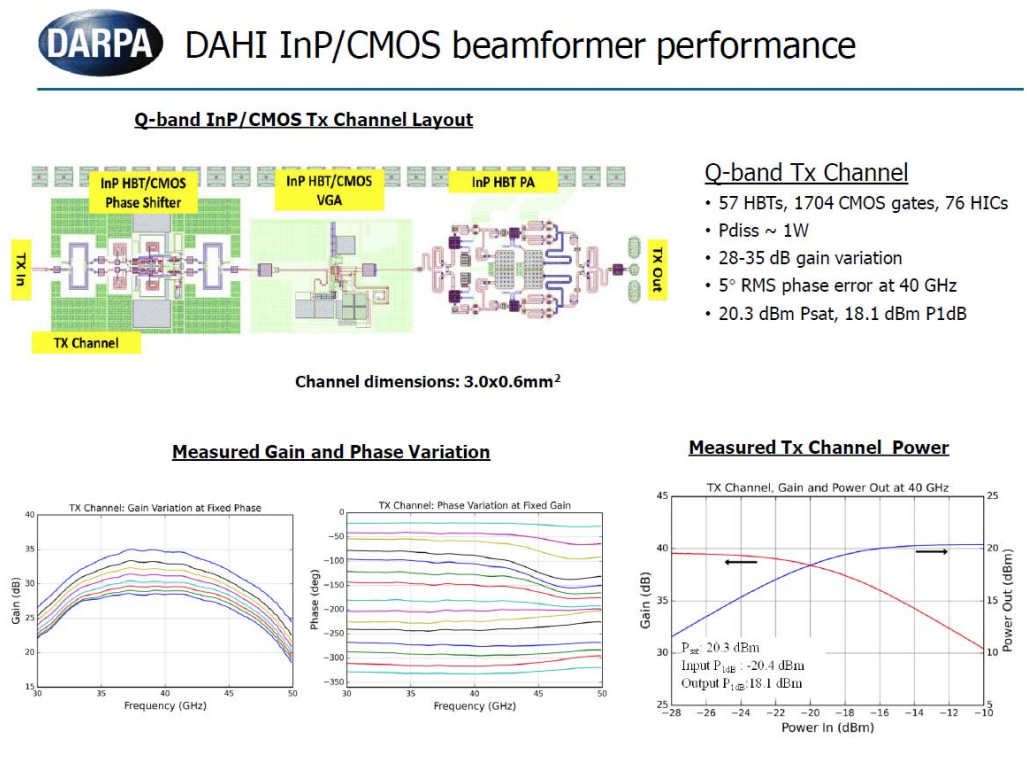


Figure 7-6. DARPA DAHI demonstrated optimum millimeter-wave transmit capability through matching the best transistor for each RF function

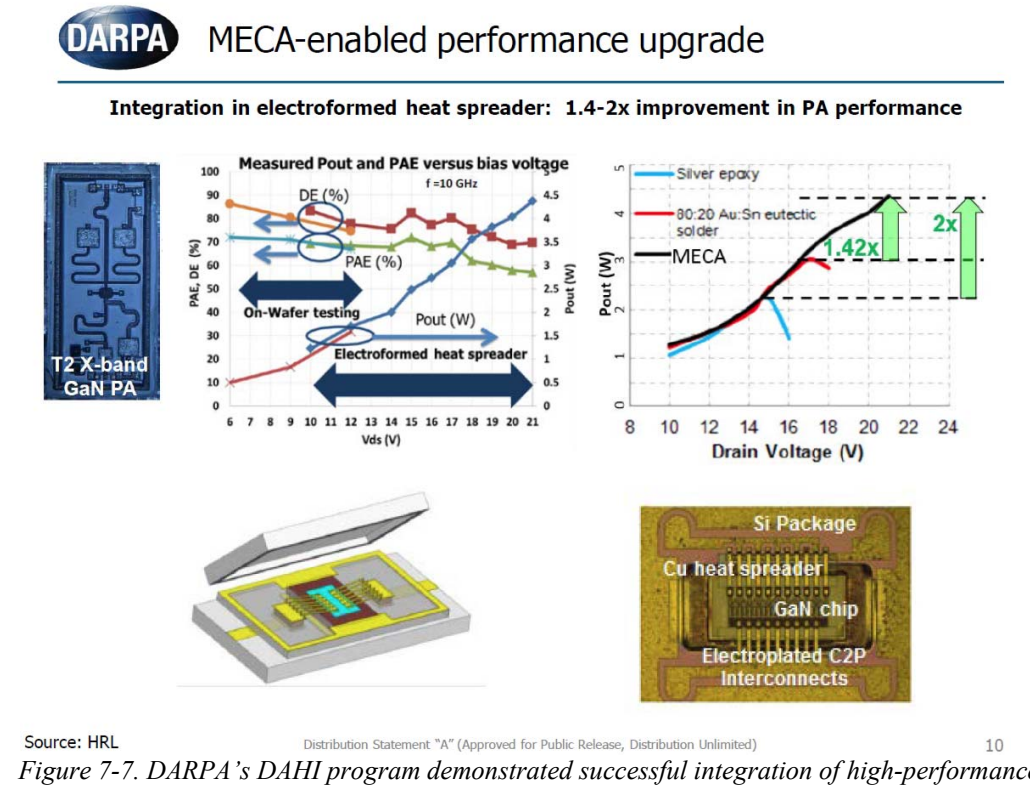


Figure 7-7. DARPA's DAHI program demonstrated successful integration of high-performance III-V device technologies with CMOS.

7.2 DARPA CHIPS Program

The DARPA CHIPS program goals are to:[13]

- Establish and demonstrate common interface standards
- Enable the assembly of systems from modular IP blocks built with these established standards
- Demonstrate reusability of the modular IP blocks via rapid design iteration

A chiplet is a functional, verified, modular re-useable physical IP block. They can be processors, converters, memory, waveform generators, accelerators, filters, etc.

A major achievement in the first 12 months of the program was the adoption of Intel's Advanced Interface Bus (AIB) as the low-power die-to-die electrical interface. AIB offers a 1-Gbps per lane SDR transfer rate for control signals and a 2-Gbps DDR transfer rate for data. A demonstration module with an Intel FPGA and several other chips was developed and manufactured in the CHIPS program.

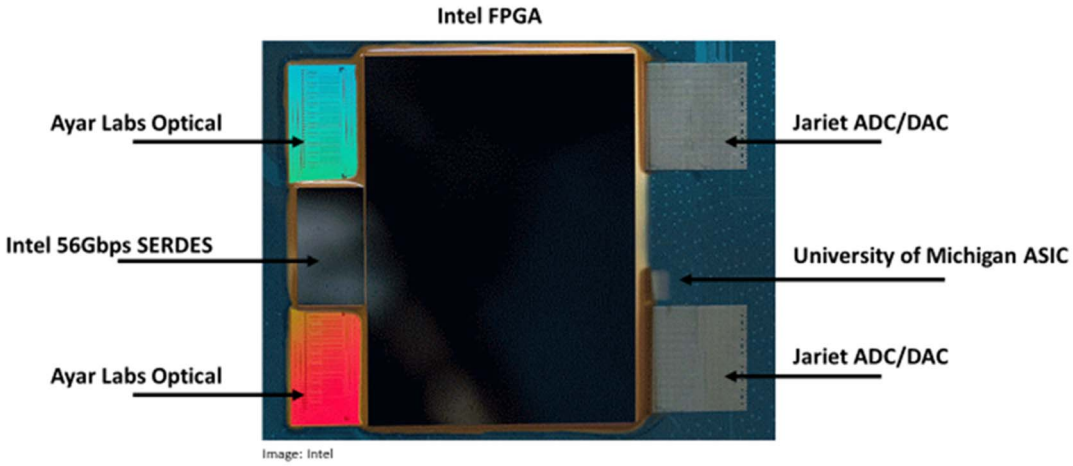


Figure 7-8. Example of CHIPS-inspired SiP that includes sensors, ASIC, FPGA, CPU, Memory and I/O using AIB Interface (Intel)

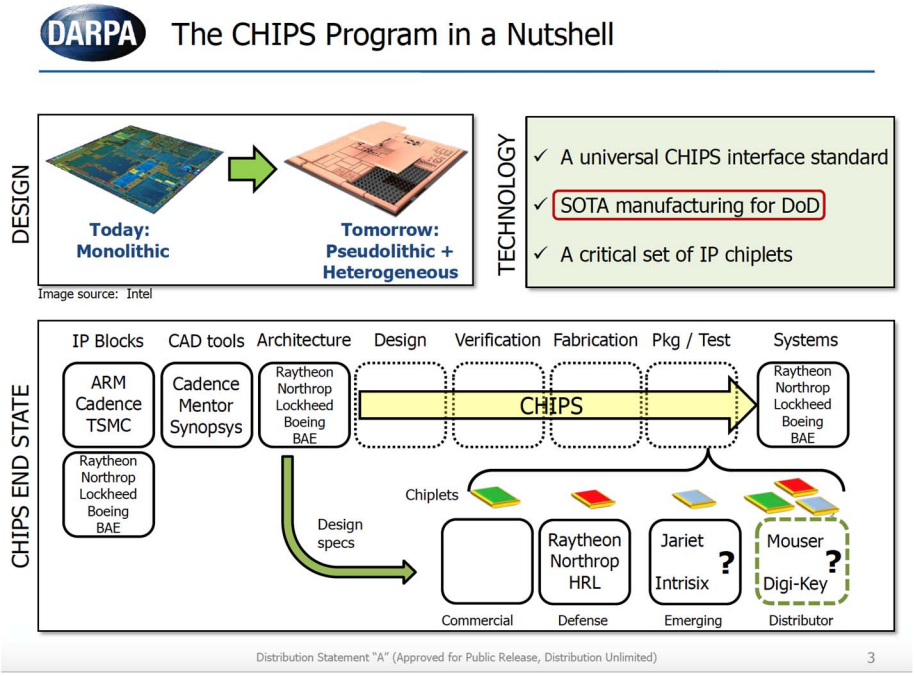


Figure 7-9. DARPA CHIPS program objectives to foster a chiplet ecosystem

[13] https://www.3dincites.com/2018/10/iftle-396-darpa-envisions-chips-as-new-approach-to-chip-design-and-manufacturing/

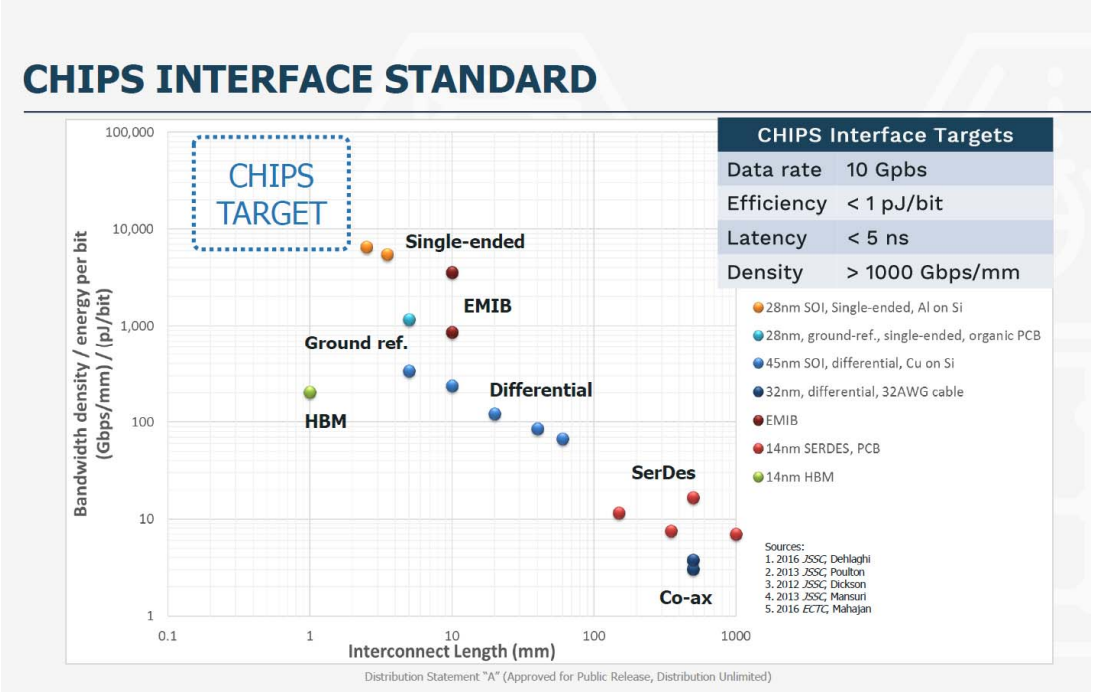
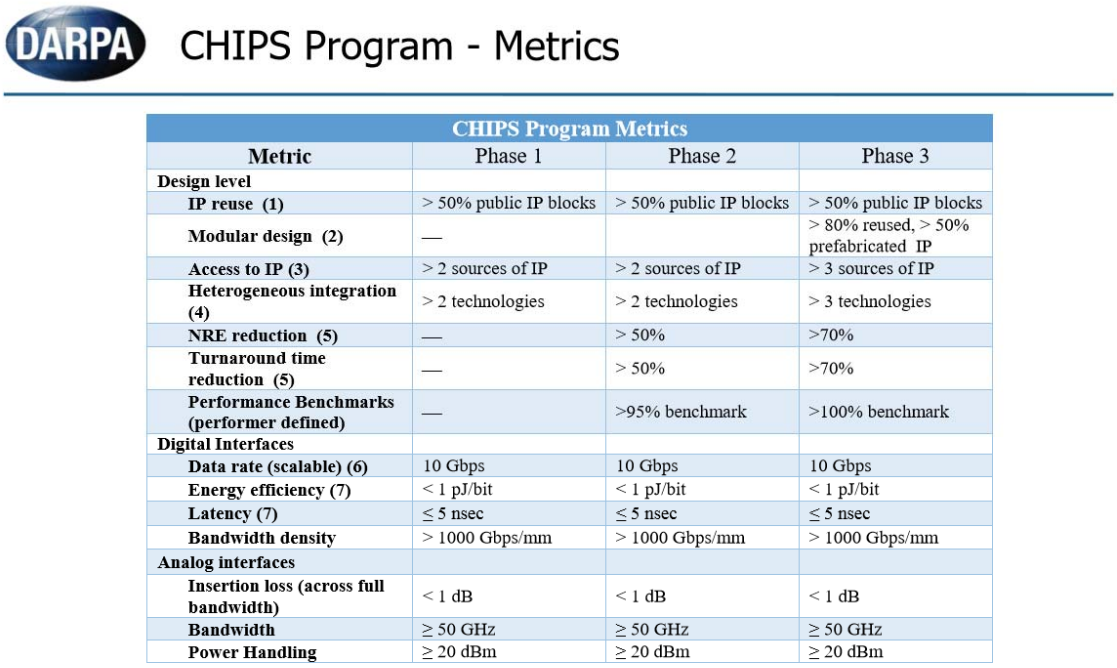


Figure 7-10. CHIPS Interface Standards – ERI Summit



CHIPS Program Metrics			
Metric	Phase 1	Phase 2	Phase 3
Design level			
IP reuse (1)	> 50% public IP blocks	> 50% public IP blocks	> 50% public IP blocks
Modular design (2)	—		> 80% reused, > 50% prefabricated IP
Access to IP (3)	> 2 sources of IP	> 2 sources of IP	> 3 sources of IP
Heterogeneous integration (4)	> 2 technologies	> 2 technologies	> 3 technologies
NRE reduction (5)	—	> 50%	>70%
Turnaround time reduction (5)	—	> 50%	>70%
Performance Benchmarks (performer defined)	—	>95% benchmark	>100% benchmark
Digital Interfaces			
Data rate (scalable) (6)	10 Gbps	10 Gbps	10 Gbps
Energy efficiency (7)	< 1 pJ/bit	< 1 pJ/bit	< 1 pJ/bit
Latency (7)	≤ 5 nsec	≤ 5 nsec	≤ 5 nsec
Bandwidth density	> 1000 Gbps/mm	> 1000 Gbps/mm	> 1000 Gbps/mm
Analog interfaces			
Insertion loss (across full bandwidth)	< 1 dB	< 1 dB	< 1 dB
Bandwidth	≥ 50 GHz	≥ 50 GHz	≥ 50 GHz
Power Handling	≥ 20 dBm	≥ 20 dBm	≥ 20 dBm

Notes:
1. Public IP is defined as IP blocks available through commercial vendors or shared among performers.
2. Reuse is defined as existing or previously designed IP that is re-implemented into the current system. Prefabricated IP is defined as IP blocks already physically instantiated.
3. Valid sources of IP must be those that are outside of the performer team.
4. Various Silicon process nodes, RF passives, or compound semiconductor devices.
5. The non-recurring engineering (NRE) cost and turnaround time will be compared against a benchmark design.
6. Minimum bus/lane data rate and should be capable of scaling to higher data rates.
7. Performance relating to transferring data between chiplets compared against a benchmark design.

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Figure 7-11. DARPA CHIPS interface metrics

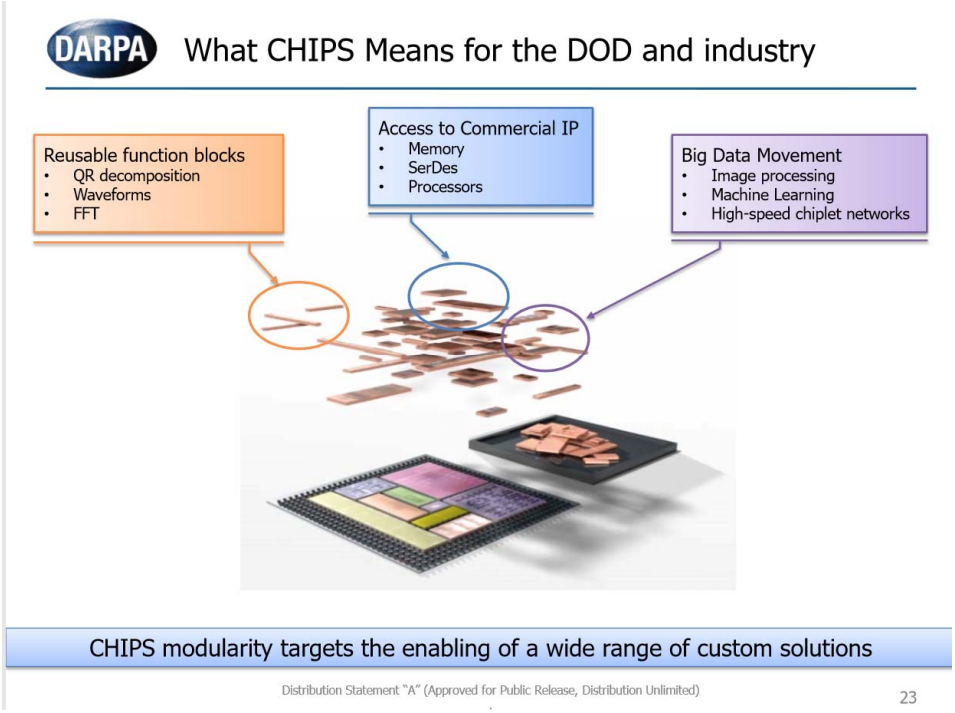
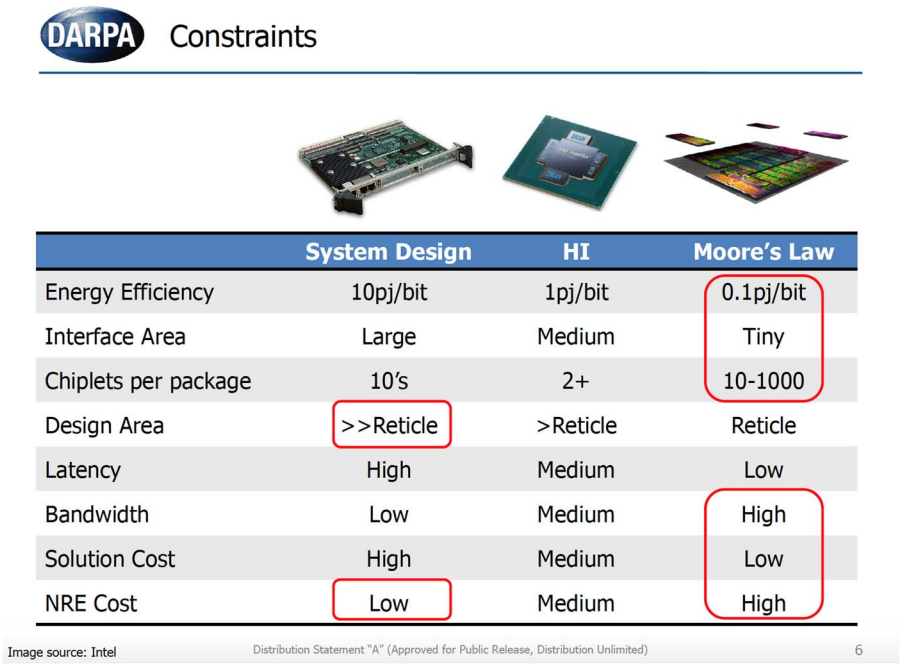


Figure 7-12. CHIPS modularity supports IP-re-use and access to high-speed data movement



	System Design	HI	Moore's Law
Energy Efficiency	10pj/bit	1pj/bit	0.1pj/bit
Interface Area	Large	Medium	Tiny
Chiplets per package	10's	2+	10-1000
Design Area	>>Reticle	>Reticle	Reticle
Latency	High	Medium	Low
Bandwidth	Low	Medium	High
Solution Cost	High	Medium	Low
NRE Cost	Low	Medium	High

Figure 7-13. CHIPS's objectives are to bridge the gap between board-level and SOC level metrics

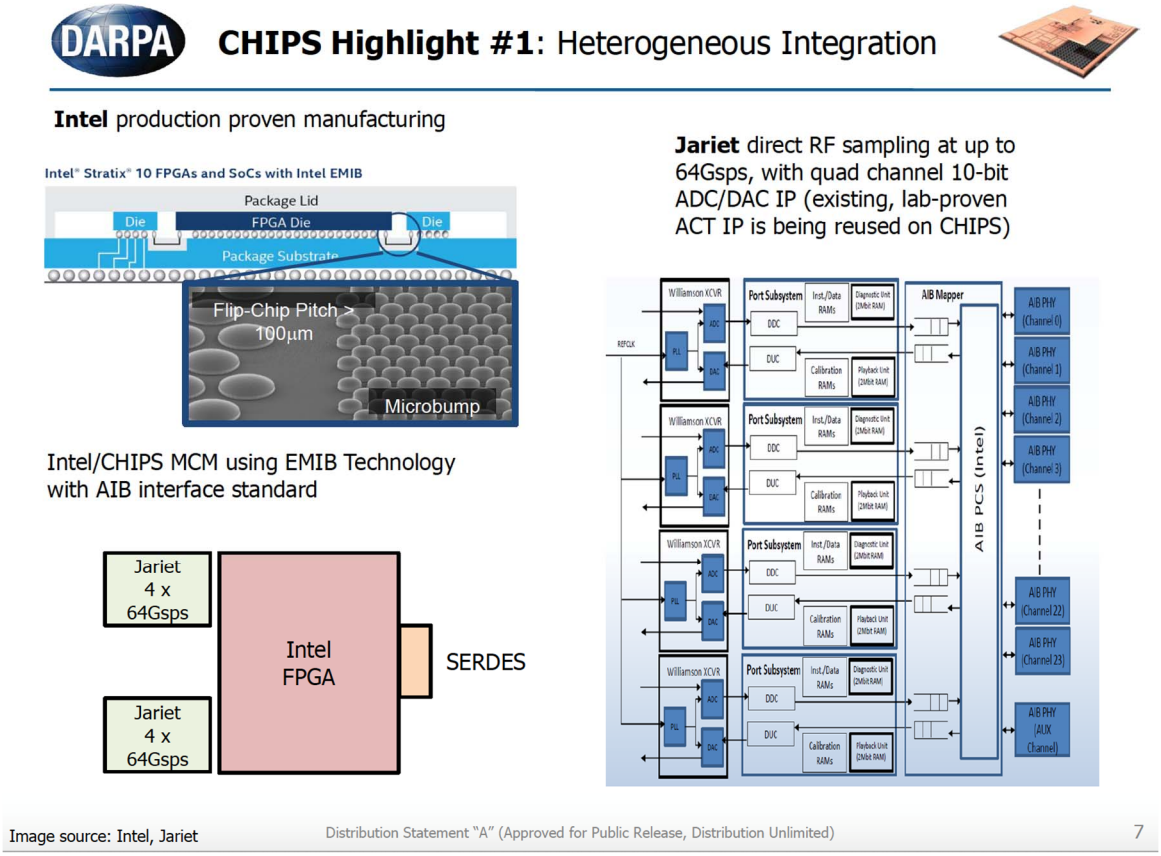


Figure 7-14. DARPA CHIPS will demonstrate high-data-rate I/O between an Intel FPGA and data-converters

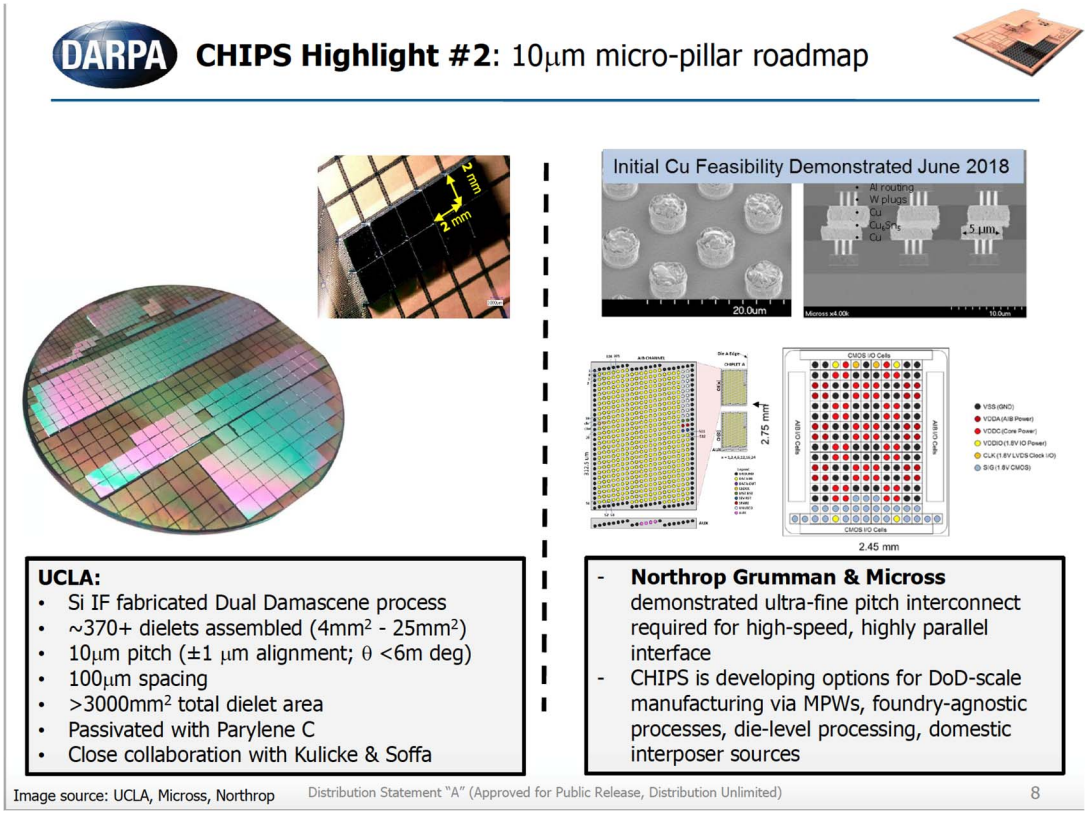
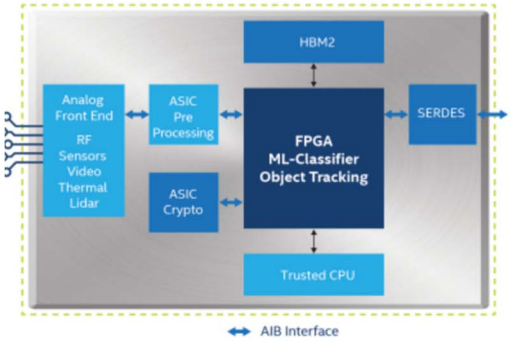


Figure 7-15. DARPA CHIPS Supports R&D for Fine-Pitch Interconnects at 10um Pitch with 100um Chiplet to Chiplet Spacing

Chiplet Standardized Interfaces



Intel's Advanced Interface Bus (AIB) is a die-to-die PHY level standard that enables a modular approach to system design with a library of chiplet intellectual property (IP) blocks.

AIB uses a clock forwarded parallel data transfer mechanism similar to DDR DRAM interfaces. AIB is process and packaging technology agnostic—Intel's Embedded Multi-Die Interconnect Bridge (EMIB) or TSMC's CoWoS* for example.

Intel now provides the AIB interface license royalty-free to enable a broad ecosystem of chiplets, design methodologies or service providers, foundries, packaging, and system vendors.

- AIB was supported by the DARPA CHIPS program.
- AIB specification is now available to the electronics community

Figure: *example of a possible heterogeneous system in package (SiP) that combines sensors, proprietary ASIC, FPGA, CPU, Memory and I/O using AIB as the chiplet interface.*

Figure 7-16. Intel Advanced Interface Bus (AIB) specification enables modular design[14]

7.3 DARPA PIPES Program

DARPA's program Photonics in the Package for Extreme Scalability (PIPES) is a program that builds on CHIPS by incorporating photonic devices in a heterogeneous integration ecosystem. The vision is summarized below, and recent progress included a demonstration by Intel and Ayar Labs. (https://www.darpa.mil/news-events/2020-03-25)

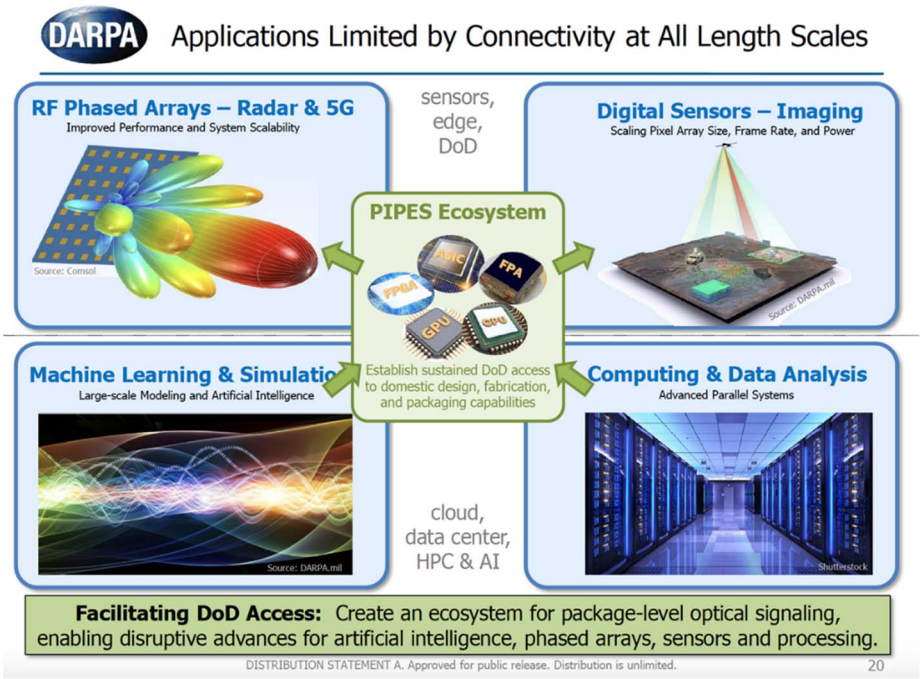


Figure 7-17: DARPA's PIPES program addresses HI by incorporating photonics (https://www.darpa.mil/attachments/DARPA_PIPES_Proposers_Day_Slides_Gordon_Keeler.pdf)

8. 3D Heterogeneous Integration

True 3D Heterogenous Integration (Figure 8-1), once developed, will provide monolithic levels in device-to-device spacing with interconnect distances in the 2 to 5um range. Significant technology challenges still exist and must be overcome to achieve the desired results. Section 8.1 describes the DARPA 3DSoC program which pushes the integration envelope to demonstrate ultra-low latency and ultra-low power I/O operations that will be needed for many AI/ML applications.

[14] Found at https://www.intel.com/content/www/us/en/architecture-and-technology/programmable/heterogeneous-integration/overview.html

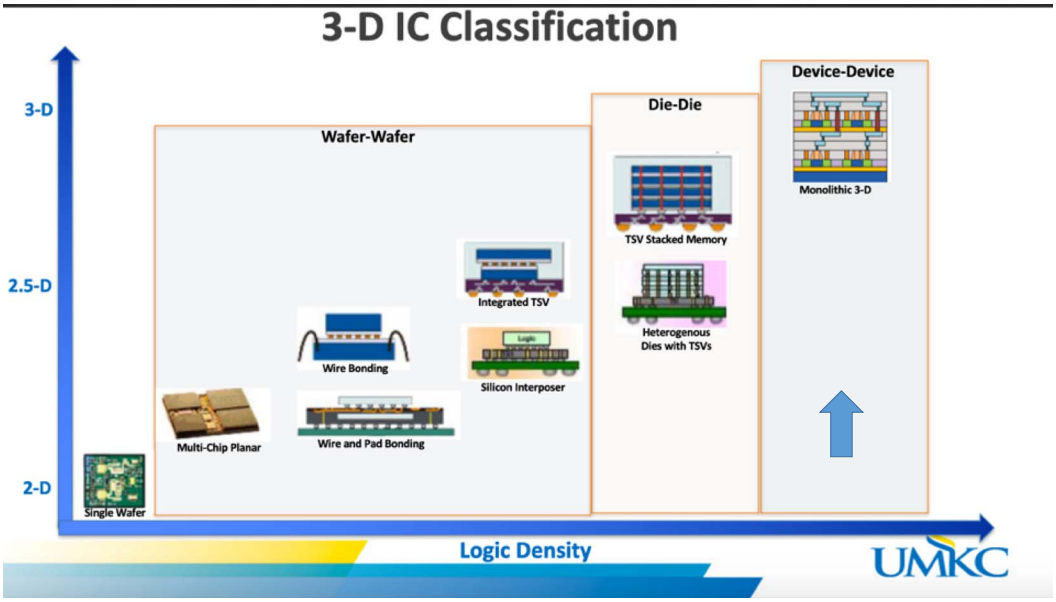


Figure 8-1. 3D integration technology is an active area of research

8.1 DARPA 3DSoC Program

A pervasive challenge in leading-edge electronic systems is the time and power required for communication between processors and memory. This "memory bottleneck" it often the primary limit on system performance. Heterogeneous integration begins to address this by enabling closer integration of processor and memory devices, and DARPA recently initiated the Three Dimensional Monolithic System-on-a-Chip (3DSoC) program to further develop the technology required to build logic, memory, and input/output (I/O) on a single die. This approach will leverage established lithography nodes but improve performance via 3D integration. Figure 8-2 illustrates this approach where progress is made via 3D integration rather than further advances following Moore's Law. Figure 8-3 shows more detail of the envisioned 3D integration of novel device types.

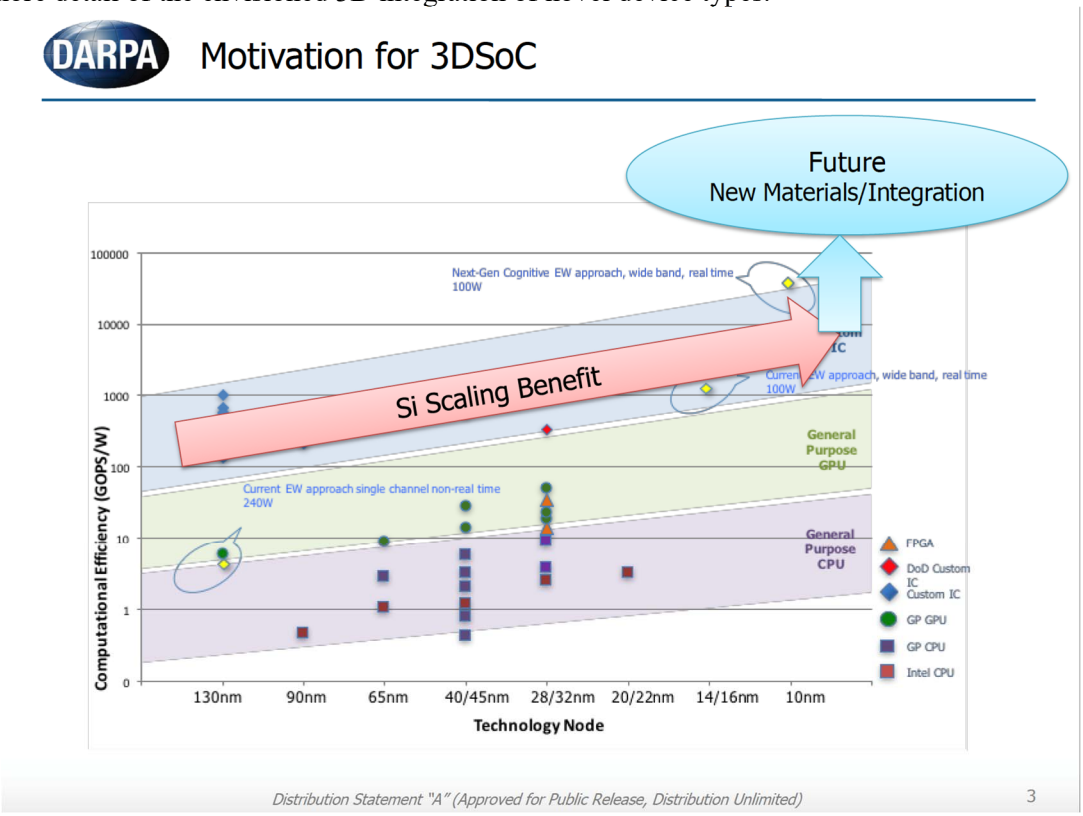


Figure 8.2 The DARPA 3DSoC program attacks the end of Moore's Law by the reduction of interconnect distances through vertical integration

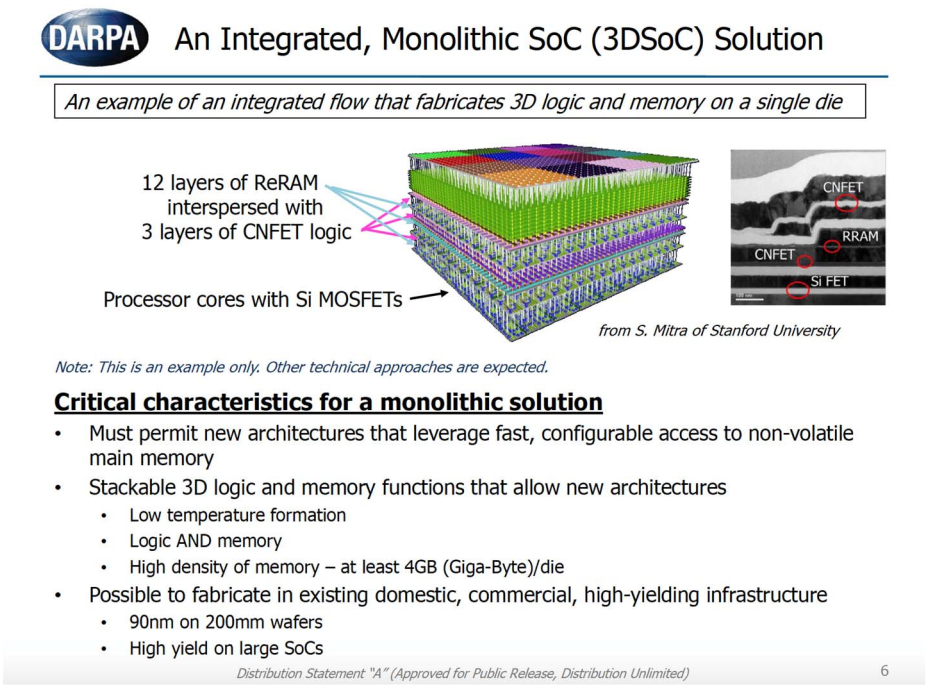
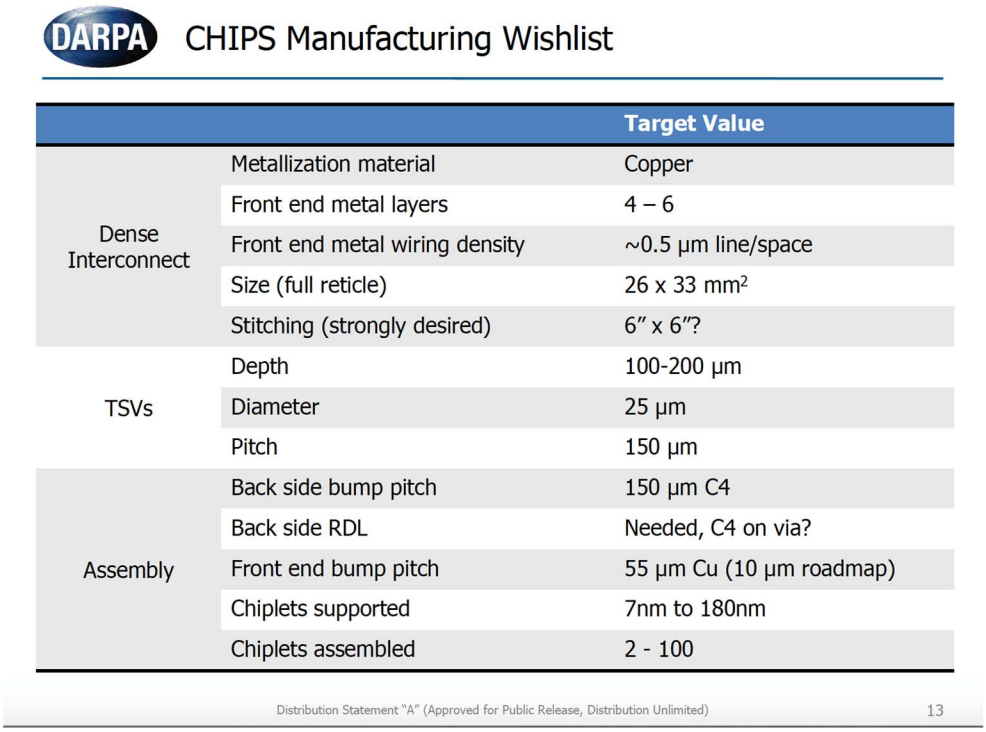


Figure 8-3. DARPA 3DSoC will demonstrate the tight integration of CNFET logic with ReRAM to have similar performance of FinFETs while using 90nm fabrication line

9. Outlook for Next 5 to 10 Years

9.1 DARPA CHIPS 2.0 (3 to 5 Years)

DARPA CHIPS is now seeking to foster a design and manufacturing chiplet eco-system for DoD users. Figures 9-1 and 9-2 show the requirements for silicon interposers, based on findings during Phase 1 of the CHIPS program. As progress is made, the A-D Chapter will be updated with the outcomes.



		Target Value
Dense Interconnect	Metallization material	Copper
	Front end metal layers	4 – 6
	Front end metal wiring density	~0.5 µm line/space
	Size (full reticle)	26 x 33 mm^2
	Stitching (strongly desired)	6" x 6"?
TSVs	Depth	100-200 µm
	Diameter	25 µm
	Pitch	150 µm
Assembly	Back side bump pitch	150 µm C4
	Back side RDL	Needed, C4 on via?
	Front end bump pitch	55 µm Cu (10 µm roadmap)
	Chiplets supported	7nm to 180nm
	Chiplets assembled	2 - 100

Figure 9-1. CHIPS wishlist for chiplet ecosystem

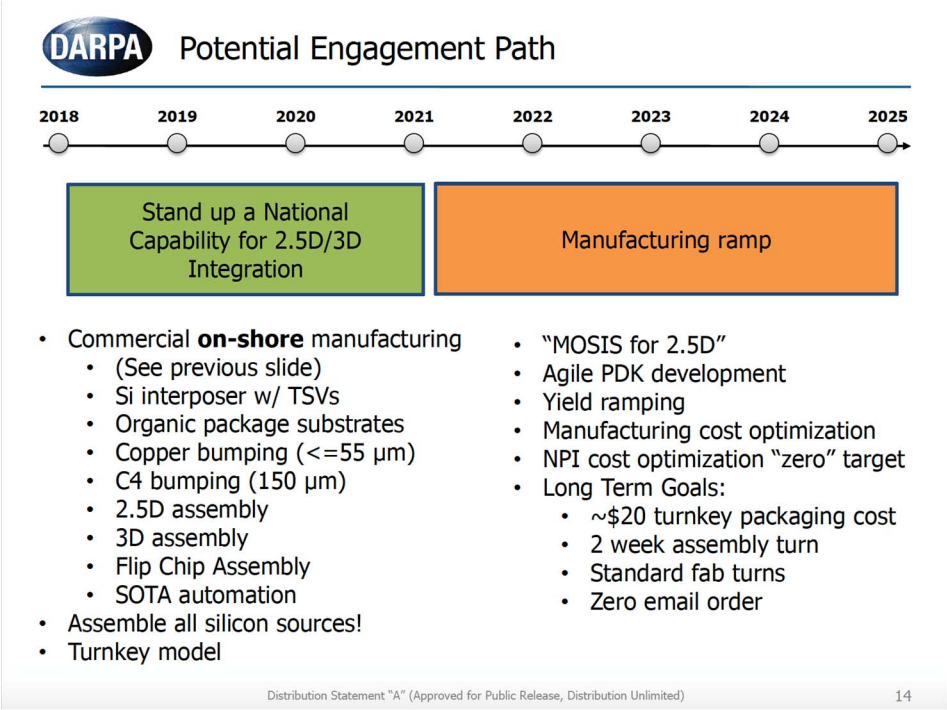


Figure 9-2. Timeline for CHIPS 2.0 vision

9.2 NSWC SHIP (3 to 5 Years)

With the lack of an established domestic manufacturing base for interposer-based HI as noted above, the State-of-the-art Heterogeneous Integrated Packaging (SHIP) program was created by the Naval Surface Warfare Center (Crane, IN). The vision is shown below (Figure 9-3), and some high-level metrics are shown as well (Figure 9-4). The program is divided into SHIP-Digital and SHIP-RF, with Intel and Xilinx selected for Phase 1 on the digital side, and Northrop Grumman, Qorvo, GE Research, and Keysight Technologies selected for RF. Each of those teams created a plan in Phase 1 to establish a self-sustaining HI manufacturing capability as a commercial entity, for either digital or RF applications. The government is willing to make a significant initial investment, but the primary goal is for that capability to be self-sustaining. It was recently announced that Intel was selected for SHIP-Digital Phase 2, and Qorvo was selected for SHIP-RF Phase 2. We expect to include an update on the continuation of the SHIP program in the 2021 edition of HIR.

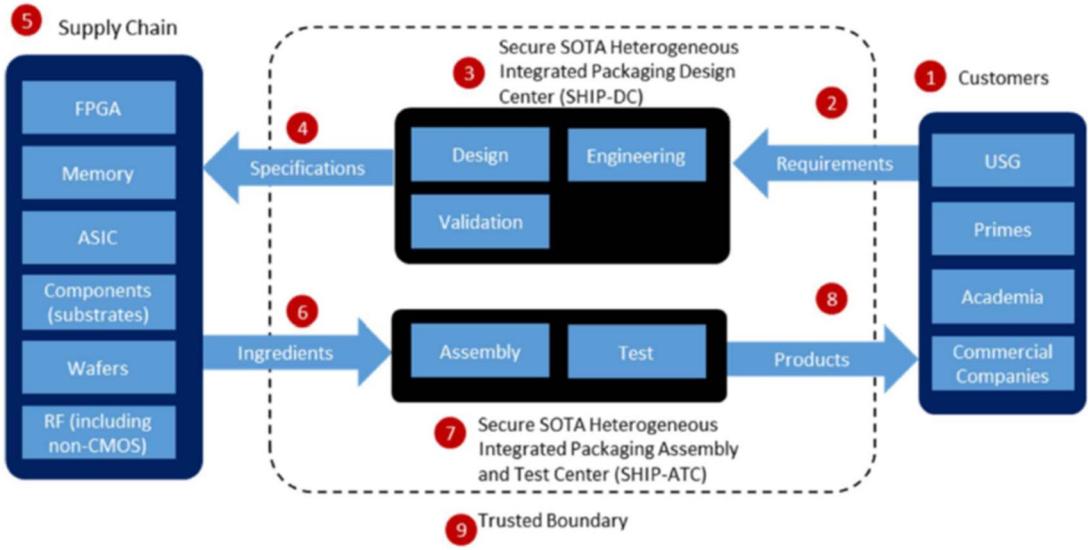


Figure 9-3. Notional design and prototyping flow in the SHIP program

Table 3 General Capacity and Capability for the SHIP-ATC

Category	IOC	FOC	Scale
Capacity: Volume (annual)	1k+	10k+	100k
Silicon interposer	Required	Required	Required
Organic interposer	Preferred	Required	Required
Utilize SOTA COTS FPGA[1] and programmable devices	Required	Required	Required
Structured ASIC	Preferred	Preferred	Required
Security	ITAR	ITAR	Classified
Number of Chips/Package[2]	4	8	12+
Supply Chain target	>50% US	>75% US	>90% US
Can process singulated die	Required	Required	Required
Can process up to 300mm wafers	Preferred	Required	Required
Can process 200mm wafers	Preferred	Preferred	Required

[1] Must include ability to integrate and test SOTA FPGA (<14nm), not required for RF centric applications

[2] Could include, but not limited to, memory, ADC/DAC, transceivers, optical couplers, ASIC, structured ASICs, etc.

Figure 9-4. High-level metrics for the SHIP program

9.3 New Legislation for Government Funding for Semiconductor Manufacturing (5 Years)

It is notable that semiconductor manufacturing is getting a lot of visibility with the proposed "CHIPS for America Act." These incentives and investments are substantial – on the order of $25B – and it is clear that the focus is on manufacturing. It is called out specifically in each top-line bullet (Figure 9-5). There is also $5B for Advanced Packaging, in the form of a National Manufacturing Institute. This is where the Heterogeneous Integration Roadmap could help frame what is needed there, and we expect to explore this collaboration in 2021. An additional point is the broad reach of the investments – DARPA, NSF, DoE, Dept of Commerce. That is an indicator that these manufacturing needs are not just for defense purposes. National security in electronics reaches beyond those traditional defense-specific requirements.

Figure 9-5. Proposed investment by the US Government in semiconductor manufacturing

9.4 Modular Single-Wafer Fabrication (5 to 10 Years)

Recent research in Japan is developing a concept called “minimal fab” which is an early example of the type of solution that could enable high-mix, low-volume production of semiconductors with approaches more typical of high-volume manufacturing. Small lots manufactured in this low-overhead approach could be an enabler for heterogeneous integration, especially for low to medium volumes as in A&D.

TOKYO Semiconductor start-up NEITAS has succeeded in creating semiconductor components in 20 hours – just a fraction of the time normally required – using a "minimal fab," a system that can produce even a single wafer with low capital spending. The breakthrough was confirmed jointly with Toyohashi University of Technology in Toyohashi, Aichi Prefecture. The company plans to set up a contract fabrication plant in Okinawa by the end of the year with the aim of achieving 10 billion yen ($88.4 million) in sales by 2020.[15]

The minimal fab was born at the National Institute of Advanced Industrial Science and Technology (AIST) in Tsukuba, Ibaraki Prefecture. It can manufacture semiconductors using small wafers just 12.5mm, or 0.5 inch, in diameter. Masks are not required because of novel lithography. Using a maskless technology developed at Toyohashi University, the equipment is capable of defining 0.8 micron dimensions. Although this is quite coarse for CMOS FEOL, this is in the right ballpark for BEOL linewidths, so the most advanced lithography tools are not needed. Clean rooms are also unnecessary because the processing is performed in enclosed spaces within the equipment.

Figure 9-6. Minimal modular wafer fabrication technology

At "SEMICON Japan 2017"[16], Minimal Fab exhibited their equipment that houses self-contained processing capability for wafer cleaning, and exposure for wafers as small as 0.5 inch. A minimal shuttle container is used to move the wafer between processing machines. This type of equipment is suitable for small-lot production and is useful for research and development with drastically reduced capital costs. Minimal Fab is working with Disco, Ishii Craft Research Institute, Apic Yamada and others to foster a minimal-equipment ecosystem. Yokogawa Solution Service[17] will act as a contact point to order and sell various equipment from different manufacturers.[18]

[15] https://asia.nikkei.com/Business/Biotechnology/Minimal-fab-tech-promises-faster-cheaper-chip-production

[16] https://www.ewarrant-sec.jp/article/%E3%81%8B%E3%81%AE%E3%81%86%E3%81%A1%E3%81%82%E3%82%84%E3%81%93%E3%81%AE%E3%80%8Csemicon-japan-2017%E3%80%8D%E3%83%AC%E3%83%9D%E3%83%BC%E3%83%88/

[17] https://www.yokogawa.com/yjp/biz/semi/minimal-fab.htm?nid=left

[18] https://eetimes.jp/ee/articles/1712/18/news033.html

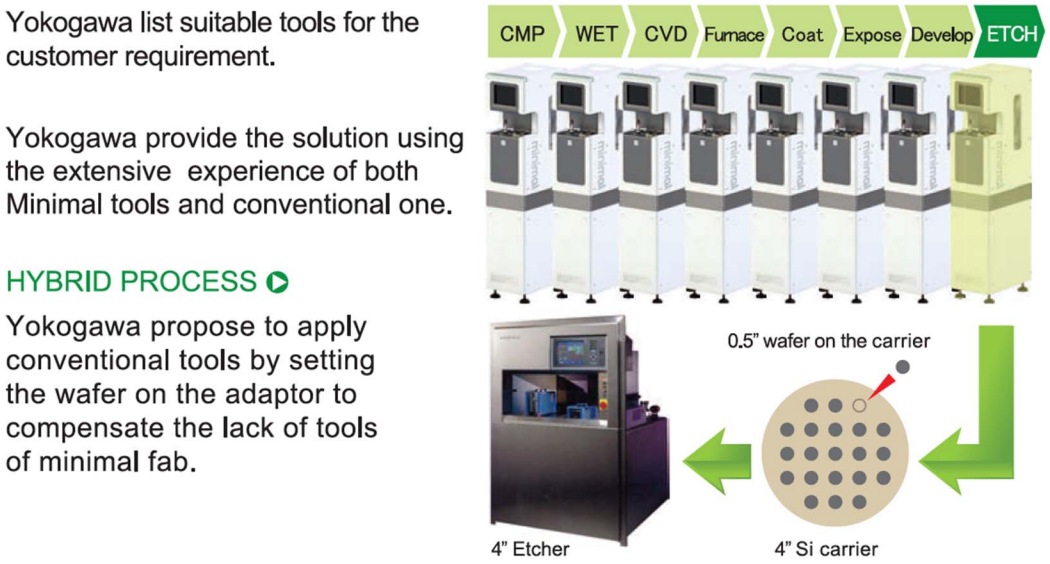


Figure 9-7. Minimal Fab's approach to low-volume semiconductor fabrication without clean-room

In 2019, the Minimal Fab approach was used to fabricate ICs for use in space electronics (Figure 9-8), in a joint effort with Japan Aerospace Exploration Agency (JAXA) and Japan's National Institute of Advanced Industrial Science and Technology (AIST). While this is still in development, it is an interesting proof point for a new approach to semiconductor manufacturing that could prompt additional work on concepts that could help address the specific challenges of A&D electronics.

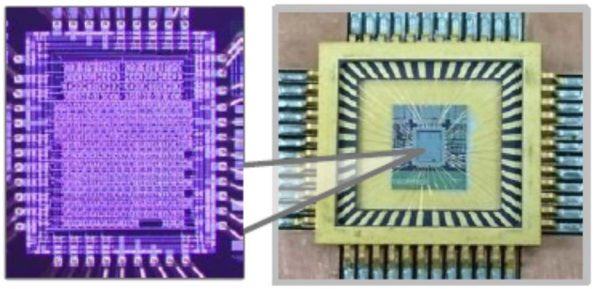


Figure 9-8. This device was made with Minimal Fab's equipment, for use in space electronics. The chip is 2 mm x 2.5 mm, with 1338 transistors. (https://global.jaxa.jp/press/2019/05/20190510a.html)

10. DARPA Electronics Resurgence Initiative (ERI)

In 2018, DARPA's Microsystem Technology Office (MTO) launched the Electronics Resurgence Initiative (ERI)[19]

- Today's critical Department of Defense (DOD) systems and platforms rely on advanced electronics to address national security objectives.
- To help tackle obstacles facing a half-century of electronics advancement, DARPA launched the Electronics Resurgence Initiative (ERI) – a five-year, upwards of US$1.5 billion investment in the future of domestic electronic systems.

Figure 10-1 shows the updated vision of ERI from DARPA's ERI Summit in August 2020. Heterogeneous integration is the cornerstone of many ERI programs, facilitating capabilities possible only with a diversity of devices.

[19] https://www.darpa.mil/news-events/electronics-resurgence-initiative-summit

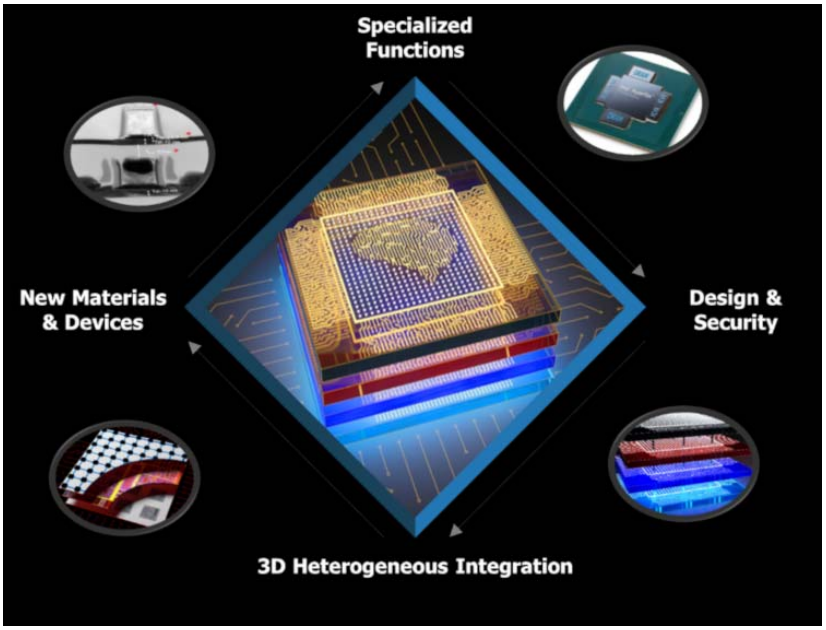


Figure 10-1. DARPA's Electronics Resurgence Initiative is structured around heterogeneous integration (https://eri-summit.darpa.mil/what-is-eri)

11. Supply Chain

11.1 International Supply Chain

The NDIA Trusted Microelectronics Team 1 Report asks: "Increasing Supply Chain Complexity: Commercially available capability (complex global infrastructure involved in SOTA designs; Fabs, IP, Packaging, Testing, etc.) is rapidly increasing, accomplished through a complex disaggregated supply chain that is fragile and subject to compromise. How can it be safely utilized?"[20]

- Foundries concentrated in Asia
- Chinese players growing
- Increasingly consolidated among leaders

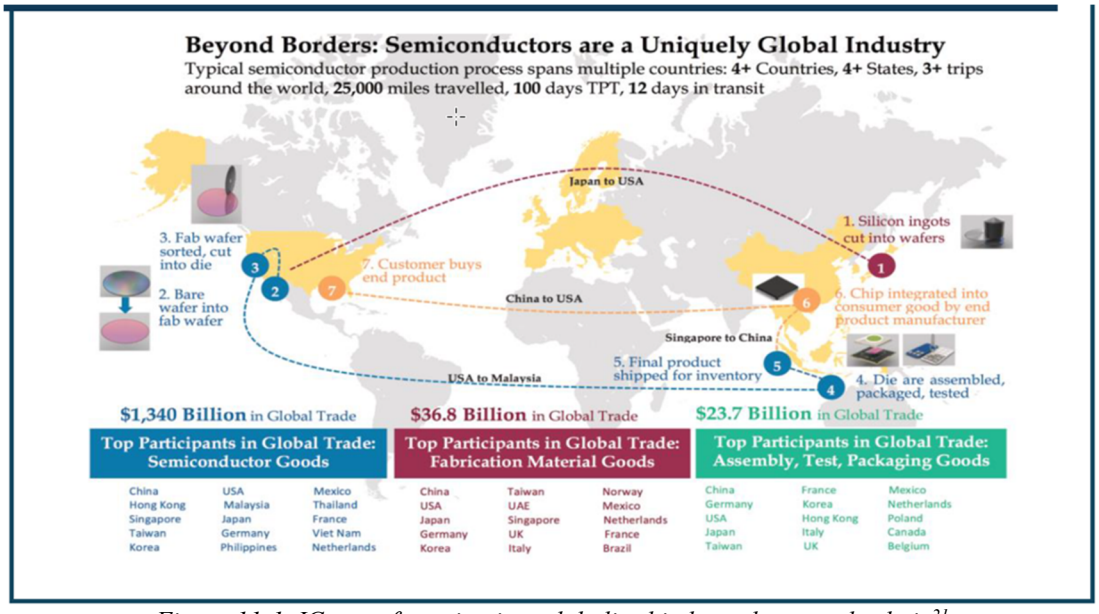


Figure 11-1. IC manufacturing in a globalized independent supply chain[21]

[20] http://www.ndia.org/-/media/sites/ndia/divisions/working-groups/tmjwg-documents/ndia-tm-jwg-team-1-white-paper-finalv3.ashx?la=en

[21] Found at http://www.businessdefense.gov/Portals/51/Documents/Resources/2016%20AIC%20RTC%2006-27-17%20-%20Public%20Release.pdf?ver=2017-06-30-144825-160

Access must also be reiterated here as a critical challenge and concern. While access to trusted components is already understood as a core concern, simple access to the parts needed from the larger global electronics industry base is an even larger concern. Figure 11-1 describes this concern, and emphasizes the need to take seriously the larger strategic issue of continued assured access to components for our current and future DoD systems.

This is a major concern as the globalization and consolidation of microelectronics companies is driven by demand in the commercial markets rather than by the needs within the Defense markets. Achieving continued assured access to advanced microelectronics components is imperative for the DoD to maintain the strongest Defense and Intelligence communities in the world. Without a coherent national strategy, the US government risks losing its ability to protect its key systems and the US microelectronics industry will lose its leadership role in this critical market. Figures 11-2 through 11-5 provide recent data on geographic distribution of semiconductor manufacturing leaders.

Table: Ranking of the Global Top 10 Foundries by Revenue, 1Q20 (Unit: Million USD)

Ranking	Company	1Q20E	1Q19	YoY	M/S
1	TSMC	10,200	7,096	43.7%	54.1%
2	Samsung	2,996	2,586	15.9%	15.9%
3	GlobalFoundries	1,452	1,256	15.6%	7.7%
4	UMC	1,397	1,057	32.2%	7.4%
5	SMIC	848	669	26.8%	4.5%
6	TowerJazz	300	310	-3.3%	1.6%
7	VIS	258	224	14.9%	1.4%
8	PSMC	251	178	41.2%	1.3%
9	Hua Hong	200	221	-9.4%	1.1%
10	DB HiTek	158	139	13.8%	0.8%
Top 10 Total		**18,060**	**13,737**	**31.5%**	**95.7%**

Notes:
1. Samsung's revenue includes revenues from its System LSI unit and its foundry business
2. GlobalFoundries' revenue includes revenue generated by the chip manufacturing unit that it acquired from IBM
3. PSMC's revenue includes its foundry revenue only
4. Hua Hong's revenue includes figures from its publicly disclosed revenue only

Source: TrendForce compiled this table with data from the respective foundries, Mar. 2020

Figure 11-2. Foundries are concentrated in Asia

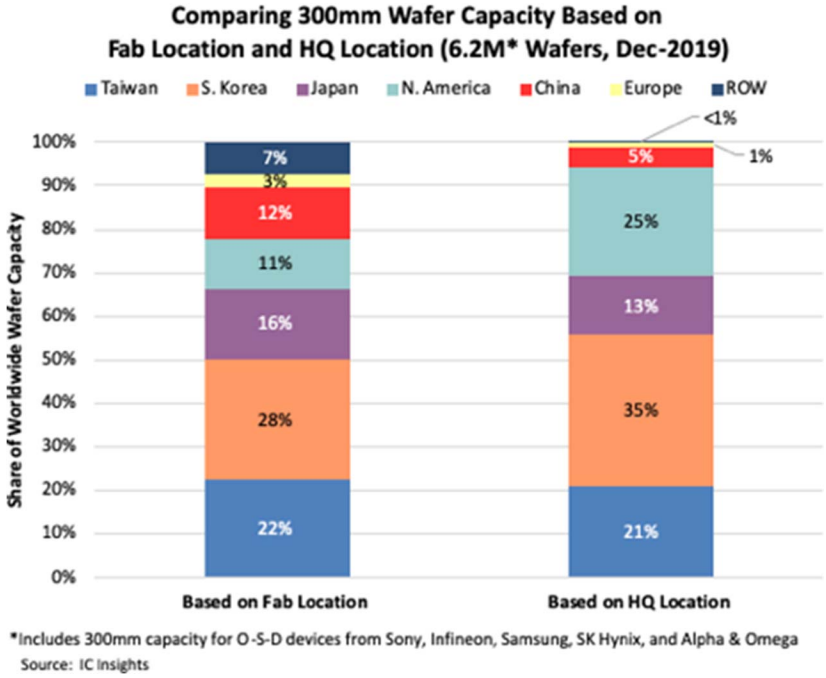


Figure 11-3. Although 25% of WW wafer capacity is owned by North American companies, only 11% of it is in North America.

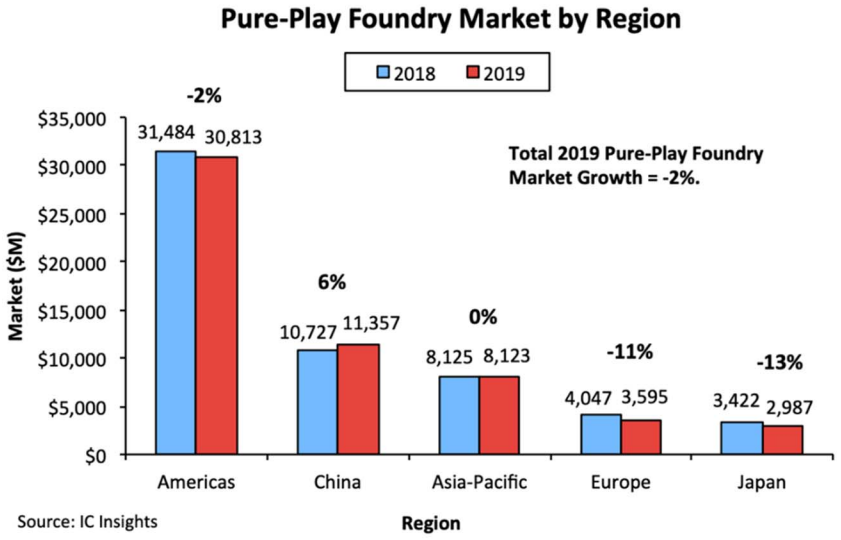


Figure 11-4. All foundry growth in 2019 was driven by customers in China

Table: 1Q20 Global Top 10 OSAT Companies' Revenue Ranking (Unit: Million USD)

Rank	Company	1Q19 Revenue	1Q20 Revenue	1Q20 Market Share	1Q20 Revenue Growth YoY
1	ASE	1,116	1,355	23.0%	21.4%
2	Amkor	895	1,153	19.5%	28.8%
3	JCET	600	818	13.8%	22.7%
4	SPIL	666	806	13.7%	34.4%
5	Powertech	469	624	10.6%	33.1%
6	TFME	253	310	5.3%	27.1%
7	TSHT	244	242	4.1%	-4.0%
8	KYEC	171	232	3.9%	35.9%
9	ChipMOS	145	185	3.1%	27.8%
10	Chipbond	152	177	3.0%	16.4%

Note 1: ASE's revenue includes its revenues from OSAT operations after subtracting for SPIL's

Note 2: Total market share in this table includes only the 10 listed companies

Source: TrendForce, May 2020

Figure 11-5. The top OSATs are concentrated in Asia (Amkor has US HQ but all production overseas)

12. Aerospace and Defense Roadmap, Rev. 0.1

Below is the first high-level roadmap table for HIR A&D. This is more qualitative than quantitative at this point, but we expect that to evolve somewhat as we drill down with more specifics. There will also be links to other HIR chapters with more details on certain topics, such as photonics, thermal management, and 3D interconnect. The A&D TWG will work on gathering inputs for the Rev 1.0 version that will appear in the 2021 update.

Area	Metric	SOTA 2020	2025	2030	2035	comment
Performance	Frequency	Higher freq., lower P				
	Power	Higher freq., lower P	Up through X-Band			
	Thermal					
Design	Tools	Point solutions				
	Interfaces	CHIPS AIB (early traction)	Broad adoption + roadmap			
	IP reuse	Chiplets (broad interest)	Business model adoption			
Integration	RF + digital	Separate solutions (e.g., SHIP)	RF + FPGA/GPU/CPU in production			
	3D	HBM, 3D layered NAND	True HI in 3D			
	Photonics	R&D (e.g. DARPA PIPES)				
Reliability	HI standards	DoD discussions	Power (GaN) & high V			
	Rework/redundancy	Custom solutions	Strategy based on standard analysis			
Supply Chain	Components	International ad hoc	"Zero trust" solutions			
	Assembly	US-only, lagging and/ or proprietary tech	On-shore HVM-like interposers, FOWLP	Flow for any volume, price, TAT		
	Security	Trusted facilities	"Zero trust" (data-based; *need metrics*)			
	Obsolescence	Lifetime buys				

Figure 12-1. Rev 0.1 of the HIR A&D high-level roadmap, to be fully updated in the 2021 edition

13. HIR Aerospace-Defense TWG Team

Name	Affiliation	Role
Tim Lee	Boeing	Co-chair
Jeff Demmin	Keysight Technologies	Co-chair
Tom Kazior	DARPA	Member
Dan Blass	Lockheed Martin	Member
Susan Trulli	Raytheon	Member
Kenji Miyake	Minimal Fab	Member

Edited by Paul Wesling