HETEROGENEOUS INTEGRATION ROADMAP

2020 Edition

Chapter 13: Co Design for Heterogeneous Integration

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Executive Summary

Semiconductor packaging traditionally provides the interconnection schemes between functional layers of systems and protection for dice from mechanical, thermal and electrical stress. Market focus on IoT, health, automotive and communication is driving the quest for more creative integration methods. With Moore's law scaling slowing down, complexity, size variability and the presence of uncertainty have rendered the design task more daunting. Multi-domain (chip, package, board) and multi-physics (thermal, optical, electrical, mechanical) challenges have given rise to the need for co-design tools and methodologies. Interdependence between different domains in the design flow dictates that analysis and design optimization in these domains must be performed concurrently. For heterogeneous integration, this implies the replacement of a segregated approach to synthesis with a parallel and integrated flow for design, analysis and optimization.

The emergence of new materials and devices with applications in computing, communication, and health care is expanding the stage for heterogeneous integration and creating new opportunities for co-design in which multi-physics, multi-scale and multi-level analyses will provide the needed solutions. New paradigms and new system architectures are being explored to better exploit these emerging technologies.

This chapter focuses on current state-of-the-art, challenges and potential solutions for Co-Design. It compliments and aligns with the chapter on Modeling and Simulation which details the needs for robust modeling and simulation tools in the context of heterogeneous integration. For example, electrical, thermal, and mechanical interactions across the chip-package-board domains can no longer be ignored. New modeling and simulation tools must accurately predict the physical (e.g. electro-thermal, thermo-mechanical, etc) coupling between multiple semiconductor components and the package/system that contains them. Although modeling tools are available for predicting electro-thermal phenomena at a component level (e.g. hotspots), there is currently no capability to predict these interactions within a co-design optimization environment where different design teams (chip – package – board) collaborate with design/model data that can be shared to support effective trade-off analysis and optimization for a whole system. In addition to this, thermo-mechanical interactions across the chip-package-board domains require robust and accurate modeling tools that can predict stress for use in new physics-of-failure based reliability models. Developments in physics-based models (multi-physics and multi-scale) and simulation tools will be complimented with new applications of AI and Machine Learning to address these challenges. The chapter on modeling and simulation provides further details on these modeling and simulation challenges and possible solutions.

Scope

This TWG explored challenges and potential solutions associated with:

- Chip-Package-Board Design Flow
- Pathfinding Solutions
- Architecture
- Silicon Photonics
- Neuromorphic Computing
- Quantum Computing

The chapter explores how co-design practices need to be defined in the context of heterogeneous integration. It addresses the traditional chip-package-board design flow as well as current capabilities and future challenges. The vision for co-design is expected to create an environment where design closure is achieved with a minimum number of iterations meeting all requirements for performance and cost. This environment must leverage from currently available technologies, namely computing power, algorithms and artificial intelligence.

System Co-Design

Traditionally, integrated circuit (IC) design is performed without consideration of the package and the board. Co-design addresses the discontinuity that exists between IC design and packaging. The objective is to streamline the process of assembling and optimizing the IC, package and printed circuit board (PCB) while applying constraints pertaining to the physical and logical interactions between these design domains.

User-friendly design flows require the creation of signal and power models for the IC, package and PCB which are then combined for system-level simulation. These steps help dictate guidelines with constraints that depend on products and applications.

Historically, packaging technologies evolved around two-dimensional methods. The need for heterogeneous integration has fostered interest in 3D stacking and packaging strategies [1]. These are facilitated by the inception of more advanced interconnection schemes such as TSV, micro-balls or direct Cu-Cu bonding and interposers. Flip chip BGAs operating in the gigahertz range with high densities of I/Os help achieve higher levels of integration while reducing the dependence on Moore's law. Interconnection schemes have also experienced dramatic changes with the demand for higher speed [5, 6]. They have evolved from passive channels made of impedance-controlled traces on top or embedded in a dielectric to complex structures that involve analog and mixed-signal components performing equalization and clock/data recovery. To achieve required performance, planning in all three domains of integration is of paramount importance.

Packaging tradeoffs must be identified and evaluated in advance in the system design. In addition, early planning is critical for a multi-domain design flow. Aligning to a good co-design space before layout and signoff is important. Floorplans become very demanding at early stages of the design flow and it becomes prohibitively difficult to conform them with board and package flows without expensive tradeoffs as the design progresses. Early floorplans along with early bump and ball maps can facilitate easy evaluations across metrics in all three domains.

In chip design, the package and board model is used as a load. In package design, the load is the chip-level I/O buffer model or the board model. Conversely, from the board, the loads are the package I/O buffer models. One option is to use the package as the "host" or "master" domain whose task is to operate as a middle-man between the IC and the PCB. As such the packaging gains influence on the choice of PCB technology and can play a role in optimizing floor-planning and bump placement on the IC die. Since some packaging technologies can be far more expensive than the integrated circuits that they house, their physical design must be cost-conscious so as not to allow the redesign of an interposer or substrate layout. Electrical budget decisions such as noise margins are decided prior to physical design and are monitored during package implementation. Auto-routers can help facilitate the task, but they need to closely cooperate with simulation tools.

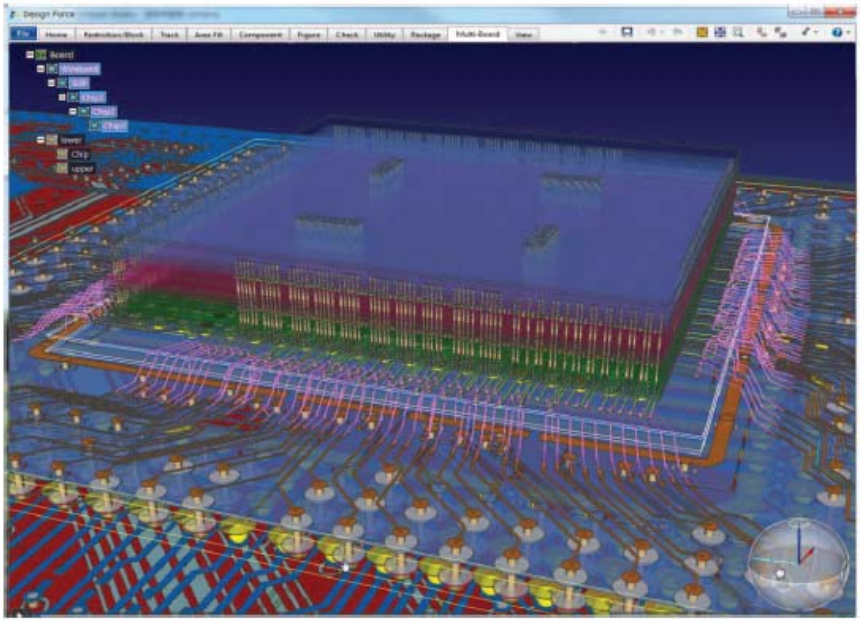

Figure 1. Domains in Co-Design Environment (Source [1]).

The ideal co-design expert system must possess the ability to simultaneously oversee the floorplan of the IC, the package, and the PCB while having the methodology for translating information between the domains and intelligently changing the design at any step within the design cycle. In addition, when bump pad pitches on the package are modified, visualization should permit capturing resulting changes on the underlying IC. Co-design optimization is achieved through floorplan visualization with the ability to track physical scaling and offset relationship between the various domains.

Traditional library components that manage connection pins and physical outline for boards and packages are too simplistic to operate in a co-design scenario. Because of the complexity and the level of layout detail that is required, the co-design vehicle should include details on trace routing, via location and internal active and passive components.

Co-design can ideally be used to optimize fanout from I/O buffers, minimize the number of PCB layers for signal traces, and optimize interposer layer count. For this to happen, the noise budgets for chips and packages must be made available. For instance, for low-voltage differential signaling, trace bumps must remain within close proximity and may need additional layers to prevent crosstalk. To facilitate power distribution analysis and I/O planning, co-design tools must offer the capability to extract interconnect parameters from the buffers to the package pins.

One critical issue is to manage the connectivity between the various levels. Intra-level and inter-level connectivity must be managed concurrently. The co-design approach must facilitate pin mapping, wire-bond placement and other logical connectivity constraints in a seamless manner. Electromagnetic compatibility concerns at the package and board levels create constraints on I/O routing, power distribution networks and even location of sensors, antennas and reactive elements. This information is to be used for accounting for obstructions, RDL routing and I/O placement. In a co-design environment this IC-level information must be shared with the package and board levels.

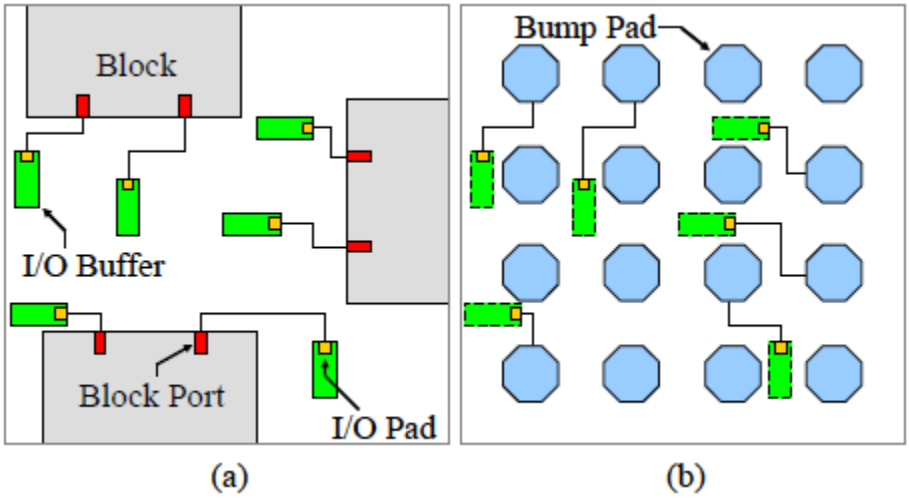

Figure 2. (a) Routing from block ports to I/O pads (b) Package level – routing from I/O pads to bump pads (source [2])

When changes are made in a domain, the information must be propagated to the other domains. Typical changes include net name changes, information about addition or deletion of signals, and scaling. Changes to the physical detail may include addition or deletion of pins, modification of pin pitch, or re-locations and re-orientations. In addition, accurate visualization of the hierarchy across all three domains can help achieve optimum connectivity and pin placement and the ability to manage cross-domain connectivity.

Database types and data formats used for package and boards are different from the IC level. To manage connectivity, traditional design flows rely on drawings and spreadsheets with labeling and names for the different domains. In particular, at the package level, spreadsheets and tables are the preferred database format because present-day CAD tools do not support the various flows that are in existence. At the board level, graphical schematics are more commonly used for connectivity management. With increasing design complexity, this method becomes intractable, making it difficult to track changes and capture co-dependencies that exist between the domains. In addition, cost-related constraints make it difficult to rely on spreadsheets and map models which are no-longer sufficient for a true co-design environment. For every co-design approach, concurrent database support is needed.

Placement and routing algorithms are at the heart of co-design strategy and have seen increasing challenges due to increasing complexity in integration. These algorithms have as their objective to determine the optimum layout while minimizing real estate and delay, improving signal integrity, and reducing cost. They also must possess computational efficiency. The increasing number of I/Os and added constraints result in the multi-domain and multi-physics nature of co-design. Balancing the goals of performance and routability while achieving optimal execution in placement is the nature of the challenge. More specifically, it is a bottleneck to concurrently optimize pin assignment and pin routing simultaneously in the different design domains (chip, package, board). At a premium are fast escape routing algorithms that handle bump assignment, RDL routing, and substrate routing with accuracy [4].

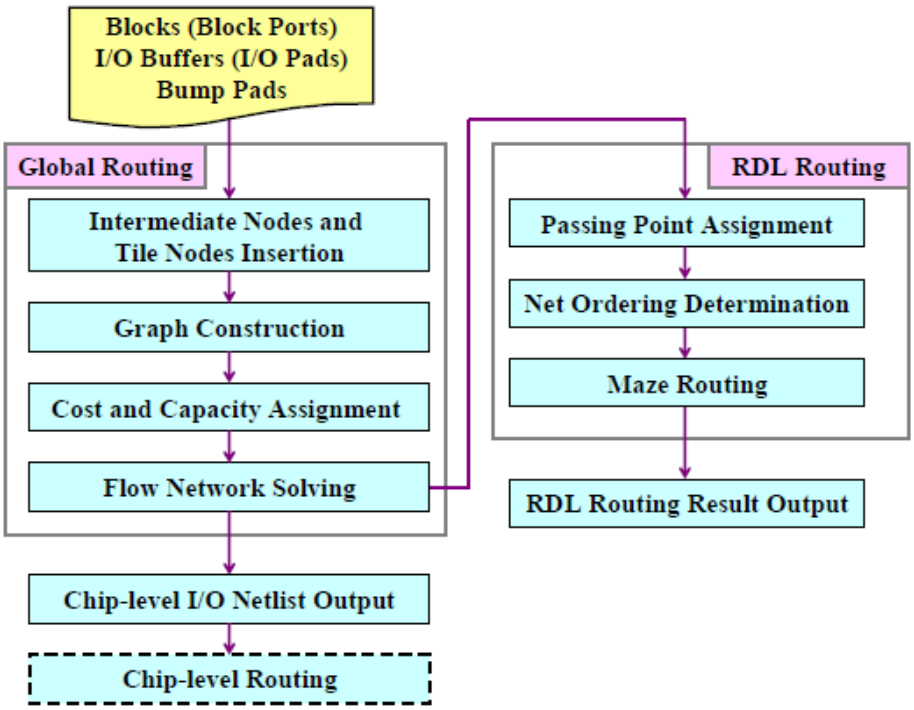

Figure 3. The Routing Flow of Chip-Package Co-design. (Source [3])

Verification is another component of a design flow that must be re-conceived for a co-design adaptation. One key step in the co-analysis of chip, package, and board systems is the reduction of complexity. At the verification stage, this is often achieved through macro-modeling and behavioral modeling. It is also necessary when the frequency dependence of interconnects must be taken into account. Macro-modeling is often used for circuit blocks for which the behavior is linear. PDN analysis often requires one to simulate systems for which equivalent circuits are not available [8]. From this, a macro-model can be generated to produce a SPICE (Simulated Program with Integrated Circuit Emphasis) stamp which reproduces the response of the system with sufficient accuracy. As an alternative, circuit netlists can be derived from macro-models for use with SPICE [10].

The complexity of integrated circuits makes transistor-level simulations intractable, resulting in a shift to behavioral modeling which not only provides a simpler and faster-to-simulate representation of the IC but also protects the intellectual property (IP). Models from the input/output buffer information specification (IBIS) aim to achieve that goal and are a standard in the electronics industry also known as ANSI/EIA-656A [7]. Other techniques involving behavioral models for nonlinear systems such as the poly-harmonic distortion (PHD) method are poised to provide viable solutions [11].

Given the complexity in current IC packaging technologies, choosing the appropriate package configuration for a product using cost, performance and reliability criteria can be a daunting task. Such a decision must be made at an early stage. Product definition in the early phases of implementation requires an expert system that can quickly predict and combine a complex assembly of components from a limited data set. Pathfinding often operates with incomplete and inaccurate inputs while providing viable solutions. It requires hundreds if not thousands of man-hours to develop a viable co-design solution.

While optimizing I/O across all the domains, simulation needs to be an integral part of the process. Pathfinding makes it possible to run some feasibility studies of different packaging options and to drive IC placement and routing with packaging constraints. This effort must bring electrical constraints and routability into packaging solutions.

It is not sufficient to transfer the design to the next team; additional collaboration is a more viable path to a successful product. In addition, useful tools can only be developed with interaction between developer and user. It is imperative that chip and package designers work together to assess early-on the system-wide impact of various packaging scenarios. Design teams need to bridge the process between pathfinding and production design. Experience has shown that tools must and will mature with customers. It is a very beneficial model, because software can be re-configured and updated continuously depending on the needs and specific applications. New methodologies need to be introduced and can only succeed with support from the major EDA players.

Not addressed in this survey is the need for true hierarchical schematics across the IC/Package/Board domain. This would entail compiling IC details required for co-design/co-optimization and representing them as one or two layers in order to integrate them with package and board level schematics. Also, not covered is the impact of higher performance (multiple voltages, higher signaling speeds, etc.), integration of multiple areas of analysis, scaling (bump pitch, BGA pitch, board level parameters, etc.) to co-design methods and tool flows. The impact of these trends on co-design requirements and the ensuing challenges will be reported in the next edition of the HIR roadmap.

Emerging Pathfinding Methodologies

In the conventional system design flow, where dice are designed and optimized individually and handed over to the package designer, pathfinding refers to finding the solution for package connectivity that results in optimal system interconnect performance. However, in the context of co-design for heterogeneous integration, pathfinding needs to ensure ICs, packages and PCBs are co-optimized, taking into account multiple physical domains and multiple system configurations [5].

State-of-the-art EDA tools (such as Siemens Graphics Xpedition Substrate Integrator [12] and Cadence OrbitIO Interconnect Designer [13]) have successfully tackled some of the key Pathfinding features required for enabling 3D Chip-Package-PCB Co-Design [5]:

- Unified workflow, including partitioning, floorplanning, design of system-level interconnects, route pathway exploration and feasibility analysis
- Capability to create abstract package models and virtual die models from multiple sources
- Ability to visualize and modify component placement scenarios and make connectivity changes in a preliminary floorplan
- Provision of dynamic manipulation of pin arrays within the abstract models
- Preserving signal assignments and rules while making adjustments to the physical pin array
- Support for multiple package variables and PCB form factors to verify and compare different system configurations
- Standardization of interface data of system blocks, usage of open-source file formats and APKs
- Enabling the interaction of design tools from different EDA vendors

Some of the difficult challenges for heterogeneous integration co-design include:

- **Routability estimation and optimal routing algorithms** are facing nets that may span across multiple die, with heterogeneous topologies. Academic efforts towards extraction of inter-die coupling [15] and power delivery pathfinding [16] have been proposed, but given the complexity of the problem, novel analytic and heuristic estimation algorithms will need to be integrated in the EDA tools. An up-to-date overview of open challenges in **multi-domain simulation and verification of 3D chip stacks** is given in Section 4.3 of [18].
- Using the conventional design flows, while each element of the system might be fully optimized, the overall system is unlikely to reach the same degree of optimization [17]. There is a clear need for **co-optimization of the global system**, using the co-design flow which allows parallel design of package and die, with adequate level of abstraction to support iterative modifications to subsystems, ideally performed in an automated manner (e.g. using machine learning [33] or other suitable algorithms).
- Co-design CAD tools need the **ability to quickly provide accurate models of physical structures and interconnects for electrical and thermal analysis**. Due to strong coupling of physical domains in 3D stacks, such modeling and simulation techniques need to be scalable, linking across different design levels. Recent academic work in the field [20] proposed transaction-level-based pathfinding, complementing previous RTL-based approaches, while commercially available EDA tools are leveraging standalone SI/PI, computational fluid dynamics thermal modeling and substrate fabrication checking tools [14].
- In particular, due to high density of tightly packed 3D systems, **the need for thermal pathfinding and co-optimization** needs to be addressed concurrently with electrical routing. Each component of a 3D heterogeneous system can be thermally optimized on its own (locally) to manage hot spots, junction temperature and power density. However, the integrated system (global) thermal management may be drastically different, due to stacking of high-performance chips in miniature packages resulting in increased heat flux, reduced cooling channel space and extreme conditions for hot spots in thin chips [24]. While transient simulation tools that take into account multiple thermal physics are becoming commercially available [113], there is still a need for unified co-optimization flow of the global system which takes into account thermal properties [25], [26], [32], which will be key to successful 3D integration of high-performance systems.

- With the increasing complexity of today's chips, packages and boards, designing each in isolation is no longer feasible. For enabling heterogeneous integration, there is a clear need for **true hierarchical schematics across the IC/Package/Board domain**. Available co-design EDA tools [27, 28] have enabled a single hierarchical schematic to drive both IC and package layout while providing LVS checking, along with automating the library development process. However, to enable efficient co-optimization, the IC details need to be abstracted and integrated with package and board level schematics [29, 30, 31].
- In order to support increasing performance and miniaturization, individual system building blocks are **growing in complexity** (multi-supply/multi-voltage techniques, higher signaling speeds and encoding techniques) and **reducing in scale** (bump pitch, BGA pitch, board level parameters). While current tool flows are equipped to tackle the problems for individual building blocks [34], [35], the tools will need to be tightly integrated into a coherent co-design methodology.
- Integration of heterogeneous devices into a 3D system necessitates **a multi-physics aware pathfinding environment** that considers the impact of material characteristics (e.g. CTE, Poisson ratio, Young's modulus, insertions loss). The environment needs to encompass electrical, mechanical, magnetic, optical, acoustic, and fluidic models of system building blocks, with the goal of enabling a holistic system-level architecture and interconnect optimization. While some systems lend themselves naturally to being packaged away into models with only electrical ports (e.g. MEMS processes), other integration cases (photonics, micro-fluidics) require non-electrical interfacing to the 3D system [18], making it difficult to capture in a pure EDA tool, and workarounds/customizations are needed to approximate it.
- **Design-for-Test and testability constraints for 3D integration** present a unique challenge to the pathfinding methodology, given the testing modality of individual system building blocks: IC bumps may have to be probed with power and routing topologies very different than in the final system. Pathfinding flow needs to enable IC/package bump layout that satisfies both sets of design constraints, similar to designing towards multiple PCB target systems in the conventional EDA flow [5]. In addition to the goal of enabling die testing that results in a high unit-to-die ratio, the interposer itself needs to be designed for testability, since it will be assembled to valuable known good die [18].
- Especially in very high complexity designs, **architectural considerations, such as redundancy, built-in self-test, (self) repair capabilities as well as failure monitoring functions** need to be considered during Pathfinding. They contribute to achieving acceptable yields and low failure rates. These measures result in cost-effective operation and long-term reliability. Co-design tools and algorithms need to support designing with redundancy and repair capabilities in mind, following the DfT design flows proposed for 3D memory chip design [22] and large-scale 3D integration [23].

System Architecture Consideration

VLSI design methodology flows by transferring specifications, constraints and details from one design layer to the next with virtually strict boundaries between the layers. In order to ensure design robustness, guard-bands are included when passing down the information, which inevitably causes over-design. With decreasing design margins, many designs can hardly afford such guard-bands under required bill-of-materials (BOM) cost and time-to-market constraints. Thus, it is highly desirable to explore methodologies that enable more flexible optimization. Architecture co-design is just such an approach that increases the optimization space across various design layers by removing the boundaries between layers.

Co-design for architecture involves preceding and back-end design layers. For the design layers at the top, it is more associated with system or software co-design, which includes:

- **Algorithm and architecture co-design** typically utilizes the hardware architecture feature to favor more efficient data access or processing. It is also possible to modify architecture details, such as deeper cache hierarchy, to improve runtime and efficiency of the algorithm.
- **Operating system (OS) and architecture co-design** provides more direct access to either OS services or the underlying cores, thereby creating a convenient programming environment at the cost of robustness.
- **Security and architecture co-design** can eliminate the inherent software vulnerabilities by optimizing the underlying architecture (as well as OS) to enforce software security policies and semantics.

On the other hand, the architecture can also be co-designed with the back-end details, which includes:

- **RTL and architecture co-design** typically combines or embeds the accurate RTL simulation into fast architecture simulation to provides more direct but accurate evaluations of the underlying core.

- **Interconnect and architecture co-design** accounts for the impact of interconnect parasitics, which is more evident at advanced nodes, but relies on a segment of interconnect layout to provide insight into the system performance at post-layout.
- **Device and architecture co-design** occurs more often for simpler architectures, such as SRAM. The unique characteristics of devices can then be directly reflected in the architecture design and functions as the motivation for architecture optimization.
- **Technology and architecture co-design** makes use of the underlying architecture features to determine the design rules and options for the technologies of interest.

However, it is not a trivial task to conduct architecture co-design. Several key limitations or challenges faced by architecture co-design will include:

- Improve co-simulation efficiency due to the fact that different design layers may employ tools with different complexities, causing speed differences in orders of magnitude. When all the design layers are connected and simulated altogether, a slower simulator for a layer may block the faster ones from completing.
- Provide communication mechanisms between different design layers. It is necessary to identify the minimum key information that needs to be interchanged to prevent unnecessary interruption.
- Support growing functionalities and heterogeneity requirements driven by the emerging devices.
- Support thermal, power integrity, and reliability management at advanced technology nodes.
- Support asynchronous accelerator or co-process design.
- Reduce time-to-market by co-design which demands details and constraints for thermal, electrical and mechanical parts.
- Drive down cost at the back-end stage to optimize design margins for layout.
- Provide models of available/proven system building blocks – at different levels of abstraction – to reduce system design time and risk of failure.

There have been industry-wide efforts in architecture design to include more functions, more materials, and highly energy-efficient co-processors [36]-[42]. Various innovations in architecture design for power and performance are highly desired to provide both the desired performance and power dissipation. The co-design methodologies account for information from other design layers to raise the potential optimization space. A trade-off between or among different layers is the goal of the architecture co-design.

Co-design in Silicon-photonics

The co-design of silicon-photonic systems involves multiple domains – electrical, optical, thermal and mechanical. The behavior of the system in these four domains needs to be carefully accounted for during the design process. The co-design process typically involves schematic capture, circuit simulation, circuit layout and design verification [43]. For schematic capture various commercial and non-commercial schematic editors exist. Both electrical and photonic components of the system can be composed hierarchically by breaking the components into sub-circuits. There are four approaches for simulating silicon-photonic systems:

- we can use a photonic circuit simulator to design photonics and electronics together;
- we can use an electronic circuit simulator to design photonics and electronics together;
- we can partition the design into its electronic and photonic components and simulate the components using separate electronic and photonic circuit simulators; and
- we can co-simulate electrical and photonic components using separate electronic and photonic circuit simulators [44].

Given the extensive design tools and design automation flows that are currently available for electronic systems, the second approach can enable us to simulate large silicon-photonic systems. For circuit layout, one can use a schematic-driven layout (SDL) approach. Depending on the hierarchy and sub-circuits in the silicon-photonic system, the SDL approach can pre-place individual components of the system, and then the designer can connect the components. However, connection of the photonic components is more challenging than the electrical components because photonic components do not follow the Manhattan-style routing rules and typically use a single routing layer. For verification, the design rule checker (DRC) and layout versus schematic (LVS) verification steps can be used for verifying both electrical and photonic components. Overall, a design environment that can accurately account for cross-domain effects is critical for designing optimal silicon-photonic systems.

The electrical and optical components have different timescales. Electrical components typically run sub-5 GHz. Optical components have a broader range and wavelength division multiplexed (WDM) optical signals can be spread

over a couple THz (even 10THz) of bandwidth. Thermal time constants are of the order of tens of microseconds. However, timescale for heating and cooling of electrical and photonic component are not always the same.

When co-designing silicon-photonic systems, we need to carefully account for the interaction between electrical, optical and thermal domains. For example, photonic circuits are very sensitive to thermal changes. So, electrical and photonic integrated circuits need to be designed and placed strategically such that heat generated due to power consumption in the electrical circuits does not impact the functionality of the photonic circuits. A ring modulator has optical power limitations, and dynamical self-heating due to both two-photon absorption (TPA) and linear absorption, and provides photocurrent because of defect absorption. This photocurrent can be used for feedback-based control of the silicon-photonic system.

Co-Design for Future Heterogenous Systems

System design and heterogeneous integration are key enablers for overcoming the challenges arising from the increasing complexity of embedded systems. In this section, we cover the design challenges for future heterogeneous systems based on neuromorphic and quantum computing.

Co-Design for Neuromorphic Computing

The architecture of digital microprocessors is fundamentally different from the biological brain. The brain consumes about 20 W and is a massively parallel structure of neurons interconnected through synapses, whereas microprocessors are mostly based on a von Neumann architecture. Inspired by biological functioning of the brain, neuromorphic architectures do not adopt von Neumann architecture by collocating memory close to the processor but structured to provide massive parallelism, high energy efficiency, reconfigurability, fault tolerance and integrability with CMOS technologies. Neuromorphic computing spans a broad range of scientific disciplines from materials science to devices, computer science to neuroscience, which are required to design an energy-efficient neuromorphic computing system.

Current CMOS-based devices and emerging devices (e.g., memristor, spintronics, magnetic, etc. [46-53]) are exploited to emulate the functionality of neurons and synapses. Just as biological neural systems are composed of networks of neurons and synapses that learn and evolve, so must the computational building blocks of neuromorphic computing systems learn and evolve to address the problems presented to them. Neuromorphic hardware platforms can emulate both the ultra-high density and the ultra-low power consumption of biological neural networks. Non-volatile memories (i.e. memristors) are one of the key enablers for biologically inspired computing [46].

Neuromorphic computing has been mainly explored based on neural networks. There are two main classes: (1) Artificial Neural Networks (ANNs) and (2) Spiking Neural Networks (SNNs) that are being developed in either digital or analog form and implemented typically in CMOS technology. Some of the notable hardware implementations have been listed in Table 1 [54].

Table 1. State of the art on neuromorphic hardware

Company/ Project	Technology	Energy Consumption	Learning and Autonomy	Integration density
IBM/ TrueNorth	Digital ASIC at 28nm CMOS	High, 26pJ per synaptic operation	No	1M neurons, 256M synapses
Intel/ Loihi	Image recognition, control of robots, etc.	Claims up to 1000 x higher efficiency than GPUs; 23.6pJ per synaptic operation	Yes	130k neurons, 130M synapses
Zhejiang & Hangzhou Dianzi Univ. (China) / Darwin	Digital ASIC at 180nm CMOS	Unknown, probably high	No	Max 32k neurons with 1000M synapses
Human Brain Project (EU)/ BrainScaleS	Mixed-signal wafer-scale ASIC at 180nm CMOS	Claims 1000 x higher efficiency than traditional chips	No	180k neurons, 40M synapses
Human Brain Project (EU)/ SpiNNaker	ARM boards at 130nm CMOS	High	No	1K neurons/core, 1M cores
DARPA & HRL Labs (US)/ SyNAPSE	Mixed-signal 180nm CMOS	17pJ synaptic operation	Yes	1024 neurons, 64k synapses

Co-Design Challenges

Neuromorphic design challenges arise from different domains (digital, analog, mixed-signal) to implement neuromorphic hardware. The interface between different domains introduces design challenges, and efforts are dedicated to increasing the accuracy of classification and computing with fewer bits and with lower precision. As a path to improve computing efficiency (and saving power), near-memory processing and computing (i.e., in-memory processing) are crucial. The design implementation challenges for neuromorphic computing are mainly related to SNR (signal to noise ratio), the variability of analog design, and mixed-signal design issues.

To build large-scale neuromorphic systems, there are several design-specific challenges. One challenge arises from the device type for emulating neurons and synapses such as chemical vs solid-state implementation. Using chemical-based devices will introduce design challenges and how these devices can be scalable, controllable and reconfigurable at the system-level. Another challenge arises for the cross-domain design needs (analog, digital, mixed-signal) which raises challenges on system level design, test and reliability. Moreover, a challenge arises from the need for a dense packaging of neurons to achieve comparable volume to biological brains. This might imply dense 3D technology packaging which challenges on package assembly, power delivery, heat removal, I/O count, and system-level design (place and route, interconnects, power/ground/clock signals). Here, we elaborate on these challenges in detail:

- **Cross-Layer Design (Material, Device, Circuits, Systems)** – Neuromorphic computing involves research competencies across layers from materials, devices, circuits, systems to packaging. Research is needed to bridge the gap between materials research, device design and system-level performance requirements. Current non-volatile memories (NVM) are limited from taking full potential of neuromorphic computing paradigm. Thus, challenges arise from cross-layer design to consider simultaneously behavior of novel devices and materials (i.e. switching properties of non-volatile devices) with system design to meet the requirements of neural networks (i.e. training and inference, symmetric up and down conductance changes in NVM devices, device-to-device variability, high bandwidth, noise sensitivity of analog elements, weight updates, area, power and scalability of design). In parallel to mainstream NVMs, new devices based on Electro-Chemical synaptic elements (ECRAM) [57] are also being investigated as novel devices for enabling AI neuromorphic computing.
- **Multiple Domain Co-Design (Analog, Digital, Mixed-Signal)** – At the core of neuromorphic computing, there are matrix manipulations done on arrays of non-volatile memories in the analog domain. These computations are performed locally in memory to avoid moving back and forth the weights from memory to the computing unit. However, not all the operations can be performed in the analog array; therefore, neuromorphic systems will need to embed the analog array into a digital backbone [58]. This will also raise challenges on the analog/digital interface such as insertion of ADCs and DACs, which might further raise concerns on noise, timing variations and power consumption issues. Thus, the focus will be given to exploring both mixed digital-analog and pure analog approaches. Moreover, NVM devices should have symmetric conductance variations, and investigation should be carried on utilizing novel-material NVMs such as phase-change materials (PCM). Additional design challenges arise from multi-physics simulations of neuromorphic devices to circuits (analog and digital), power/timing sign-off, power/signal/thermal integrity across domains, reliability (i.e. system-level connectivity and latency) and power delivery challenges.
- **Packaging** – Neuromorphic computing requires massive parallelism and significant data movement. One of the challenges arises in the system design and package integration. Cost-effective 3D solutions (3D stacking and monolithic integration) packaging technology should be explored to enable massive parallelism and increase in energy efficiency.

Co-Design for Quantum Computing

Quantum computing has become a very active and promising topic in recent years. Quantum computers hold the promise to solve certain sets of complex problems that are intractable for even the most powerful current supercomputers. Some of those problems are integer factorization, molecule simulation, search, and optimization that have application in fields as cryptography, chemistry, pharmacy, medicine, artificial intelligence and machine learning [57, 58].

The idea of building a quantum computer was introduced by the physicist Richard Feynman [59] in the early 80's. He proposed building a quantum machine to simulate quantum systems. Since then, many quantum algorithms have been developed, one of the most famous being the Shor's algorithm [60] for factoring large numbers that has

theoretically proven to have exponential speedup compared to its best classical counterpart. Another example is Grover's algorithm [61] to solve unstructured search problems with quadratic speedup. In addition, different quantum technologies are being implemented.

With the development of quantum algorithms and the advances in quantum hardware, main IT companies (Intel, Google, IBM, Alibaba) and research groups are working on building the first universal quantum computer. This requires contributions from several fields of knowledge, including Physics, Mathematics, Computer Science, and Electrical and Computer Engineering.

Background and overview

The basic unit of information in quantum computing is the quantum bit or qubit. A qubit can be in any of its basis states $|0\rangle$ or $|1\rangle$ but also in a superposition of both. This is mathematically described by $|\psi\rangle=\alpha|0\rangle+\beta|1\rangle$, where α and β are complex numbers and satisfy $|\alpha|^2+|\beta|^2=1$. When a qubit is measured, it only provides a binary value '0' or '1'(measurement result) with probability $|\alpha|^2+|\beta|^2$, respectively. In addition, the quantum state is projected onto the corresponding $|0\rangle$ or $|1\rangle$ state. Due to this probabilistic behavior of the measurement, quantum computation is non-deterministic and an algorithm needs to be run several times and averaged to get the correct result. By combining qubits and exploiting superposition and entanglement, quantum computers can be faster than classical computers. In order to perform quantum computation, the states of the qubits have to be changed. This can be done by applying quantum gates (or operations) when the circuit model of computation is adopted. An alternative approach is adiabatic quantum computing [62].

The main issue with qubits is their fragility. They easily decohere, that is, loose their information extremely fast just due to interaction with the environment. In addition, quantum gates are faulty, having error rates $\sim 10^{-2}$-10^{-3}. In order to make quantum computing fault-tolerant (FT), quantum error correction (QEC) and fault-tolerant mechanisms are required [63, 64]. To this purpose, a logical qubit is encoded into multiple unreliable physical qubits and FT operations are applied on them. In addition, the quantum system is continuously monitored to detect and correct for possible errors. The use of QEC significantly increases the number of qubits (up to four orders of magnitude) and imposes some extra requirements on the system design. One of the most promising QEC codes is surface code.

As will be explained in the next section, there are different ways of implementing qubits. Current quantum processors consist of tens of 'noisy' qubits. Although quantum processors have been able to demonstrate small quantum algorithms [65] and quantum error detection [66, 67, 68], quantum advantage and supremacy[1] still need to be proven.

The main challenges in quantum technologies are: i) improving qubit lifetime and gate fidelity and ii) scalability, to build large-scale FT quantum systems. We are now entering the Noisy Intermediate-Scale Quantum (NISQ) era [69] which refers to quantum processors with 50 to a few hundreds of qubits and with imperfect control over them.

Qubit implementations

There are different quantum technologies that are being developed which differ in their implementation and properties. The most relevant ones are superconducting qubits, ion traps, silicon-based qubits, topological qubits, and photonic qubits. The main properties and challenges for each of these technologies such as number of qubits, qubit lifetime, gate fidelity, gate time, connectivity and scalability are described in [70,71,72]. It is still unclear which technology will succeed, but nowadays superconducting and ion-trap qubits seem to be the most promising candidates as they have achieved the larger number of qubits. On the other hand, silicon quantum dots might be easier to scale up (smaller components), photons can be operated at room temperature, and topological qubits might have long lifetime and gate fidelities making it easier to achieve FT computation.

Current co-design challenges

As quantum computation is a relatively new field, there is no clear design process when building a quantum system. The first 'quantum computer' prototypes are [2]being developed and some of them are accessible through the Internet (quantum in the cloud) [73, 74]. The main challenges are related to building a scalable fault-tolerant quantum system and can be divided as:

- **Quantum hardware**: For building a large-scale quantum computer, quantum hardware must meet a set of requirements known as DiVincenzo criteria [75]. Although some of the qubit implementations such as ion-traps seem to already fulfil them, in general, lower error rates still need to be achieved by enhancing coherence time and gate fidelity. Most of the technologies are also facing scalability issues, that is, to

[1] Quantum advantage refers to the potential of quantum processors to solve problems faster than a classical computer. Quantum supremacy refers the moment when a quantum computer will solve problems that are unsolvable by classical computers.

integrate a larger number of qubits and quantum error correction mechanisms [76, 77]. Some solutions include using crossbars of qubits and even connecting small arrays of qubits using long-distance qubit couplers (silicon spin qubits) [78, 79]. Others propose to define unit cells that can be replicated and vertical I/O interconnects using through-silicon-vias or flip-chip bonding (superconducting qubits) [80] or build micro-fabricated traps and photonic interconnects or using modules (ion traps) [81, 82, 83].

- **Control electronics**: General purpose instruments, such as arbitrary waveform generators (AWGs) and digitizers, are used to operate and control the qubits, which would be unfeasible for large systems because of their size and cost. In addition, some quantum technologies such as solid-state qubits need to be kept at cryogenic temperatures, posing a connectivity challenge between the qubits and the control electronics that are at room temperature. Proposed solutions include multiplexing, to move classical control electronics closer to the quantum chip (cryogenic CMOS electronics) or even move qubits to higher temperatures (hot silicon quantum dot qubits) [79, 84, 85, 86, 87].
- **System design and integration (SW-HW co-design):** A computing system is composed of software (SW) and hardware (HW) layers. To bridge quantum applications with quantum devices, quantum SW as well as HW layers that serve as an interface between SW and quantum processors need to be developed. Software platforms have been built to connect to different quantum processors and/or quantum computer simulators [88]. However, as quantum technology still needs to mature and scale up, there are limited works that explore the entire system design [89, 90, 91, 92]. High-level quantum programming languages and compilers already exist to easily describe quantum algorithms and translate them into low-level quantum instructions, most of them expressed in a quantum assembly language (QASM) [88]. Furthermore, the first quantum instruction set architectures and corresponding microarchitecture have been proposed that target small quantum processors [93, 94, 95, 96]. The main challenge is to add 'programmability' to current quantum processors and exploring the design trade-off between hardware and software as the number of qubits grows. In addition, although the term quantum computer is extensively used, what we will have in the next coming years is a quantum co-processor or accelerator in which some parts of the computation will be offloaded (hybrid classical-quantum computing paradigm) [97, 98, 99, 100].

Electrical-Thermal Co-Design

3D/2.5D integration technology is seen as a major step forward towards achieving more than Moore's law performance in future electronic systems [101]. This technology provides the capability to continuously miniaturize integrated systems using advanced interconnect schemes such as through-silicon vias (TSVs), bump arrays and interposers that results in increased interconnect density and improved system performance. One of the key challenges seen in easy adoption of this technology is the significantly increased thermal budgets. This, in turn, adversely impacts the electrical performance of these vertically stacked systems.

With continuous scaling and higher interconnect and via density, significant increase in complexity of thermal management is seen, largely due to enhanced power density of 3D integrated systems. This results in chip temperature increase and higher voltage drop driven by thermal coupling. Some of the main thermal issues plaguing 3D/2.5D integration include:

- Joule heating,
- Electro/thermo migration, and
- Thermal stress.

These issues, in a significant way, degrade the overall electrical performance and reliability of 3D ICs and systems. Further, electrical resistivity being a temperature-dependent phenomenon results in localized Joule heating effects. These localized hotspots are becoming the main contributor to the temperature increase in packages. The variability in temperature and material features such as dielectric roughness and conductor surface roughness are essential aspects of the early design cycles and reliability assessment studies. Fig. 4 summarizes the typical causes for thermal effects.

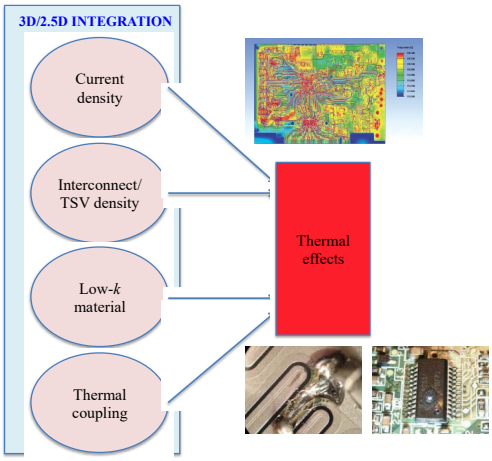

Figure 4. Typical causes for thermal effects in 3D/2.5D ICs and systems [2]

Greater understanding of thermal effects is quite important in handling overall system-level performance and reliability issues. Earlier approaches have been to separately attack these distinct yet interconnected design issues. However, the need is to perform electrical and thermal co-analysis that accurately predicts the performance of 3D ICs/systems/packages based on the interaction between electrical and thermal physics [101].

The typical electrical-thermal co-analysis flowchart for a Chip-Package-System is depicted in Fig. 5. Generally, the input for our analysis happens to be power-maps on chips. The temperature map from thermal analysis is used for material property adjustment in electrical design analysis. Power analysis results in normalized power maps that are the inputs for the next set of thermal analysis. Increased temperature on chips can result in significantly altered properties of the electrical materials as compared to that at room temperature. For example, we see more than 40% increase in electrical resistivity due to temperature increase. This severely affects the electrical design parameters in functional prediction and leakage power dissipation, which is the main source for elevated temperature. Thus, we can clearly see the electrical-thermal correlation from the perspective of overall system performance and reliability [102].

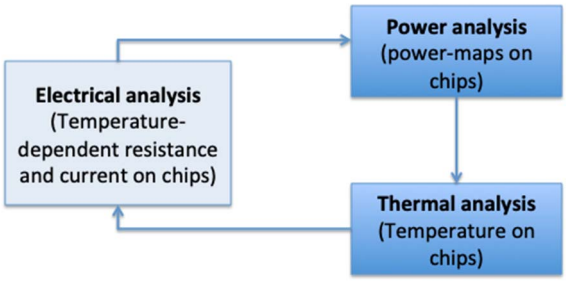

Figure 5. Typical IC/Package/System co-analysis flow [3]

We now present an executive summary of some of the analytical methods and simulation techniques for electrical-thermal co-design of a range of 3D/2.5D packages and systems.

- Simulation time can exponentially increase in a 3D chip/package architecture due to large-scale geometrical heterogeneity involving complex materials and structures including stacking of chips using TSVs, microbumps, interposer, package, and PCB. Volumetric meshing based on domain decomposition is an efficient approach that divides large complex structures into many subdomains, which are smaller and thus efficient in analyzing 3D systems/interposers/packages and PCBs by capturing the IR drop and thermal gradients across the system [104].
- On the other hand, the average power handling capability in coupled interconnects is a critical design metric that requires accurate calculation of frequency- and temperature-dependent variables. In high-power radio-frequency (RF) circuits, thermal effects on interconnect performance are major design constraints. The effect of geometrical and physical parameters, such as metal line thickness, electrical conductivity, and chip/system temperature, are quite critical [105].
- Thermal issues are quite important for TSVs and require deeper understanding of their equivalent circuit for an efficient electrical-thermal co-analysis framework, as shown in Fig. 6 [106].

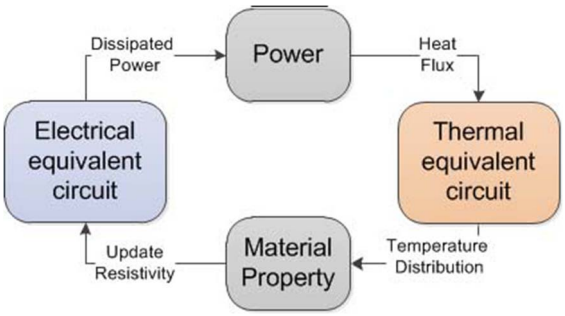

Figure 6. Generalized electrical-thermal co-analysis framework for TSVs

- For the PCB design ecosystem, the demand for speed is constantly increasing with every technology upgrade. While PCIe speeds have doubled every generation from 8 Gbps (@ Gen 3.0) to 16 Gbps (@ Gen 4.0) to 32 Gbps (@ Gen 5.0), the channel loss budgets have not doubled. This has, in-turn, reduced the margin of error in high-speed designs, thereby creating a lot of pressure to consider all possible impairments that would impact high-speed PCBs. Thermal effects are inseparable aspects of interconnects due to Joule heating and/or environmental heating and are directly linked to temperature-dependent material properties in PCBs. Table 2 shows the typical measured values of dielectric constant and loss tangent with respect to temperature [102, 108] for a mid-loss PCB material.
- Novel technologies including glass/polymer/flex packages are seen to suffer from thermal effects largely due to the lower thermal conductivity of the substrates. An array of metal-based package vias are normally inserted that act as thermal structures or heat sinks. However, this technique can severely degrade the electrical performance due to proximity effects and coupling [107].

Table 2. Material properties with respect to temperature [108]

Temperature ^oC	Dielectric constant D_k	Loss tangent D_f	Resistivity $\Omega - m$
20	4.23	0.0124	1.72E-08
60	4.26	0.0146	2.00E-08
100	4.3	0.0173	2.27E-08

To summarize the above points, electrical-thermal co-design can be seen as a systematic approach towards achieving improved electrical performance in 3D/2.5D systems (on-chip, chip-to-chip, PCBs, interposers, etc.) while also enhancing their reliability and minimizing the overall system-level power and thermal budgets.

Co-Design and Analysis of Chiplets, Interposers and Packages for Multi-Die Systems

Competition in the process technology race will continue for the next decade. However, this will not be the only factor for competitiveness. Cost and bandwidth have been the driving forces for the computer industry over the past 60 years. These relied on the assumption that advances in technological manufacturing would lead to advances in integration. While scaling occurred for many component parameters, it did not occur uniformly. Irregular scaling is exemplified by analog circuits for which certain components scale with the wavelength rather than technology node. Thus, the difficulty of interfacing digital and analog components has become more serious in the lower nodes. At this point additional scaling does not necessarily result to a proportional increase in performance on a per-node basis.

Chiplets offer manufacturers a more efficient means of achieving die scaling on those portions of the chip that would yield more substantial gain in performance. With such an approach, an entire IC does not need to shrink. In addition, smaller die lead to less wafer waste, higher number of cores per wafer, improved yield and facilitated testing. Finally, chiplets can facilitate heterogeneous integration by combining different types of technology (e.g. silicon and gallium arsenide).

In addition, scaling has become more difficult and expensive at each node, and the power and performance improvements to be gained have diminished. While scaling alone can improve performance for each new node below 7nm, changes related to advanced packaging, heterogeneous integration and hardware-software co-design can boost performance by several orders of magnitude.

Co-Design of Chiplets

In current 2.5D chiplet systems, each chiplet is often designed independently as a single unit and then the chiplets are mounted on an interposer or a package to form a heterogenous system. There is very little co-optimization of

chip-interposer-package design. This design approach is not optimal when the interactions between chips, interposer and package are critical to the overall system performance, power, chip-to-chip communications and reliability as well as cost. The RDL routing, interposer design and package layout need to be implemented with constraints to improve the overall system.

The design flow that considers the Chip-Package Co-Design goals in 2.5D integration technology is shown in Figure 7. In this flow, the design of the 2.5D package together with the chiplets is implemented in the same design environment. This enables exchanging design information between the chiplets and the package during the optimization steps, which is essential to achieve an optimized heterogenous system [109]. It starts with a partitioning scheme that is compatible with the 2.5D package routing layers in a chip design process. Then the floor planning of chip and package routing is analyzed to reach an optimized heterogenous system.

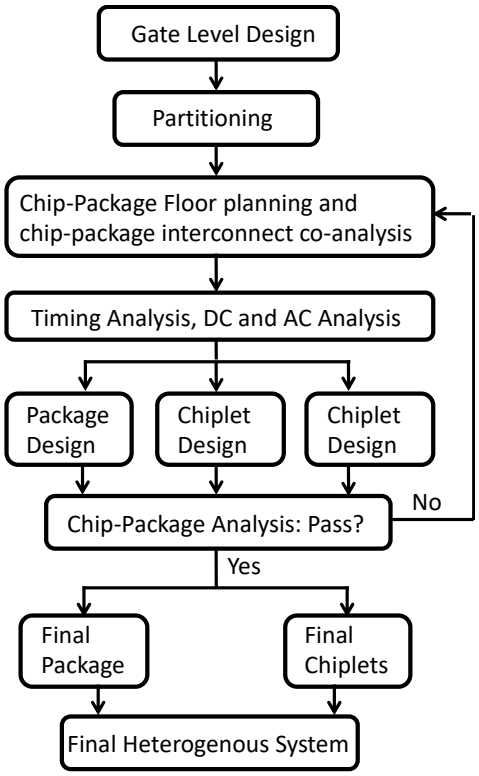

Figure 7. Chiplet-package co-design flow.

The common implementations of heterogonous integration systems using organic substrates or silicon substrates with and without TSVs are reviewed. The performance, density and cost of the die-to-die interconnects using these four approaches can be significantly different. A conceptual drawing of the cross-section of a heterogeneous system with organic or silicon interposer, chip-on-wafer-on-substrate (CoWoS), and Embedded Interconnect Bridges (EMIBs) are shown in Figure 8. Most common implementations of 3D system-in-package (SiP) are designed and manufactured with a large organic interposer (substrate) with fine-pitch and fine-line interconnections [110]. Silicon interposer and EMIB are also used for high-end and high-performance systems [111]-[112]. Figure 9 summarizes different characteristics of EMIB and silicon interposers with respect to organic substrates. Due to the higher interconnect density, silicon interposer and EMIB are more effective in high-end heterogeneous systems.

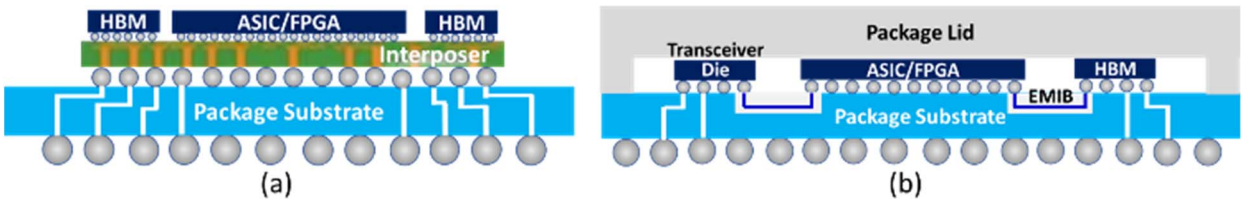

Figure 8. Heterogenous integration using (a) organic or silicon interposer and (b) EMIB technology.

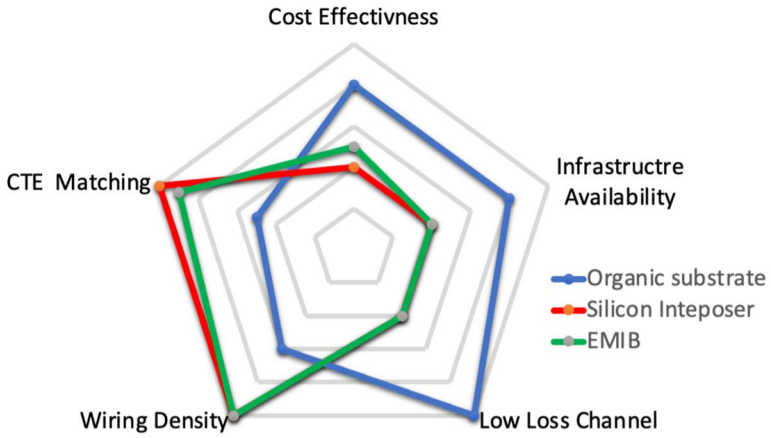

Figure 9. Comparison EMIB and silicon interposers with respect to organic substrates.

Although the scale of interconnect dimensions achievable in silicon interposer is finer than what is realizable in organic packages, the signal conductor and dielectric losses in organic substrate are significantly less than in silicon interconnect. The dimension of interconnects used in silicon interposer or EMIB is similar to that of silicon metallization, thus the resistive loss and crosstalk between signal routings can be one of the dominant sources of noise and timing error when compared to package and board. While traces in package and board may require only 2D-based crosstalk analysis, an interposer and silicon bridge need 3D crosstalk analysis including vertical paths such as via, bump and micro-via.

As shown in Figure 10, a typical silicon interposer often uses one-sided 3 or 4 layers of redistribution layer (RDL) and through-silicon via (TSV). The physical dimensions and material properties shown in Figure 10(a) and Table 3 are used in the analysis. The metal configuration of the three copper conductor layers with signal layer and power mesh are also shown in Figure 10(b). The diameter of the TSV is 10 um and the insulation layer thickness is 0.5 um.

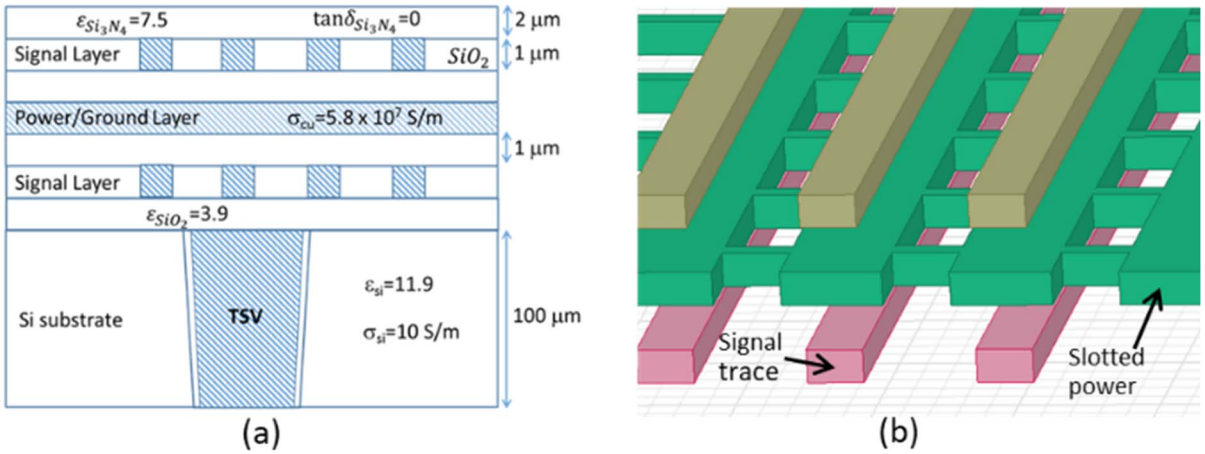

Figure 10: (a) A typical physical dimension and materials properties and (b) the signal and power/ground interposer design.

The fine pitch offered by silicon interposer and EMIB allows high density routing among multiple processors, transceivers and HBM dies. Although the channels between the dies on the same package are relatively short, the transceiver dies can communicate with another processor placed on another organic package using TSV or micro-via, package, board traces and vias; thus, signal integrity can be a concern. The effect of TSV or interposer via with optimized design, using single or multiple TSVs, in off-chip high-speed channels can be negligible.

Unlike the silicon interposer, the silicon bridge (i.e., EMIB) does not require TSVs. The EMIB is embedded in the package and uses micro-bumps to connect signals as well as power/ground planes between two silicon dies, as shown in Figure 10(b).

Signal Integrity Analysis of Chiplets

Since hundreds of signal interconnects are densely integrated in a small space in either the organic or silicon interposer, there exist several coupling mechanisms. Since all signal micro-bumps are very crowded in a limited space, and only a limited number of ground signals often provide the reference, it is necessary to analyze the coupling

effect between power and signal nets. Power-to-signal coupling can be a major source of noise and jitter in both interposer and EMIB.

The signal integrity of the three types of second-level interconnects – organic and silicon interposers and EMIBs – are analyzed using the dimensions and materials properties summarized in Table 3. All implementations have two signals surrounded by power and ground traces. The insertion loss of the three implementations are shown in Figure 11 (a). The attenuation of the silicon interposer is higher due to the aggressive design rules shown in Table 3. The DC loss is higher due to the smaller cross section of the silicon interposer traces. As shown in Figure 11 (b), the crosstalk for the silicon interposer is minimized by using ground and power traces for shielding, even though the ground and power planes are hatched.

Table 3. Cross-section and materials properties of the three channels

Interposer Type	*H (um)*	*T (um)*	*W (um)*	*S (um)*	ε_r	*tan (δ)*
Organic	10	10	7	7	4.6	0.02
EMIB	2	1	2	2	3.9	0.001
Silicon	1	1	1	1	3.9	0.001

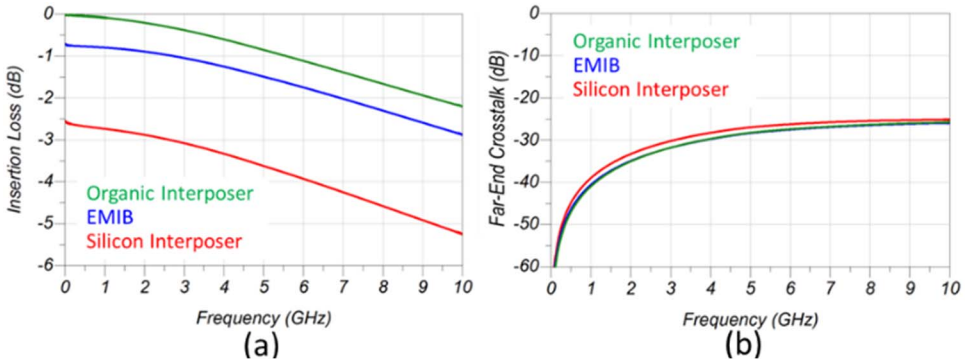

Figure 11. Channel characteristics of the organic, silicon interposer and EMIB: (a) insertion loss and (b) far-end crosstalk.

Power Integrity Analysis

The power distribution network (PDN) of the heterogeneous integrated system includes the interposer or EMIB power and ground routings connected to the PDN of the rest of the system that consists of PCB, package and micro-bump routing, as shown in Figure 12. If a PDN connection exists in the interposer or silicon bridge, then the PDN impedance or resonance of the dies with smaller on-chip decoupling capacitors can be significantly improved through charge-sharing from those dies with large decoupling capacitors. Since the EMIB technology does not use TSVs, power connections among multiple dies are made through package-surface or horizontal-silicon routing; thus, the power delivery networks of IPs must be planned early in the design phase. For example, if there are power network connections between die 1 and die 2 through the interposer and/or package routings, and the power supplies are shared, die 1 can take advantage of available capacitance provided by die 2. A typical example of capacitor- or charge-sharing often occurs in a multi-die system with HBM devices. Therefore, without the interposer or EMIB connection, the PDN in die 1 may have a very high peak exceeding 1.0 Ohm while the die 2 PDN peaks at only 0.1 Ohm. Such shared PDN impedances for digital and analog supplies are shown in Figure 13. Therefore, the power network connections between multiple dies through interposer or EMIB routings allow sharing of decoupling capacitors to lower self-generated noise. However, the proper tradeoff has to be made as the noise coupling may increase among the charge-sharing silicon dies leading into elevated coupled power supply noise.

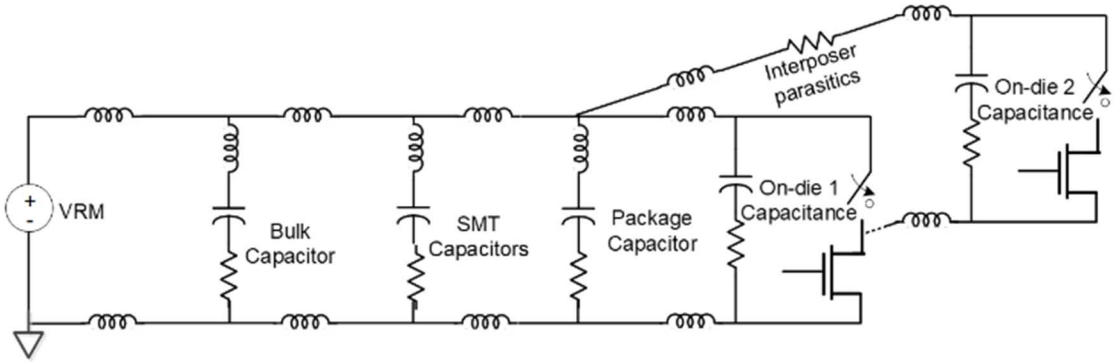

Figure 12. PDN model for a heterogeneous integrated system including board, package, interposer, and parasitic and die decoupling capacitance.

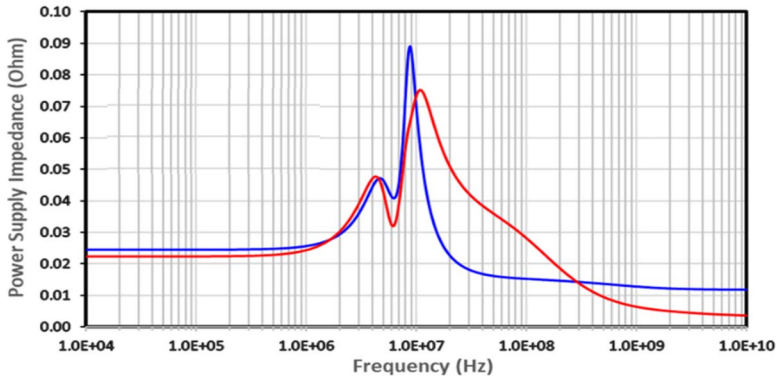

Figure 13. Typical PDN profiles of two supplies.

Analysis of Chiplet Interface

A Die-to-die interface, shown in Figure 14, is very different from traditional memory interfaces or SerDes (Serializer/Deserializer) links in many respects. The massive I/O often present in die-to-die interconnects is not impedance controlled and designed to efficiently operate strongly coupled to the channel. The interface operates power efficiently in the few-Gbps data range. The I/O often use HSUL (high swing unterminated logic) where the transmitter is not designed to be linear. Some I/Os use LVSTL (low-voltage swing termination logic) to save power with reduced swing.

Although the operating data rates of die-to-die I/O are often lower compared to the latest modern links, there are unique challenges to optimizing the performance. Often, the I/O can be partitioned into analog and digital sections where only the jitter of the digital section is calculated and the voltage noise and timing jitter for the analog section of the link is analyzed. The jitter and noise in the analog section is summarized in Table 4.

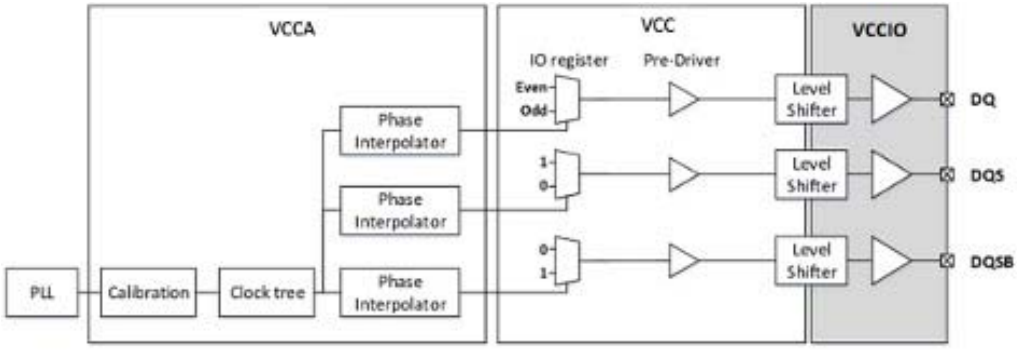

Figure 14. Block diagram and power supply partition of a typical I/O PHY TX for source-synchronous parallel

Table 4. Timing and noise contributions of the analog link

Channel Jitter/Noise Sources	Contribution
ISI Jitter [UI]	0.07 – 0.10
ISI+ Crosstalk Jitter [UI]	0.12 – 0.19
ISI + Crosstalk + SSN jitter[UI]	0.19 – 0.25
Power Supply Noise [mV]	60 – 85

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