HETEROGENEOUS INTEGRATION ROADMAP

**2020 Edition**

# Chapter 22: Interconnects for 2D and 3D Architectures

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# Chapter 22: Interconnects for 2D and 3D Architectures

**Executive Summary**

With increasing interest in on-package Heterogeneous Integration (HI), there is a need to describe package architectures and their interconnect capabilities in a simple and consistent manner. This chapter has two primary objectives: to (a) define and proliferate a new standardized nomenclature for package architectures covering and clearly demarcating both 2D and 3D[1] constructions and to (b) define and proliferate key metrics driving the evolution of the physical interconnects in these architectures.

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## 1. Introduction

Moore's Law Scaling has paced growth of the microelectronics industry for the last 50 years by providing a template for silicon scaling and homogeneous SoC (System on Chip) integration of different IP. Moving forward, HI, enabled by changes in the physical features, and electrical and thermal attributes of packages and microsystems is expected to increasingly complement Moore's Law scaling and continue to provide improved functionality. Current and new package architectures will continue to be major enablers to sustain and enhance growth in the microelectronics industry. These architectures enable novel heterogeneous SiP (**S**ystem **i**n **P**ackage) configurations and represent key innovations for cost-performance optimized microelectronics systems [1-8]. Historically, the primary purpose of the package was to provide mechanical protection for the die, and space transformation for silicon features. Innovations in packaging have focused on minimizing impact to silicon size scaling, power, performance and latency while maximizing performance opportunities made possible by Moore's Law. In addition, the semiconductor packaging industry has also produced MCPs (**M**ulti-**C**hip **P**ackages) for a few decades, primarily for improved time-to-market and for critical HI needs (e.g. DRAM integration). Industry trends today show an increasing need for HI driven by a need to add diverse functionality (often realized with different IP on silicon nodes from multiple different suppliers) [9], improved silicon yield resiliency and the continued need for rapid time to market. 2D and 3D package architectures are ideal heterogeneous integration platforms because they provide short, power efficient, high-bandwidth connections between components in compact form factors.

Heterogeneous packaging technologies:

- Deliver power-efficient, high-bandwidth on-package IO links using different communication protocols;
- Enable a diversity of off-package IO protocols;
- Deliver noise isolation for single ended and differential signals;
- Manage increasing cooling demands;
- Support complex power delivery architectures;
- Meet diverse application functionality, form factor and weight constraints ranging from high-performance servers to flexible, wearable electronics;
- Meet a broad spectrum of reliability requirements for different market segments and applications;
- Provide cost effective, high precision and quick turn assembly.

Developing products using advanced packaging requires an integrated approach involving collaboration with product architects, system architects, process engineers, materials engineers, and reliability engineers, and a detailed understanding of the fundamental thermal, mechanical and electrical characteristics of the various architectures.

## 2. Scope

This roadmap chapter has a two-fold purpose:

- Define and proliferate a new standardized nomenclature for package architectures covering, and clearly demarcating, both 2D and 3D constructions. Currently there are a number of intermediate definitions between 2D and 3D constructions, referred to as 2.xD architectures. Experts in this road-mapping effort, representing a wide spectrum of industry, academia and consultants, agree that the current nomenclature (e.g. 2.1D, 2.3D, 2.5D architectures) does not have a common rational basis and that there is a need to provide a comprehensive classification framework based on a common set of assumptions. The objective of this chapter is to drive clarity and provide a nomenclature framework that will house different architectures.

[1] Scope of this chapter is restricted to electrical interconnects between one or more semiconductor devices.

- Define and proliferate key metrics driving the evolution of the physical interconnects in these architectures. This chapter will list their current values (based on the state of the art) and projections for the next generations.

The chapter is organized into 4 primary areas:

- Converged Nomenclature Framework for 2D and 3D Architectures
- Key Metrics:[2]
  - Design Attributes
  - Electrical Attributes including Signal Integrity and Power Delivery
- Difficult Challenges
- Discussion

## 3. Converged Nomenclature Framework for 2D & 3D Architectures

a. A 2D architecture is defined as an architecture where two or more active silicon devices are placed side-by-side on a package and are interconnected on the package. If the interconnect is "enhanced", i.e., has higher interconnect density than mainstream organic packages, and is accomplished using an organic medium, the architecture is further sub-categorized as a 2DO (2D Organic) architecture and similarly, if the enhanced architecture uses an inorganic medium (e.g. a silicon/glass/ceramic interposer or bridge) the architecture is further sub-categorized as a 2DS architecture. Architectures that include enhancements over and above traditional 2D architectures (typically 2 or more die flip-chip attached on a traditional organic package) are variously referred to as 2.x architectures to emphasize their specialness. These nomenclatures do not have any particular technical basis. It is proposed here that they all be broadly categorized as 2D enhanced architectures.

b. A 3D architecture is defined as an architecture where two or more active silicon devices are stacked and interconnected **without** the agency of the package.

The ideas described by this nomenclature[3] are schematically shown in Figure 1.

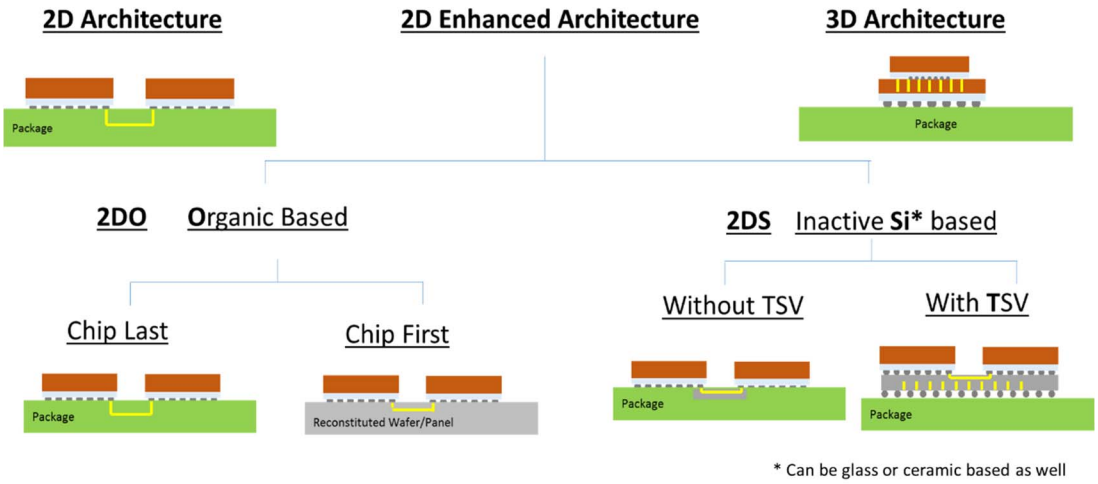


*Figure 1: Schematic describing the Converged Nomenclature Framework for 2D & 3D Architectures.*

## 4. Interconnect Nomenclature

Package interconnects can be classified as:

(a) **Die-Die Interconnects:** Interconnects between stacked die for vertical connectivity between multiple die in a 3D stack. These may be further sub-categorized using the process these interconnects are created with, which can lead to different physical attributes, such as Die-Die interconnects created using a:

a. Wafer-to-Wafer attach process
b. Die-to-Wafer attach process
c. Die-to-Die attach process

The roadmap for these interconnects is described in Section 5.1.1.

[2] Other key attributes such as thermal and process attributes are covered in different chapters in this Roadmap

[3] Figure 1 only describes a nomenclature, and technology equivalence is not intended or implied.

(b) **On-package Die-to-Die Interconnects:** i.e. 2D and Enhanced-2D Interconnects: Interconnects between die (and/or die stacks/pre-packaged die) within the package for lateral connectivity. The roadmap for these interconnects is described in Section 5.1.1.

(c) **Die-to-Package Interconnects:** Interconnects between the die and the package (Figure 2), typically known as the first level interconnect (FLI).

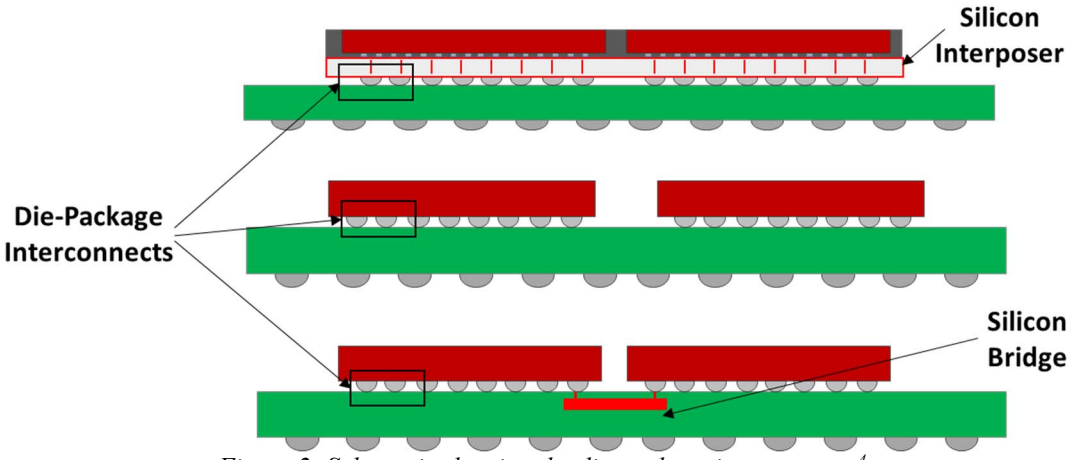


*Figure 2: Schematic showing the die-package interconnects*[4]

The schematic in Figure 2 only shows area-array interconnects. Wire-bond interconnects are also an important die-to-package interconnect. Three types of wire bonding technologies, Au, Cu and Ag wire-based technologies, are widely used today. The finest in-line wire-bond pitch currently seen in high volume manufacturing (HVM) remains at 40 µm inline pitch and has been that way for the last few years. Wire-bonders are capable of supporting a minimum inline pitch of 35 µm or 40 µm staggered (dual row) pitch in HVM (Au, Cu, or Ag wire). Process advances in recent years have brought Cu wire bonding capabilities just about on par with Au wire bonding capabilities. Additionally, current bonders have successfully demonstrated 30 µm inline pitch capability to provide an envelope covering potential near term demand. Table 1 shows the best-judged 5-year roadmap from leading wire-bond experts. For additional details on the wire-bonding technology, including discussions on multi-tier stacking that allows for considerable innovations on heterogeneous integration, the reader is referred to the chapter on Single Chip and Multi-Chip Integration (chapter 8) in this roadmap [10].

Another key metric is the flip-chip pitch for area array interconnects. Table 1 shows a 5-year roadmap for the traditional flip-chip pitch. Given that the pace of change is flat, it is reasonable to assume that the flip-chip pitch will stay at a minimum bound of 90 µm. This pitch does not cover the fine pitch scaling available in enhanced 2D and 3D architectures.

| Year of Production | 2018 | 2019 | 2020 | 2021 | 2022 | 2023 | 2024 |
|---|---|---|---|---|---|---|---|
| Au Wire bond – single in-line (µm) | 40 | 35 | 35 | 33 | 30 | 30 | 30 |
| Cu wire – single in-line (µm) | 40 | 35 | 35 | 33 | 30 | 30 | 30 |
| Flip chip array, low end & consumer (µm) | 150 | 150 | 130 | 130 | 130 | 130 | 130 |
| Flip chip – cost performance (µm) | 110 | 110 | 110 | 100 | 100 | 100 | 90 |
| Flip chip – high performance (µm) | 110 | 100 | 100 | 90 | 90 | 90 | 90 |

*Table 1: Die-Package Interconnect Pitch Roadmap*

(d) **Within-Package Interconnects:** Interconnects within the package that enable lateral connections between two or more die. Roadmap projections of within-package interconnects are not discussed in this chapter. The reader is referred to the chapter on package substrate technologies (chapter 8).

(e) **Package-to-Board Interconnects:** Interconnects between the package and the next level, which is typically the motherboard, are referred to as the second level interconnect (SLI). SLI connections are either socketed or ball grid array (BGA) and may be combined with on-package cabling[5]. The 2015 ITRS roadmap projections for socket pin

[4] Note that the values discussed in this section do not include the case where the organic substrate is scaled to accept fine pitch die stacks such as HBM @ 55µm, with and without EMIB. Since instances such as these are more relevant to die-die interconnects, they are discussed in Section 5.1.1.

[5] This chapter does not address on-package cabling solutions or provide a roadmap since this class of solutions is still maturing.

counts are reproduced below [11] in Table 2a[6]. Figure 3 shows a trend graph based on how sockets have actually evolved (see [12] for a technology validation data point). This exponential pin-count growth is expected for the near term, as shown in Figure 3. However, the effect of heterogeneous integration on the pin-count growth is yet to be comprehended for the long term. The 2015 ITRS projections are reasonable extrapolations for the cost-performance segment (minor changes are shown in Table 2b). For the high-performance segments, the projections look reasonable until ~2021 but seem to be under-projecting significantly after that. This is likely because the pin-count increase trend in the 2015 projections was assumed to be linear. Table 2b shows an updated projection for the high-performance segment using a combination of exponential and polynomial fits.

| | *2019* | *2020* | *2021* | *2022* | *2023* | *2024* | *2025* | *2026* | *2027* | *2028* | *2029* | *2030* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Low-end, Low-cost package | 550 | 550 | 550 | 600 | 600 | 600 | 600 | 600 | 650 | 650 | 650 | 650 |
| Memory (MCP) | 260 | 280 | 280 | 280 | 280 | 280 | 280 | 280 | 280 | 280 | 280 | 280 |
| Cost-performance | 3200 | 3300 | 3400 | 3500 | 3600 | 3700 | 3800 | 3900 | 4000 | 4100 | 4200 | 4300 |
| Harsh | 693 | 728 | 764 | 803 | 843 | 860 | 877 | 894 | 911 | 928 | 945 | 962 |
| High performance | 5394 | 5651 | 5934 | 6231 | 6543 | 6855 | 7167 | 7479 | 7791 | 8103 | 8415 | 8727 |

*Table 2a: Socket pin count projections from 2015 ITRS [11]*

| | 2019 | 2020 | 2021 | 2022 | 2025 | 2028 | 2031 | 2034 |
|---|---|---|---|---|---|---|---|---|
| Cost performance | 3200 | 3300 | 3400 | 3500 | 3800 | 4100 | 4400 | 4700 |
| High performance | 5125 | 5694 | 6302 | 6946 | 9105 | 11601 | 14434 | 17604 |

*Table 2b: Updated projections for socket pin count in the Cost-Performance and High-Performance segments*

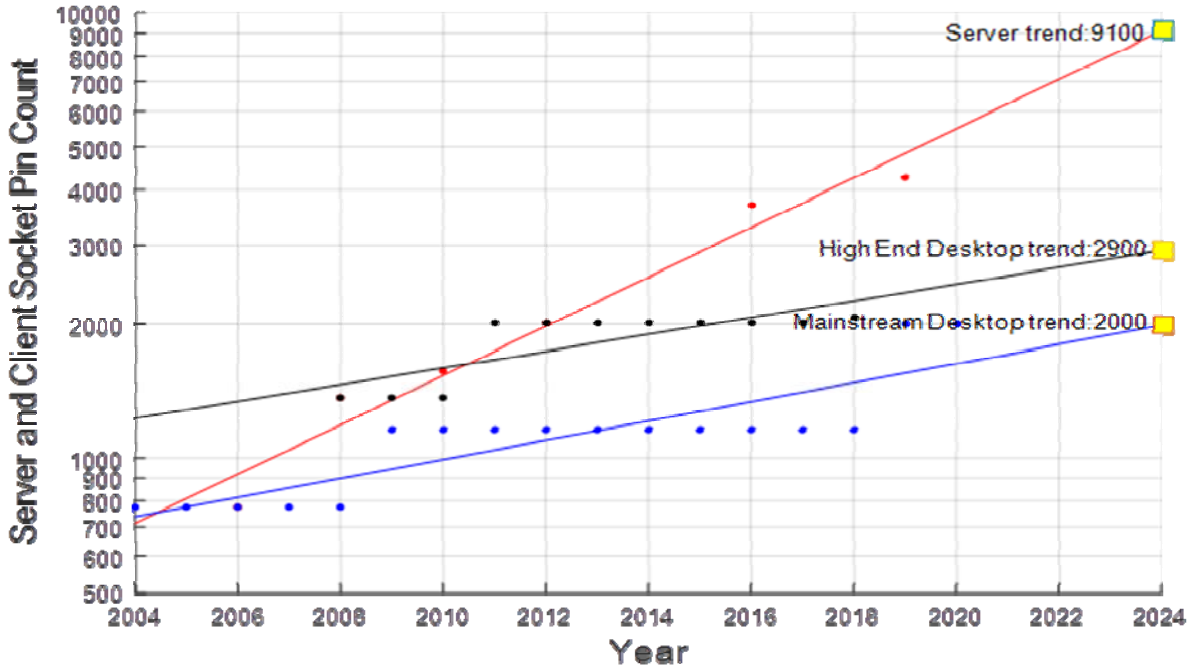


*Figure 3: Near term trend graph based on actual pin count evolution (Source: Intel)*

As described in [13], off-package bandwidth, electrical lane speeds and ASIC IO continue to scale steadily. In addition to pin-count scaling, socket constructions that minimize signaling losses should be developed. 2015 ITRS projections for BGA pitch continue to be valid.

(f) **POP (Package-on-Package) Interconnects:** The PoP construction [14] allows for packages to be placed on top of other packages using peripheral package interconnects, also referred to as VI (**V**ertical **I**nterconnects). It is

[6] The ball count for Mobile packages has been removed from this table. The 2015 projections show a flat trend and this trend needs additional study in light of the current evolution of mobile products.

typically used to stack memory packages on logic to create compact form factors. One such typical construction is shown in Figure 4.

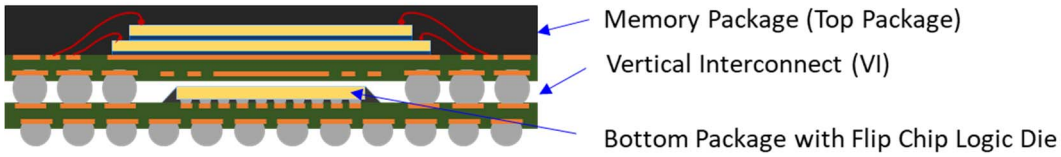


*Figure 4: Typical Package-on-Package Architecture.*

The VI pitch and the overall height of the package are two key characteristics for this architecture. Currently there is no methodology to project a roadmap for these architectures and in lieu of such a roadmap, the state-of-the-art pitches and package heights, along with their projected changes, are listed in Table 3.

| PoP Architectures | VI Pitch (mm) | Maximum Bottom Package Height (mm) |
|---|---|---|
| Bare Die PoP | 0.5 | 0.75 |
| Bare Die PoP with 2-Step solder resist (SR) + solder on pad (SOP) | 0.4 | 0.75 |
| TMV PoP | 0.4 | 0.78 |
| Exposed Die TMV PoP | 0.35 → 0.27 | 0.69 |
| Interposer PoP | 0.27 → 0.20 | 0.67 |
| FOWLP PoP | 0.30 → 0.20 | 0.50 → 0.30 |

*Table 3: State-of-the-Art Pitches and Package Heights and their projected targets for PoP Architectures*

## 5. Key Metrics

### *5.1 Design Attributes*[7]

***The physical attributes and signaling speeds needed to enable generation over generation BW doubling are described in this section.***

5.1.1 Peripheral Interconnects for 2D and Enhanced-2D Architectures

A key role of packaging is to provide physical interconnects.[8] The two design metrics that describe the capability of these interconnects are linear escape density and areal escape density. These two metrics are shown in Figure 5A. Note that these two can be combined into a single metric by multiplying the two (Figure 5B). Tables 4-6 show possible ways of physical interconnect scaling to achieve raw bandwidth doubling generation over generation. It is important to emphasize that the physical IO dimensions listed are not bounding parameters and depend on specific business and technical demands – i.e. the same bandwidth doubling can be achieved through more or less aggressive choices of the physical IO dimensions.

[7] 2D to 3D packaging architectures provide the physical construction architecture to enable signaling and power delivery. To the first order, these physical constructions are agnostic to the IO protocols for which they are used. Hence all attributes described here are independent of the IO protocol.

[8] These interconnects must be designed to minimize power dissipation and signal distortion in addition to provide effective interconnects [15, 16, 17].

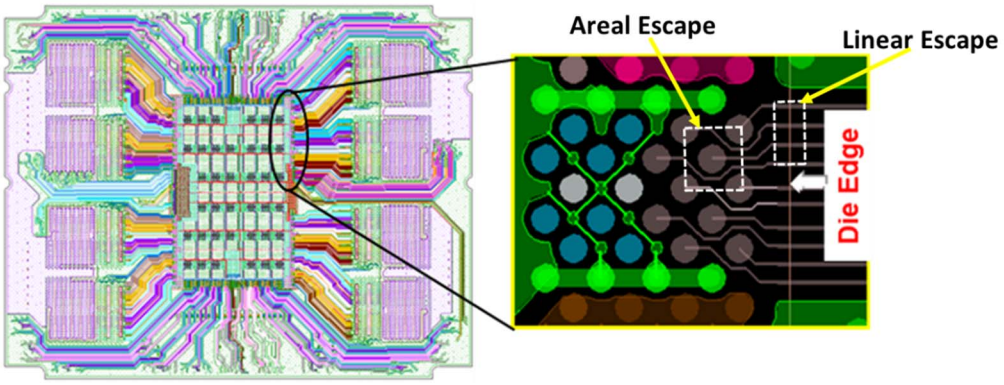


*Figure 5A: Two Key Physical Design Attributes: (a) IO/mm (of die edge) - Linear Escape Density and (b) IO/mm² (of die) - Areal Escape Density. Note that the term IO here refers to physical bumps and wires.*

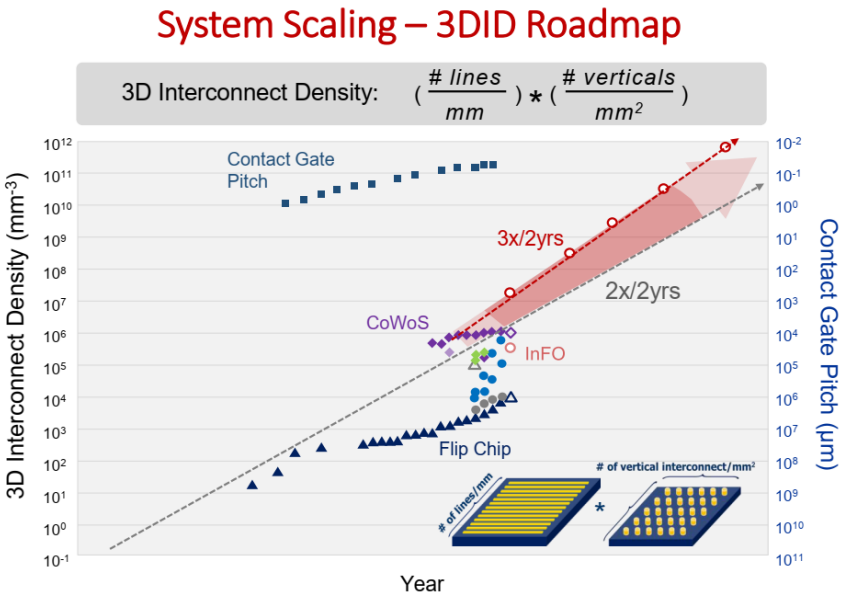


*Figure 5B: Two Key Physical Design Attributes: (a) IO/mm (of die edge) - Linear Escape Density, and (b) IO/mm² (of die edge) - Areal Escape Density. These are multiplied to create a single 3D Interconnect Density (3DID). Note that the term IO here refers to physical bumps and wires. (source: TSMC)*

| **Generations**[9] | | **1** | **2** | **3** | **4** | **5** |
|---|---|---|---|---|---|---|
| Raw Linear Bandwidth Density (GBps/mm)[10,11,12] | | 125 | 250 | 500 | 1000 | 2000 |
| Package Technology | Minimum Bump Pitch (µm) | 55 | 50 | 40 | 35 | 30 |
| | Linear Escape Density (IO/mm)[13] | 500 | 667 | 1000 | 1500 | 2000 |
| | Areal Escape Density (IO/mm²) | 331 | 400 | 625 | 816 | 1111 |
| Signaling Speed (Gbps)[14] | | 2 | 3 | 4 | 5.33 | 8 |

*Table 4: Physical IO Scaling Roadmap for Solder-based Interconnects*

[9] At present there is no universal understanding of the required time gap between generations. The TWG judgment is that it will be a minimum of 2 years, and from a planning perspective we recommend a maximum of 3 years, to ensure that the interconnect roadmap is competitive.

[10] Per mm of die edge.

[11] Starting value of 125 GBps/mm is estimated raw bandwidth possible in an AIB style implementation.

[12] Raw Bandwidth is essentially the product of # of connections and signaling speed per connection. Achieved bandwidth will be lower since not all connections are used for data transmission. The starting point of 125 GBps/mm is a judged value.

[13] Since multiple silicon back-end layers or package layers can be used to route the bumps, specific geometrical features of the layers are not described.

[14] Representative example showing how the BW goals are reached. These speeds are not unique.

| Generations | | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|---|
| Raw Linear Bandwidth Density (GBps/mm) | | 125 | 250 | 500 | 1000 | 2000 |
| Package Technology | Minimum Bump Pitch (μm)[15] | 55 | 40 | 30 | 20 | 10 |
| | Linear Escape Density (IO/mm) | 500 | 667 | 1000 | 2000 | 4000 |
| | Areal Escape Density (IO/mm$^2$) | 331 | 625 | 1111 | 2500 | 10000 |
| Signaling Speed (Gbps) | | 2 | 3 | 4 | 4 | 4 |

*Table 5: Physical IO Scaling Roadmap for solder and hybrid interconnects [18-23]*

5.1.2 Area Interconnects for 3D Architectures

| Generations | | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|---|
| Raw Areal Bandwidth Density (GBps/mm$^2$)[16] | | 125 | 250 | 500 | 1000 | 2000 |
| Package Technology | Minimum Bump Pitch (μm)[17] | 40 | 30 | 20 | 15 | 10 |
| | Areal Escape Density (IO/mm$^2$) | 625 | 1111 | 2500 | 4444 | 10000 |
| Signaling Speed (Gbps) | | 1.5-2 | 1.5-2 | 1.5-2 | 1.5-2 | 1.5-2 |

*Table 6: Physical IO Scaling Roadmap for solder and hybrid interconnects*

### *5.2 Signal Integrity Attributes*

The short and high-density interconnects described in Section 5.1.1 become more and more RC dominated with the generational scaling. The interconnect inductance is expected to have a secondary effect on the channel performance.

5.2.1 Signal Integrity Attributes for 2D and Enhanced 2D Architectures

| Generations | | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|---|
| Linear Bandwidth Density (GBps/mm) | | 125 | 250 | 500 | 1000 | 2000 |
| Channel Performance | Channel Length (mm) | <2 | <1.7 | <1.4 | <1.1 | <0.8 |
| | Bump-to-Bump Channel RC (ps) | <10 | <10 | <10 | <10 | <10 |

*Table 7: Channel Signaling Characteristics for 2D Architectures*

5.2.2 Area Interconnects

The signal integrity performance of the extremely short-area vertical interconnects is dominated by their capacitance. Their resistance and inductance are expected to have a secondary impact on the channel performance with the generational scaling.

| Generations | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|
| Areal Bandwidth Density (GBps/mm$^2$) | 125 | 250 | 500 | 1000 | 2000 |
| Bump Capacitance (fF) | <30 | <22 | <15 | <10 | <7 |

*Table 8: Channel Signaling Characteristics for 3D Architectures*

### *5.3 Power Delivery Attributes: Area Interconnects for 2D and 3D Architectures*

5.4.1 Area Interconnects for 2D and 3D Architectures

| Generations | | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|---|
| Core Power Density (W/sqmm) | | 5 | 8 | 12 | 18 | 25 |
| | On-die MIM Capacitance Density (nF/mm$^2$) | 400 | 100 | 200 | 300 | 400 |
| | Silicon Trench Capacitance Density (nF/mm$^2$) | 300 | 500 | 1000 | 1750 | 3000 |
| | VR Power Density (W/mm$^2$) | 0.4 | 0.6 | 1 | 1.5 | 2 |
| | Ceramic Cap Density (μF/mm$^2$) | 40 | 50 | 60 | 700 | 800 |
| | Bump Current Carrying Capability (A/mm$^2$) | 6 | 9 | 14 | 20 | 30 |

*Table 9: Power delivery Attributes for 2D and 3D Architectures.*
*It should be noted that power delivery attributes are agnostic to the architecture*

## 6. Difficult Challenges

The high IO/mm values listed in Tables 4 and 5 are achieved using silicon back-end technologies to create thin, closely spaced wires (Figure 6). This roadmap projects the need for increasing density, i.e., reduced line pitch. When

[15] Starting value of 55μm is based on the most common current implementation, i.e., HBM.
[16] Per mm$^2$ of die area.
[17] Starting value of 40 μm bump pitch based on known implementations in HBM and WIO2. .

combined with increasing signal speeds, there will be greater concerns about signal quality due to increased cross-talk caused by the reduced line spacing. The packaging community will be challenged to develop solutions that minimize impact to signal integrity and provide physical links with improved power efficiency.[18]

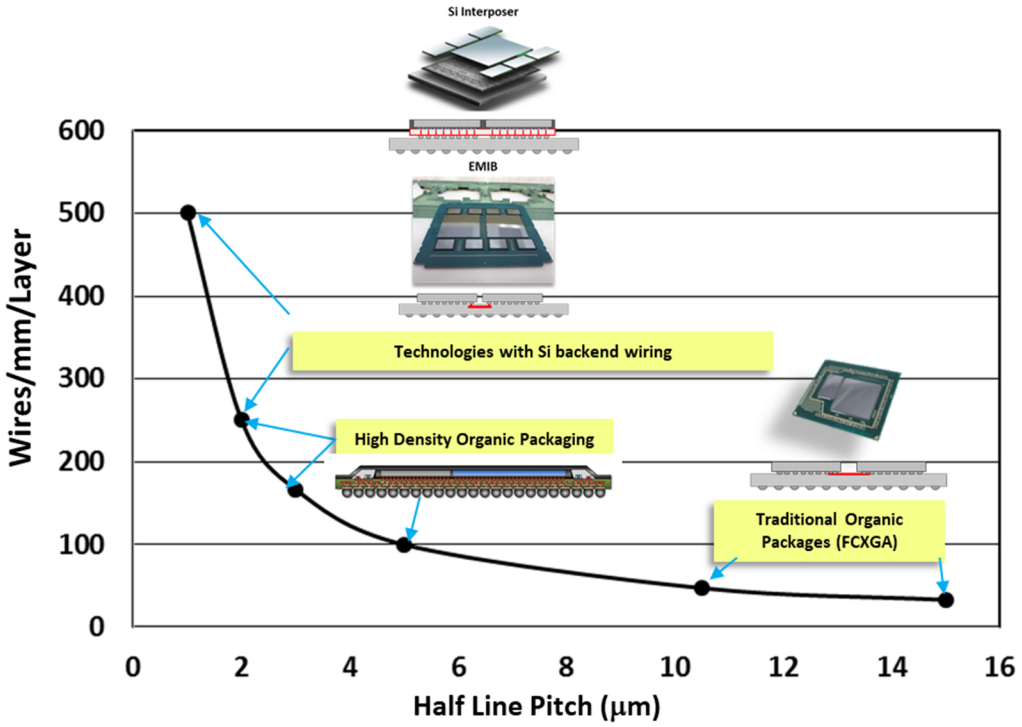


*Figure 6: Technologies for different wiring features. L is the width of the line in µm, S is the minimum space between lines in µm; half line pitch is (L+S)/2. Technologies that use silicon backend wiring can achieve wiring densities of greater than 1000 with L & S ≤ 0.5µm.*

There will be greater need to enable novel assembly technologies for ultra-fine pitch enhanced-2D and 3D architectures using both solder and non-solder-based approaches. A number of researchers have demonstrated the reduced bump pitches described in Table 4 and there is a fairly good understanding of the technologies needed to transition from solder-based interconnects to solderless interconnects [18-23]. Key challenges for stacked-die architectures will continue to be in fine pitch sort/test, thermal management, power delivery network development, design process co-design, in-line process control and equipment readiness for high volume.

## 7. Discussion

The primary driver for advanced 2D and 3D packaging technologies is the need for increased interconnect densities to support HI and deliver increasing bandwidth in a power efficient manner while enabling efficient power delivery. An increasing number of innovative packaging architectures deliver significantly improved HI envelopes, e.g., while the 2019 version of this chapter was being matured and after its publication, quite a few new architectures some of which include and enable stacking of active chips, have been announced [24-27]. In these HI architectures physical interconnects (i.e. wires, bumps) and link RC characteristics are completely under the control of packaging technologists and it is relatively easy to establish a non-unique scaling roadmap. Already number of power efficient, high bandwidth IO links that take advantage of advanced packaging have been defined to further spur the proliferation of heterogeneous integration [28-32]. We anticipate that moving forward, this chapter will spur discussion among product architects and will help develop further clarity on various use cases that will drive the pace of technology innovation. Even though it is not the focus of this chapter, it is also important to note that the ability to integrate the right thermal features will define the physical envelope (i.e. form factor and number of die/die stacks that can be integrated on the package) and the warpage characteristics that will ensure manufacturability [33].

[18] Power efficiency (measured in pJ/bit) is a sum of Tx, Rx and link power efficiency. The die-die links need to provide reducing RC (Table 6) to ensure improved power efficiency.

**8. Acknowledgments**

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