HETEROGENEOUS INTEGRATION ROADMAP

2019 Edition

Chapter 1: HIR Overview and Executive Summary

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Chapter 1: Heterogeneous Integration Roadmap: Driving Force and Enabling Technology for Systems of the Future

Executive Summary

1. Vision

The Heterogeneous Integration Roadmap (HIR) provides a long-term vision for the electronics industry, identifying difficult future challenges and potential solutions. The roadmap offers professionals, industry, academia, and research institutes a comprehensive view of the landscape and strategic technology requirements for the electronics industry's evolution over the next 15 years, and provides a 25-year vision for the heterogeneous integration of emerging devices and emerging materials with longer research and development timelines. The purpose is to stimulate precompetitive collaboration and thereby accelerate the pace of progress.

The HIR team is comprised of 22 Technical Working Groups representing the interactive complexities of the electronics ecosystem. It is a volunteer initiative drawing critical expert professionals from across industry, academia, and research institutes for the common good. The HIR is sponsored by three IEEE[1] Societies (Electronics Packaging Society[2], Electron Devices Society[3], and Photonics Society[4]), SEMI[5], and ASME EPPD[6], representing a wide cross-section of the global electronics community.

2. Prologue

The year 2019 marks the 50th anniversary of mankind's landing on the Moon, an initiative first publicly proposed by US President John Kennedy at Rice University in May 1962. In a stirring speech, he announced, *"We choose to go to the Moon in this decade and do the other things, not because they are easy, but because they are hard, because that goal will serve to organize and measure the best of our energies and skills, because that challenge is one that we are willing to accept, one we are unwilling to postpone ..."*

Before the end of that decade, on 14 July 1969, men indeed landed on the moon by way of the Apollo 11 mission. The moment has been forever immortalized through the powerful quote from Neil Armstrong as he stepped off the lunar module, followed by fellow astronaut Buzz Adrin: *"That's one small step for a man, one giant leap for mankind."*

The Moon landing was undeniably an engineering and scientific achievement of gigantic proportion, made possible only by many technological innovations and marvels of human ingenuity. Not least was the electronics and semiconductor innovation and creativity that went into the design of the Apollo Lunar Landing Module's Computer.

1962 was an exciting time for the electronics industry. For semiconductor companies, integrated circuits (ICs) had been invented just a few years back by Jack Kilby of Texas Instruments and Robert Noyce of Fairchild Camara. NASA and computer companies were asking themselves: When and how can we adopt this newly invented integrated circuit, trading off performance advantage against the risk of a new technology with issues of supply, quality and reliability? NASA engaged the MIT Instrument Lab (later named Draper Lab) for a comprehensive study on which technology to adopt for the Apollo Lunar Module Computer. The report given by Eldon Hall from the MIT Instrument Lab to Charles Frisk at the NASA Apollo Program Office in November 1962 recommended proceeding with the integrated circuit [1]. Fairchild Camera, Texas Instruments, and Motorola were among the IC suppliers.

We do not know how much Gordon Moore, then at Fairchild Camera's Semiconductor Division, was involved with this NASA Apollo study nor with Fairchild Camera's NASA business. What we do know is that when he published the paper *"Cramming More Components onto Integrated Circuits"* in *Electronics* on 19 April 1965 [2], he was looking far beyond the military and space markets. His market vision is clearly depicted in a memorable cartoon showing home computers being sold directly to department store customers from a counter propped between the "notions" and "cosmetics" counters, and at a time when mainframe computers were room sized, housed in air-conditioned rooms, mostly just within banks and government institutions. (note: IBM launched the 360 mainframe system in June 1964).

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[1] The Institute of Electrical and Electronics Engineers, www.ieee.org
[2] IEEE-EPS, eps.ieee.org
[3] IEEE-EDS, eds.ieee.org
[4] IEEE-PS, www.photonicssociety.org
[5] SEMI (was Semiconductor Equipment and Materials International), www.semi.org
[6] American Society of Mechanical Engineers, Electronic and Photonic Packaging Division, www.asme.org

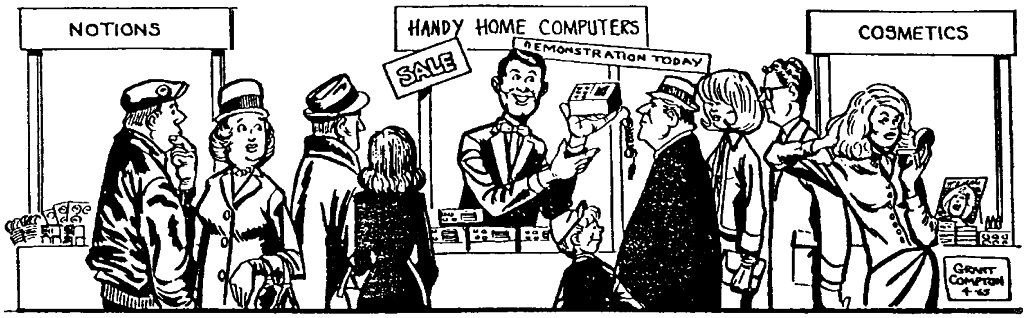

Figure 1. Cartoon from Moore's paper illustrating his market vision [1]

In a later section of his paper, titled *"Day of Reckoning",* he concluded with a remarkably prophetic statement: *"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically."* [2] Clearly, back then, he foresaw the home computer market for the consumer and the need for Heterogeneous Integration (HI) in the future. The electronics industry revenue in 2018 was US$2,126 billion [3], of which 44% was consumer spending in line with Gordon Moore's vision.

3. Disruptions and Changes

It has been more than 50 years since the invention of the integrated circuit. Since its inception in 1991, the International Technology Roadmap for Semiconductors (ITRS) [4] had been a guidepost for industry progress, projecting technology progress that followed the cadence of Moore's-Law scaling. While significant ongoing innovation in design and process technologies continue the drive to advanced nodes, Moore's-Law economics and performance are evidently plateauing. Shown below are two graphs presented by John Hennessy at the ERI Conference in July 2018 [5]. The graph to the left shows forty years of DRAM capacity and the slowing down of density, while the graph to the right shows forty years of computing performance with plateauing in the recent years.

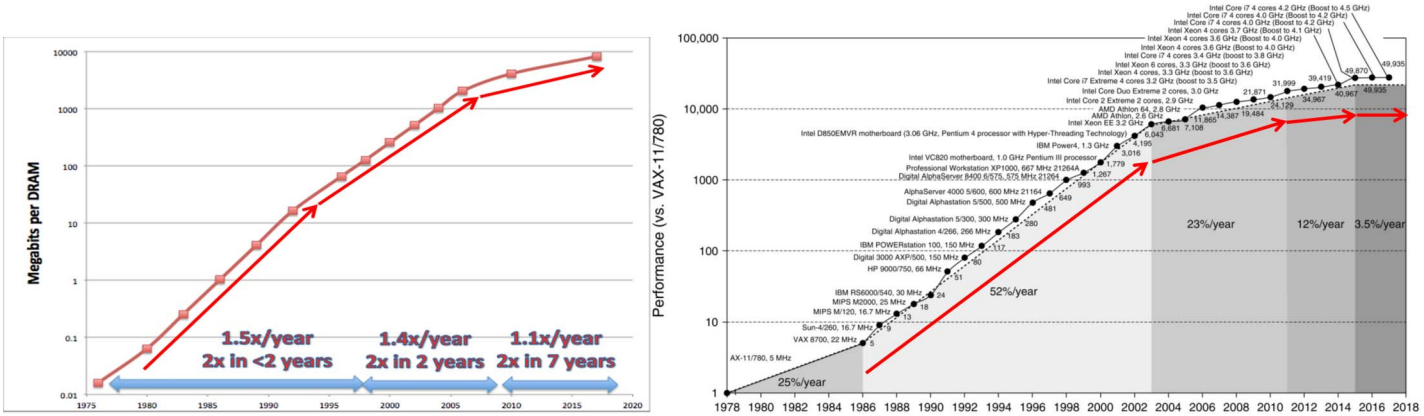

Figure 2. Plateauing of DRAM Density, and Computing Performance. Source: J Hennessy, ERI Conf July 2018

Figure 3. Die Cost Increase at Advanced Nodes. Source: Lisa Su [6] SEMICON WEST 2019

Shown in Figure 3 is a graph in a keynote presention by Lisa Su at SEMICON West, 9 July 2019 [6], showing that die "costs continue to increase" at advanced nodes.

The SIA[7] brought the ITRS to closure in July 2016, ending an era for ITRS roadmapping. But we are now in a new world order with changes and disruptions that we could never have imagined before, and the need for roadmapping has never been more clear. The business landscape is experiencing great change with the continued rise of technology companies that are driving social media, cloud computing, search, online commerce, and big data, leading to integrated hardware-software driven applications and unprecedented growth of application spaces.

2006	2019
• Exxon Mobil	➢ Apple
• General Electric	➢ Microsoft
• Gazprom	➢ Amazon
➢ Microsoft	➢ Alphabet
• Citicorp	➢ Berkshire Hathaway
• Bank of America	➢ Facebook
• Royal Dutch Shell	➢ Alibaba
• BP	➢ Tencent Holdings
• Petro China	• JP Morgan Chase
• HSBC	• Johnson & Johnson

Figure 4. Rise of the Tech Companies. Source: The Economist[6] & Statista

Figure 4 lists the top 10 publicly traded companies by market capitalization in 2006 and 2019. While there was only one tech company in the 2006 list, the 2019 list features the top four (and seven of the top ten) that are tech companies, signifying a powerful transition to the digital age [6].

There's a triple inflection point signified by the rise of tech companies and resulting disruption, comprising the plateauing of Moore's Law economics; the explosive expansion of digital data growth; and the coming of 5G and artificial intelligence. This calls for continued progress that requires a different phase of electronics innovation.

SIA & SRC[8] jointly published a report titled "Semiconductor Research Opportunities: An Industry Vision and Guide" in March 2017 [7]. In the report it stated*: "The path forward is not as clear as it was during the Moore's Law era. However, [there is] the enormous potential for economic and societal benefits – some that are envisioned and others yet to be imagined…. At this pivotal point, progress requires industry, government, and academia to step up … to be a key player in the spectrum of activities that will be necessary, from fundamental scientific research to commercial application."*

This Heterogeneous Integration Roadmap (HIR) is dedicated to embracing innovation wherever it arises and to promote collaboration wherever possible to accelerate progress in the microelectronics market landscape. The purpose is to provide a long-term vision for the electronics industry, identify difficult future challenges and propose potential solutions. The roadmap offers professionals, industry, academia, and research institutes a comprehensive view of the landscape and a strategic forecast of technology requirements for the electronics industry's evolution over the next 15 years. It also provides a 25-year vision for the heterogeneous integration of emerging devices and

[7] Semiconductor Industry Association, https://www.semiconductors.org
[8] Semiconductor Research Corporation, https://www.src.org

emerging materials with longer research and development timelines. The goal is to stimulate precompetitive collaboration and thereby accelerate the pace of progress.

Electronics are deeply embedded into the fabric of our society, changing the way we live, work and play while bringing new efficiencies to our global lifestyles, industries, and businesses. We are entering the era of the digital economy and myriad connectivity, and the market forces driving data growth include:

- Migration of data, logic, & applications to the cloud
- Consumerization of IT with the rise of social media
- Evolution in our mobile devices
- 5G communications together with Internet of Things (IoT) to Internet of Everything
- Artificial Intellegence (AI) with Virtual Reality (VR) Augmented Reality (AR)
- Autonomous vehicles

The six major markets are shown in the figure below:

Figure 5. Six application spaces undergirded by AI, VR and AR. Source: ASE

4. Heterogeneous Integration Roadmap

Heterogeneous Integration refers to the integration of separately manufactured components into a higher-level assembly (System in Package – SiP) that, in the aggregate, provides enhanced functionality and improved operating characteristics. *In this definition, components should be taken to mean any unit, whether individual die, MEMS device, passive component and assembled package or sub-system, that are integrated into a single package. The operating characteristics should also be taken in its broadest meaning including characteristics such as system-level performance and cost of ownership. Source: ITRS Assembly & Packaging Chapter.*

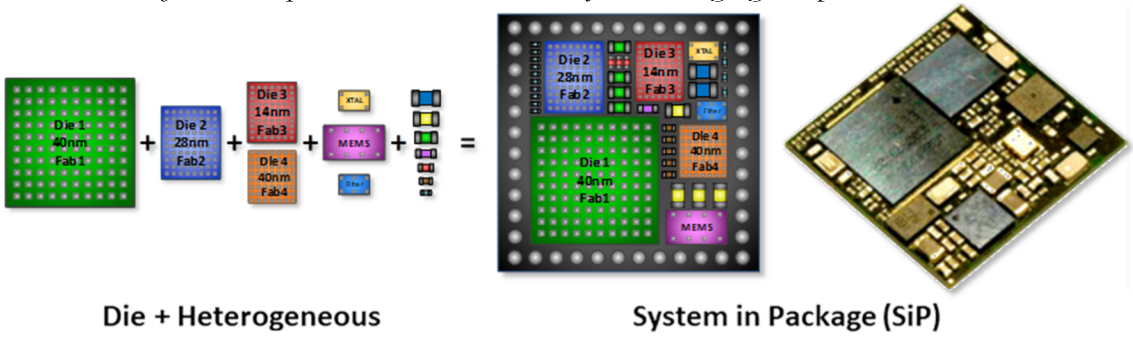

Figure 6. Heterogeneous Integration and System in Package (SiP). Source: ASE

Heterogeneous Integration through SiP follows naturally from the conceptual vision to build large, complex systems out of smaller functions separately packaged, as described in Gordon Moore's 1965 paper. Heterogeneity and associated integration is far-reaching and can relate to materials, component type, circuit type, node, interconnect method, and source or origin. There are many examples of Heterogneous Integration through SiP today.

Heterogeneous Integration is and will be the key technology direction going forward. It is the "low hanging fruit" for initiating a new era of technological and scientific advances to continue and complement the progression of Moore's Law Scaling into the distant future. Packaging – from system packaging to device packaging – will form the vanguard to this enormous advance.

The Heterogeneous Integration Roadmap is designed to be a system application-driven roadmap, blending the duality of market pull and technology push across the entire electronics ecosystem. Recognizing that future technology advances will be driven by advances in system integration in response to market applications, we have identified six market application areas that are the leading technology drivers for the Heterogeneous Integration Roadmap. They are:

- High Performance Computing and Data Centers
- Medical, Health and Wearables
- Autonomous Automotive
- Mobile
- Aerospace and Defense
- IoT

The key questions we attempt to answer are, *What are the building blocks for electronic systems? What integration technology progress is needed in these basic building blocks to keep system integration on track?*

The building blocks we envision are:

- Single Chip and Multi Chip Integration (including substrates)
- Integrated Photonics
- Integrated Power Electronics
- MEMS and Sensor integration
- 5G and Analog and Mixed Signal

Underlying these building blocks are technical areas that cut across all the market application segments:

- Materials and Emerging Research Materials
- Emerging Research Devices
- Test
- Supply Chain
- Security
- Thermal Management
- Co-Design
- Simulation

Finally, we have identified three major technology areas for Heterogeneous Integration:

- SiP
- 3D & 2D Interconnects
- Wafer-Level Packaging – WLP (fan in and fan out)

Altogether the Heterogeneous Integration Roadmap contains 23 chapters including the Executive Summary.

5. Highlights: Heterogeneous Integration Applications

1.) Now in production are silicon interposer-based integrations of advanced-node ASICs along with high-bandwidth memory (HBM) stacks. The example below (Figure 7) is AMD's Fiji GPU with 4 HBM, first in production at ASE in 2016 for gaming applications.

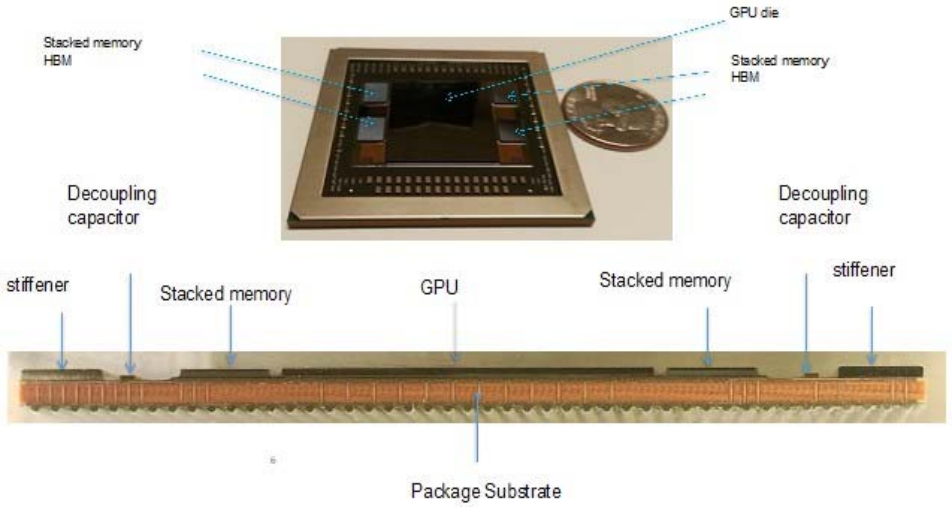

Figure 7. AMD Fiji GPU-HBM Si Interposer 2.5D Package. Source: ASE

2.) Intel's embedded multi-die interconnect bridge (EMIB) technology has been appled to a Chiplet application, where a silicon bridge is used to link multiple die together in close proximity on an organic substrate. Components of different nodes or from different companies can be heterogeneously integrated together in one SiP. Shown in Figure 8 is Intel's Agilex FPGA in a chiplet application.

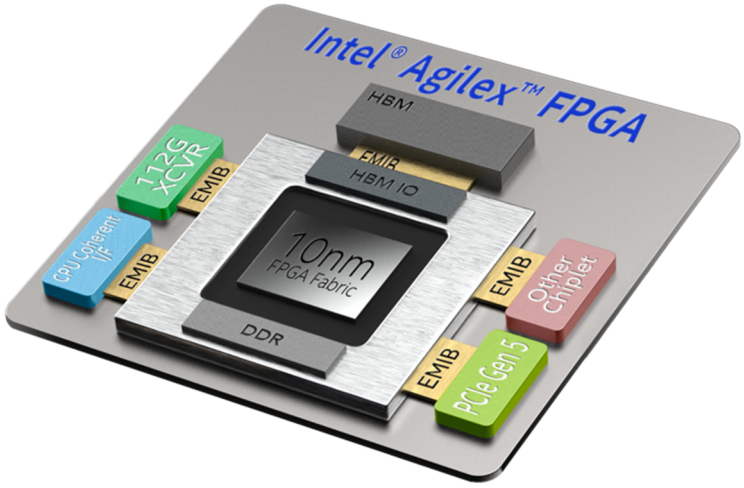

Figure 8. Intel Agilex FPGA Chiplet application. Source: Intel

At advanced nodes, the die yield falls exponentially with die size. Splitting a large monolithic SoC into smaller tightly coupled die, first demonstrated by Xilinx on a silicon interposer, is now being seriously considered and executed. At the same time, die cost per unit area is escalating [5]. As reported in Chapter 8 (Single Chip and Multichip Packaging), below are two generations of the AMD EPYC server processors (Figure 9). To the left the large monolithic SoC has been split into four tightly coupled die (for better yield) called chiplets, using homogeneous integration on an organic substrate. To the right there are two groups of four 7-nm chiplets on each side of the larger 14-nm I/O die, using heterogeneous integration to optimize unit area die cost.

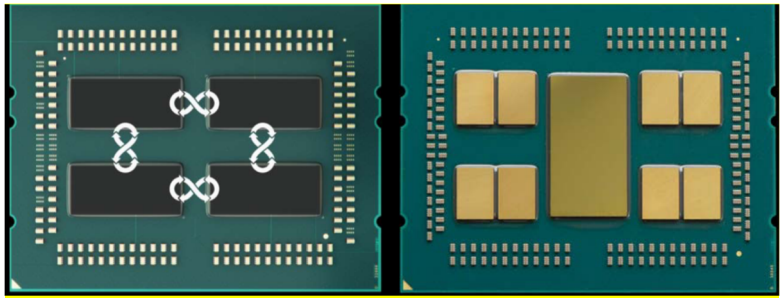

Figure 9. AMD EPYC Server Processors. Source: AMD [6]

3.) The CHIPS program is an important part of the DARPA Electronics Resurgence Initiative (ERI) helping drive HI. CHIPS stands for *Common Heterogeneous Integration and Intellectual Property (IP) Reuse Strategies Program.* The vision is an ecosystem of discrete modular IP blocks, to be assembled into a system using existing and emerging integration technologies. This is described in Chapter 21 (SiP and Module) and Chapter 6 (Aerospace and Defense). Recent updates of the program may be found at the 2019 ERI conference proceedings. Further information is found in Chapter 6.

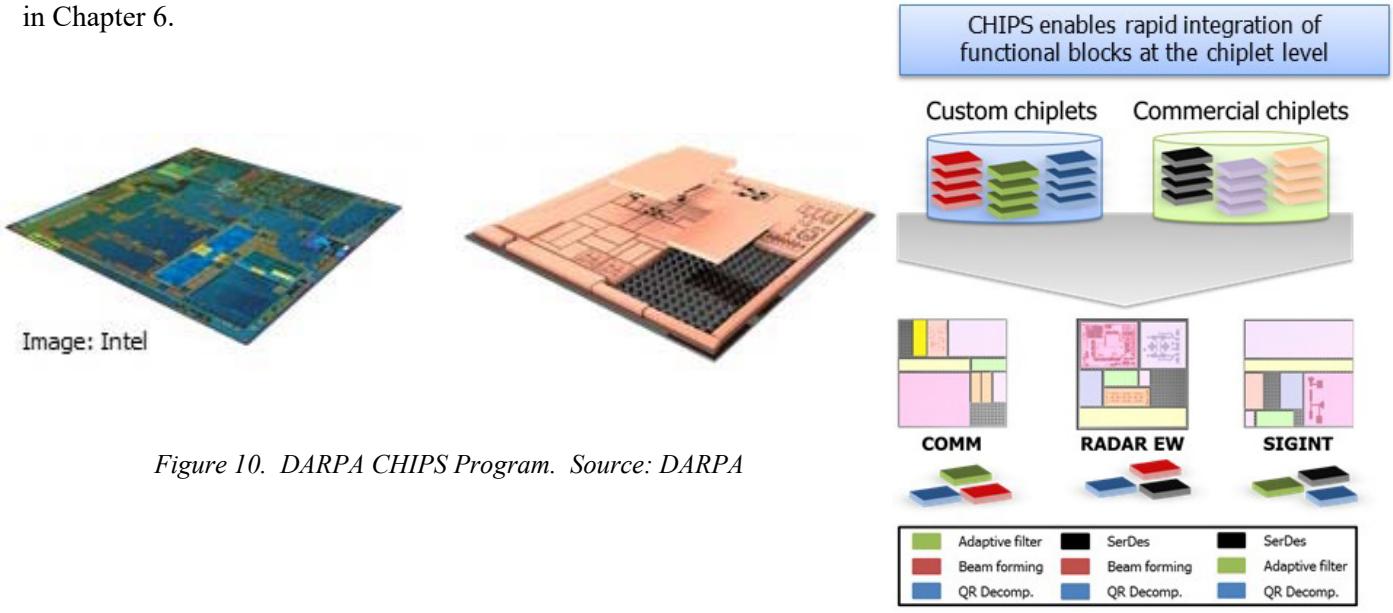

Figure 10. DARPA CHIPS Program. Source: DARPA

4.) The smartphone industry has been an early adopter of HI technologies in the use of SiP for multiple generations, essentially for the advantages in miniaturization, modularity for co-design, and enhanced generation-over-generation performance, extensively discussed in Chapter 7 (Mobile). The application processor is almost always on the most advanced node and housed in a Package on Package (PoP) configuration with memory component(s) stacked on top of this ASIC. Shown below are teardowns of the PoP packages for three premium Smartphones: Apple XS_{Max}, Samsung Galaxy S9+, and Huawei 20 Pro. They are examples of Wafer Level Fan-Out (TSMC[9] INFO), Panel Level Fan-Out (ePLP), and advanced high-bandwidth flip-chip PoP (Kirin), respectively.

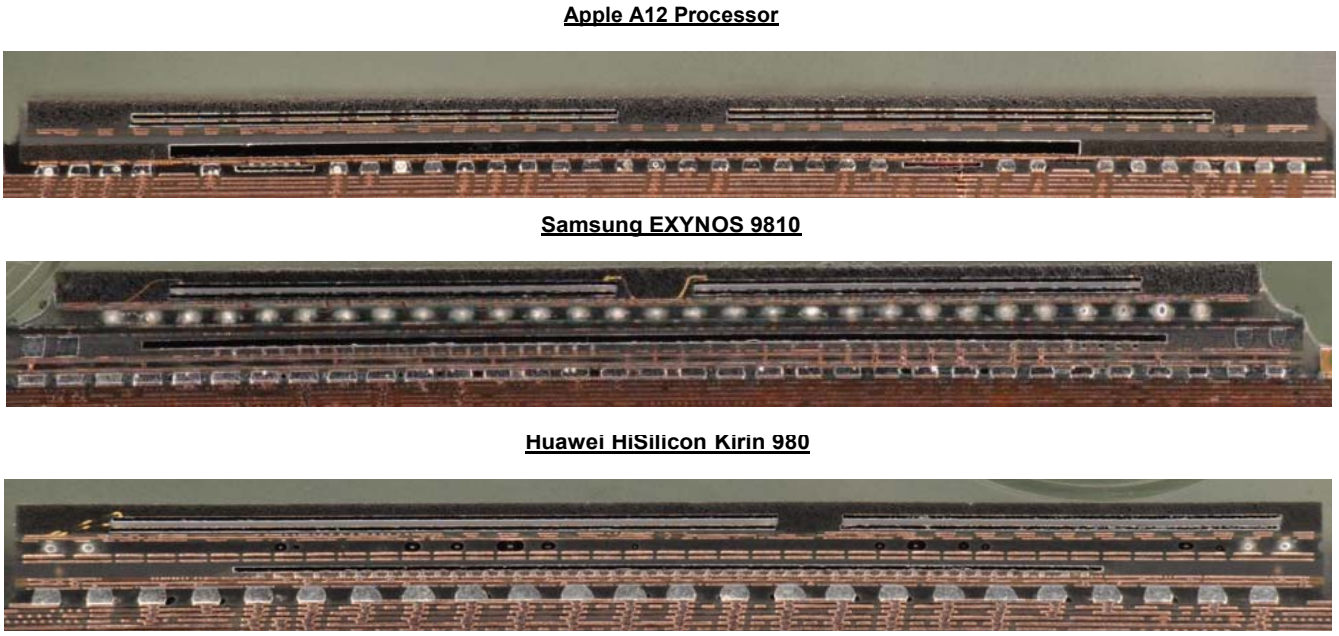

Figure 11. Three examples of Package on Package [PoP] in Smart Phone Teardowns. Source: Prismak Partners & Bingahmton University

[9] Taiwan Semiconductor Manufacturing Company, www.tsmc.com

5.) From Chapter 23 (WLP Fan-In and Fan-Out) we have two examples of Fan-Out technologies. Shown below is the Fan-Out Chip on Substrate with two die in close proximity in production.

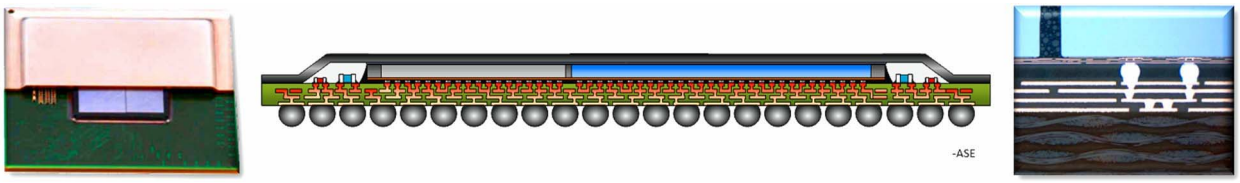

Figure 12. Fan-Out Chip on Substrate (HIR WLP Chapter, Figure 9)

6.) Taking this fan-out and stacking concept one step further, multiple SoCs and memories can be incorporated into a multilayer stackup using an advanced structure called 3D Multi-stack (MUST) system integration technology. This 3D MUST-in-MUST (3D-MiM) fanout package was described in reference [9] in a TSMC paper at the 2019 ECTC[10] conference.

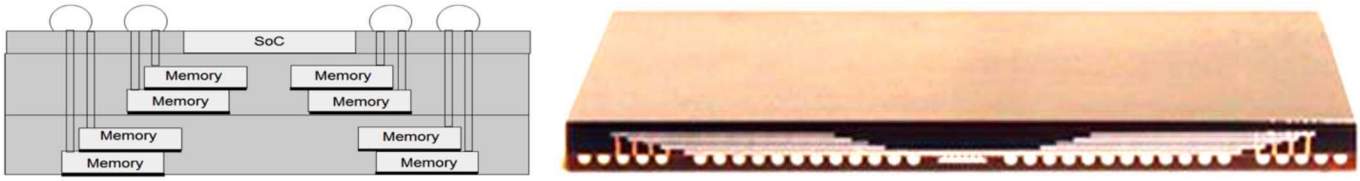

Figure 13. Fan-Out Multi-Stack integration (TSMC MiM). (WLP Chapter Figure 38, and ECTC 2019)

7.) In Chapter 21 (SiP and Modules), the SiP integration of Wide-Band-Gap (WBG) power semiconductors such as silicon carbide (SiC) and gallium-nitride (GaN) power systems in a package is discussed. Shown below is an example of an Embedded SiC half-wave bridge module; it provides very low parasitic inductance, allowing the use of very fast switching cells. Face-up and flipped dies are assembled to the substrate and embedded into epoxy prepreg layers. The substrate also provides excellent thermal management for the module. This module was developed at Fraunhofer IZM. Comparable modules have been industrialized by several suppliers.

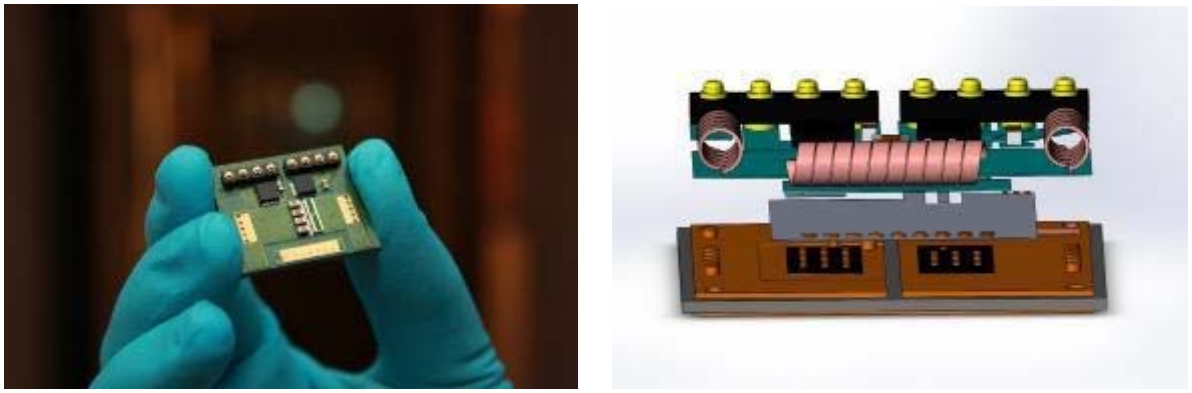

Figure 14. Example of EMI-optimized SiP SiC Module. Source: Fraunhofer IZM

8.) With the rollout of 5G networks in many cities, 5G smart phones are now becoming available. Shown below is a picture of the Samsung Galaxy S10 teardown. Note that there are three different mmWave Antenna modules positioned at the periphery of the frame, and that there is a 2G/3G/4G antenna module near the bottom of the frame. An indepth review of the 5G antenna technology may be found in Chapter 12 (5G Communications). More discussion on the Samsung Galaxy S10 PoP is in Chapter 7 (Mobile).

[10] Electronic Components and Technology Conference, http://www.ectc.net

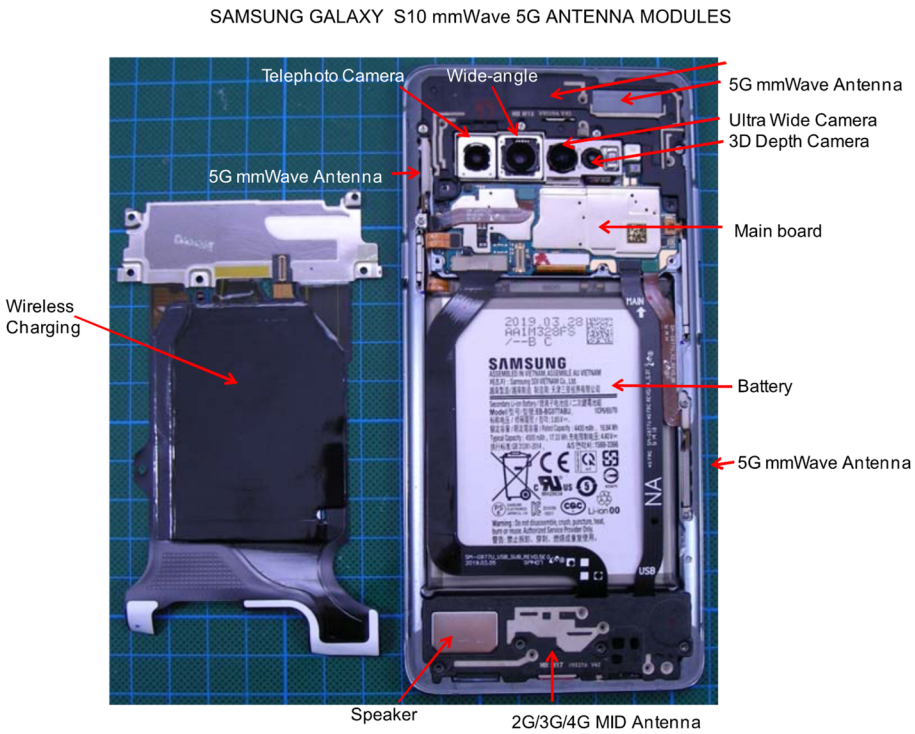

Figure 15. Samsung Galaxy 10 teardown showing 5G antennas. Source: Prismak Partners & Bingahmton University

6. What Comes Next

At the HIR workshop at SEMICON West 2019, John Shalf (LBNL11) presented a talk on the "Future of Computing beyond Moore's Law", specifically on the requirements for ExaScale Computing 2022-2023. Figure 16 shows the plateauing of the technology scaling trends and asks "**then what**?"

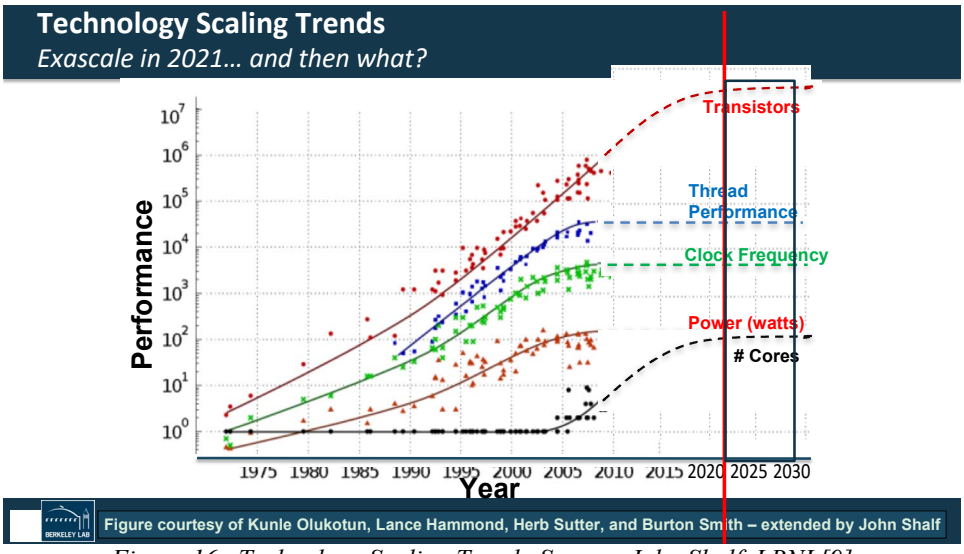

Figure 16. Technology Scaling Trend. Source: John Shalf, LBNL[9]

He further addresses a number of challenges and potential solutions. Noting that when using silicon interposers, the package's Cu-pin bandwith density matches the photonics badwith density, he showed a conceptual slide for silicon photonics co-integration. An in-depth review is to be found in Chapter 9 (Integrated Photonics).

[11] Lawrence Berkeley National Laboratory, https://www.lbl.gov

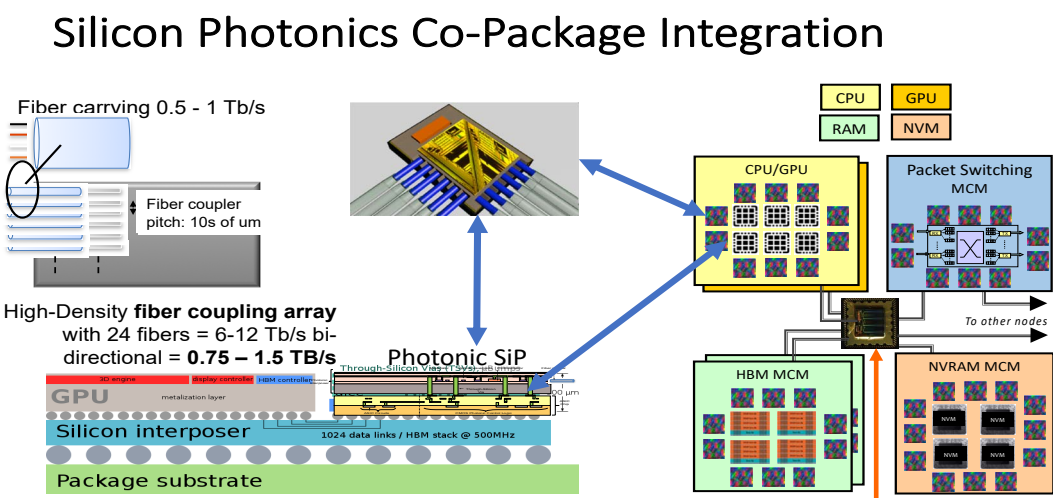

Figure 17. Si Photonics Integration Concept. Source: John Shalf (LBNL) [10]

7. Artificial Intelligence

At the AI Design Forum at SEMICON West 2019, Cliff Young (Google Research) gave a presentation on "Codesign for Google TPUs – How can Materials Help?" Shown in Figure 18, from the left, are pictures of three generations of the Tensor Processor Unit (TPU): TPU1, TPU2 and TPU3.

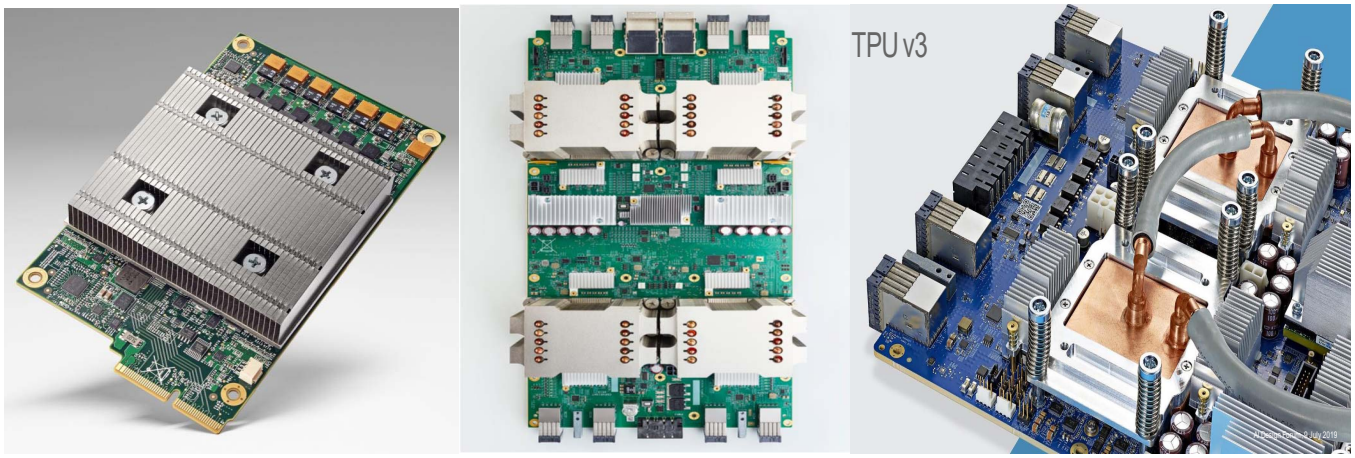

Figure 18. Three Generations of Google TPUs. Source: Cliff Young, Google Research [11]

At the end of the presentation he asked the rhetorical question, What does Google Need from this Community? The condensed version of his answer is:

- As much **more-than-Moore** as we can get;
- Options (possibly raw) that might be **off the main path**;
- True **codesign collaboration**.

He concluded his talk with Figure 19 and the message: "Deep Learning has Reinvigorated Hardware."

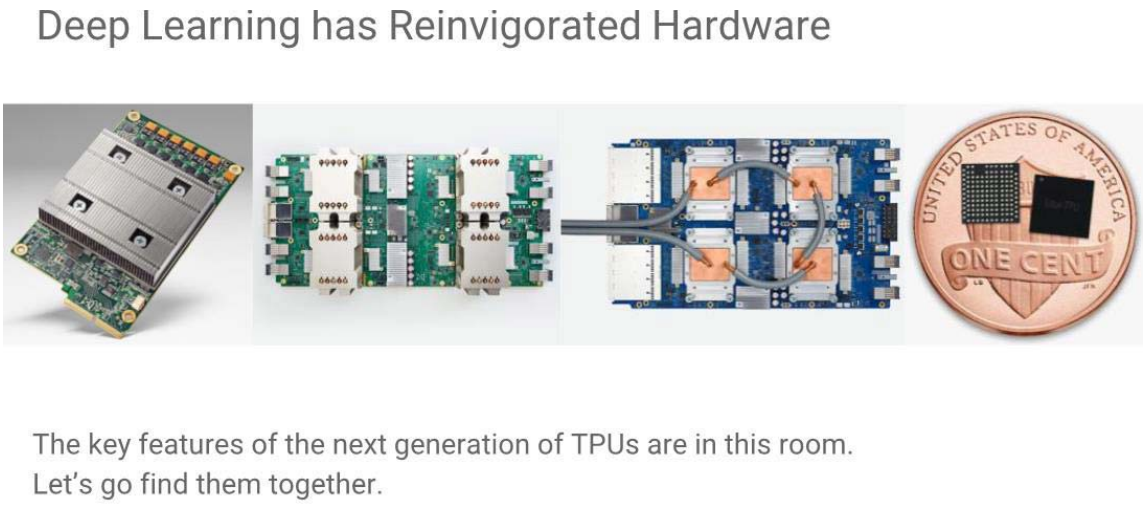

Figure 19. Hardware Reinvigoration. Source: Cliff Young, Google Research [11]

A very important message Cliff Young posed for the electronics engineering community is the opportunity afforded by artificial intellegence and deep learning on every thing we do, from co-design (Chapter 13) and simulation (Chapter 14) to development and manufacturing. This is a Grand Challenge and a Grand Opportunity.

8. Wrap-Up

Fifty years ago, the world was mesmerized and awestruck by the image of man walking on the Moon. Many youngsters were inspired not only by such an incredible achievement for the human race, but also by the words spoken by Armstrong. The role of the semiconductor in this considerable feat of engineering should absolutely be recognized. One major area of innovation in the decade-long effort that put man on the Moon was the electronics propelled by the earlier invention of transistors and emergence of integrated circuits.

Today, the US, China and India governments have all announced plans to explore space further, by sending astronauts and robots to planets and places deep within the solar system. There are also announcements from private companies who aspire to offer space travel and tours. The progress in electronics has indeed been astounding, but ongoing innovation will help pioneers achieve what might seem unimaginable today.

In Gordon Moore's 1965 celebrated paper *"Cramming More Components onto Integrated Circuits,"* his first focus was integration of transistors into integrated circuits*: "The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas."* In the 54 years since that time, the industry has succeeded tremendously well indeed, through investment, technology and the science of scaling or "cramming" billions of transistors into integrated circuits, over the evolution from wafers to chips and chips to electronics products. This was the "transistor focus" (Figure 20).

Figure 20. Integration with a Transistor Focus [11]

In the same 1965 paper, Gordon Moore identified a "system focus" while pointing out the value of heterogeneous integration.

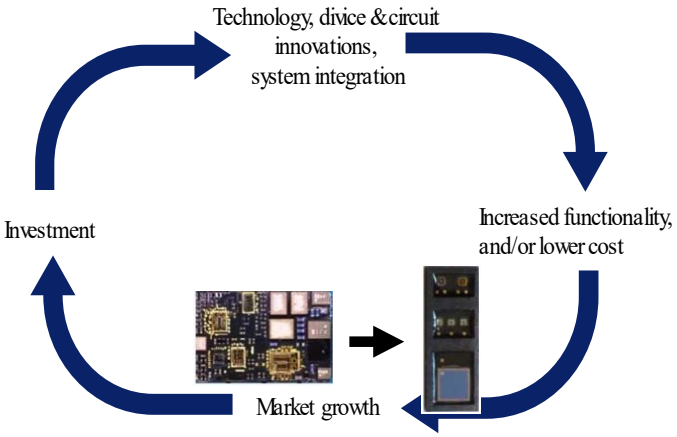

Figure 21. Integration with a System Focus [11]

Electronics packaging is fundamental to innovation in many industry applications and system products, across applications such as cloud computing, IoT, medical and health, automotive, aerospace, consumer, and home. The HI roadmap offers professionals, industry, academia, and research institutes a comprehensive view of the landscape and strategic forecast of technology requirements for the electronics industry's evolution over the next 15 years, and provides a 25-year vision for the heterogeneous integration of emerging devices and emerging materials with longer research and development timelines. The goal is to stimulate our total ecosystem towards precompetitive collaboration and thereby accelerate the pace of progress.

Summary

- The expanding digital economy – connectivity and network platforms, driven by 5G, IoT to IoE, smart devices, data to the cloud, and autonomous vehicles – is fast changing the electronics industry landscape.
- Within the digital disruptive markets, each has its own metric for performance, reliability, volume and cost tradeoffs. There is an immense need for pre-competitive technology roadmaps that address future vision, difficult challenges and potential solutions.
- Roadmaps are focused on system-level integration and advanced packaging technologies that address expanding markets and enable continued progress, just as the past 50 years have been propelled forward by following Moore's Law and the ITRS.
- Heterogeneous Integration is essential to maintain the pace of progress with higher performance, lower latency, smaller size, lighter weight, lower power requirement per function, and lower cost.
- The opportunity afforded by artificial intellegence and deep learning on everything we do, from co-design to development and manufacturing, will be a Grand Challenge as well as a Grand Opportunity.

References

1. "Journey to the Moon, History of the Apollo Guidance Computer", Eldon Hall, page 79
2. "Cramming More Components onto Integrated Circuits", Gordon Moore, pp 114 – 117, Electronics, 19 April 1965
3. Prismark Patners seminar at ASE Group, August 2019
4. International Technology Roadmap for Semiconductors (ITRS). ITRS Roadmap is sponsored by the Semiconductor Industry Association (SIA). ITRS 2015 edition may be found at the SIA Website.
5. "Semiconductor Research Opportunities, An Industry Vision and Guide", March 2017, was jointly sponsored by SRC and SIA. It may be found at the SRC website.
6. Presentation by John Hennessy, ERI Conference, 2018
7. Presentartion by Lisa Su, SEMICON West, July 2019
8. The Economist, 17 May 2017.
9. Presentation by John Shalf, HIR Vision Workshop, SEMICON West, Moscone Center, July 2019
10. Presentation by Cliff Young (Keynote), SEMICON West, Moscone Center, July 2019
11. Presentation by Yin Chang, ASE Group, SEMICON West, July 2018.

Appendix 1: Acknowledgments

A. HIR Chapters: Technical Working Group Chairs and Co-Chairs

The Heterogeneous Integration Roadmap is the result of dedicated collaboration and enormous effort by TWG members from across the electronics community. We acknowledge the primary contributions of the Working Group chairs and co-chairs:

Chapter 2: **High Performance Computing and Data Centers**
- Kanad Ghose and Dale Becker

Chapter 3: **Internet of Things (IoT)**
- Wei-Chang (Robert) Lo

Chapter 4: **Medical, Health and Wearables**
- Mark Poliks, Nancy Stoffel and Jan Vardaman

Chapter 5: **Automotive**
- Rich Rice, Venkatesh Sundaram and Urmi Ray

Chaper 6: **Aerospace and Defense**
- Tim Lee and Jeffrey Demmin

Chapter 7: **Mobile**
- William Chen, Benson Chan, Mark Gerber and Brandon Prior

Chapter 8: **Single Chip and Multi Chip Integration (including substrates)**
- William Chen and Annette Teng

Chapter 9: **Integrated Photonics**
- W R (Bill) Bottoms and Amr Helmy

Chapter 10: **Integrated Power Electronics**
- Patrick McClusky and Douglas Hopkins

Chapter 11: **MEMS and Sensor Integration**
- Shafi Saiyid

Chapter 12: **5G Communications**
- Tim Lee and Herbert Bennett

Chapter 13: **Co-Design**
- Jose Schutt-Aine and Andrew Kahng

Chapter 14: **Modeling and Simulation**
- Christopher Bailey and Xuejun Fan

Chapter 15: **Materials and Emerging Research Materials**
- W R (Bill) Bottoms

Chapter 16: **Emerging Research Devices**
- Meyya Meyyappan

Chapter 17: **Test**
- Dave Armstrong and Ken Lanier

Chapter 18: **Supply Chain**
- Tom Salmon and Paul Trio

Chapter 19: **Security**
- Sohrab Aftabjahani

Chapter 20: **Thermal Management**
- Madhusudan Iyengar, Avram Bar-Cohen and Azmat Malik

Chapter 21: **SiP and Modules**
- Rolf Aschenbrenner, Erik Jung and Klaus Pressel

Chapter 22: **2D and 3D Interconnects**
- Ravi Mahajan, Rajasekaran Swaminathan, Adeel Bajwa and Subramanian Iyer

Chapter 23: **WLP (fan in and fan out)**
- Rozalia Beica and John Hunt

B. Global Advisory Council

We wish to thank the Global Advisory Council members for their wisdom and guidance:

- Ajit Manocha – President & CEO, SEMI
- Babak Sabi – Corporate Vice President and Director, Assembly and Test Development, Intel
- Nicky Lu – Chairman, CEO & Founder, Etron Technology, Inc
- Herbert Lakner – Chairman of the Board of Directors of Fraunhofer Group Microelectronics

C. HIR International Roadmap Committee

- William (Bill) Chen (Chair)
- WR (Bill) Bottoms (Co-Chair; IEEE EPS)
- Tom Salmon (SEMI)
- Subramanian Iyer (IEEE EDS)
- Amr S. Helmy (IEEE Photonics)
- Ravi Mahajan (ASME EPPD)
- Gamal Rafai-Ahmed (alternate, ASME EPPD)

D. Administration and Editing

We wish to express our appreciation to Denise Manning, Executive Director of IEEE's Electronics Packaging Society, for her constant diligence, thoroughness and patience in support of the HIR initiative. We are also greatly indebted to Paul Wesling for his excellent editing and composition efforts, working with the TWG chairs and co-chairs and delivering the final product.

Edited by Paul Wesling