HETEROGENEOUS INTEGRATION ROADMAP

2021 Edition

Chapter 24: Reliability

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Chapter 24: Reliability of Heterogeneous Integration Systems

1. Executive Summary

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This chapter examines the reliability implications of 'SysMoore', i.e. the system-level heterogeneous integration (HI) that is being developed as a means to keep delivering the rate of performance increase that we have come to expect based on Moore's Law. Increasing system complexity, functionality, diversity and density, as a result of the twin drives for HI and on-chip advances, will pose new challenges for meeting and verifying customers' reliability targets. Multifunctional HI systems of the future are expected to be complex multiscale and multiphysics systems. Heterogeneous integration requires a convergence between the semiconductor industry and the packaging industry, and a unified reliability approach across the entire product architecture hierarchy from device level to package, boards/modules and systems. The resulting complex chip-package-board interactions (CPBI) will pose new reliability challenges and will need to be addressed by an integrated reliability team across all these levels of device-to-system integration, to meet the customer's reliability targets. HI reliability engineers will also need to meet holistic constraints such as reducing the time required for new product introduction (NPI) and minimizing cost of ownership over the life-cycle of successive generations of products. Such an integrated approach towards reliability will require a rigorous, disciplined and proactive fusion approach that strategically combines a bottom-up reliability physics approach with a top-down approach that leverages powerful artificial intelligence algorithms and the unprecedented levels of real-time field performance data, service condition data, product stress data and system/component reliability data that is becoming available via the IoT infrastructure. HI systems of the future are expected to combine highly resilient designs with self-monitoring, self-cognizance and varying degrees of adaptive reconfiguration and self-healing capabilities to provide high reliability and availability, in the presence of high diversity of technologies and potential stochastic distributions of intrinsic material and manufacturing variabilities. This chapter lays out the scope, challenges, disruptive opportunities and potential approaches for achieving such an integrated reliability approach for HI technologies, that are likely to emerge over the next 0-5, 5-10 and 10-15 years.

2. HI System Reliability: Introduction and Scope

Reliability describes the ability of products to meet intended performance targets throughout their useful life. The metric often used to quantify reliability is the time-dependent probability of meeting the intended performance goals. Related metrics are the histories of the instantaneous failure rates and hazard rates. Developing, operating and supporting reliable HI systems will require consideration of factors such as hardware reliability, software reliability, human operator reliability, cyber security and their interactions. This current chapter will focus predominantly on hardware reliability risks. The additional risk factors listed above will be addressed in future editions of this chapter.

Reliability risks in hardware systems come from a combination of cumulative aging and degradation due to *wearout* aging mechanisms and unexpected catastrophic degradation/failures due to *overstress* events during the lifecycle. Optimum hardware reliability can be achieved by understanding the reliability expectations, product micro/macro environment and impact of the environment on wearout behavior based on product technology characteristics. As illustrated in Figure 1, at the simplest level, reliability risk is often visualized as a stress-strength interference, where unreliability comes from the probability that the applied 'stress' will exceed the inherent 'strength' of the product. The tasks of managing reliability include effective ways to quantify these distributions (and their evolution throughout the life-cycle) and balancing their interactions, as a function of product design, manufacturing variabilities and service expectations, to ensure that the resulting reliability margins will meet the customer's expectations.

The process of quantifying and managing the time-dependent 'stress' and 'strength' interference requires science-based multi-physics, multiscale co-design approaches that leverage the rich disciplines of multi-physics simulations, reliability physics (RP) and artificial intelligence (AI). The 'stress' distributions will have to be identified based on a combination of multi-physics simulation and data-driven AI approaches. AI approaches will have to be based on sophisticated machine learning methods that exploit data analytics and deep learning technologies. The outcome of this 'stress analysis' will help to identify the intensity of the electrical, thermal, mechanical and chemical fields expected at potential failure sites throughout the expected life cycle of the product. Simultaneously, identifying the corresponding multi-physics 'strength' distributions will require a similar combination of fundamental RP models and advanced AI methods.

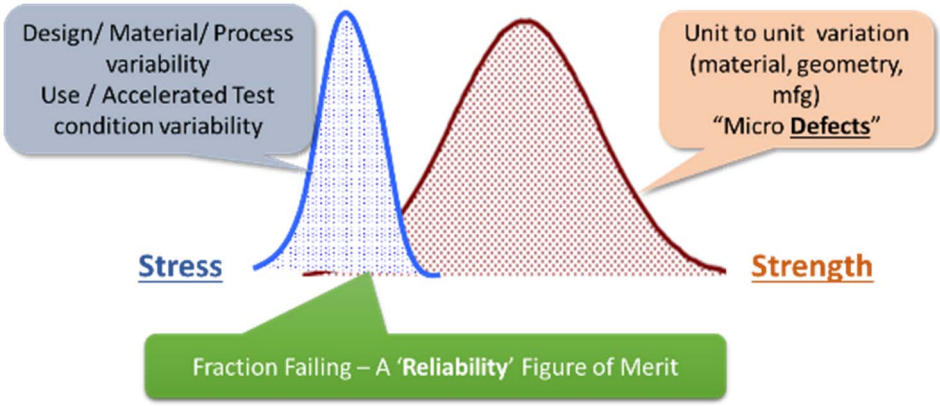
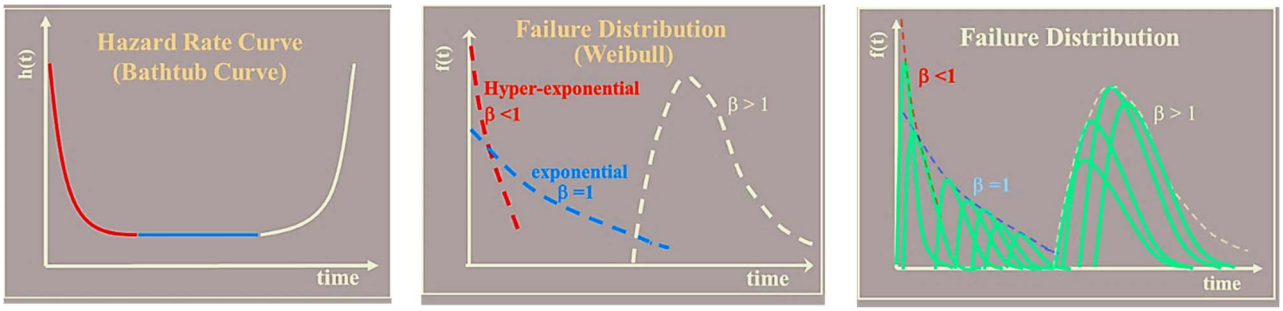


Figure 1: 'Stress' vs. 'Strength' interference

RP uses a 'bottom-up' approach to enable robust design margins based on assessment of dominant degradation/failure mechanisms at critical sites, while AI provides a complementary 'top-down' perspective of system-level risk, based on the unprecedented level of real-time field reliability data and user profile data that will become available via the IoT infrastructure. This fusion approach will be able to leverage prior AI knowledge and RP assessments, to minimize accelerated stress-testing, thereby shortening product development cycles.

The concept of a RP perspective of system-level risk is schematically illustrated in Figure 2, where the traditional system-level reliability 'bathtub' curve is shown in terms of hazard rates in Figure 2a and probability density functions (pdfs) in Figure 2b. Figure 2c emphasizes the corresponding 'bottom-up' RP view that this system-level failure information is actually the result of many competing degradation/failure mechanisms that are active at multiple critical failure sites. End-of-life failures (under the white section of the bathtub curve in Figure 2) depend on the intrinsic robustness of the design. The pre-mature failures (under the red and blue portions of the bathtub curve) depend on the distribution of weak sub-populations due to manufacturing and materials variabilities/defects. In complex, multi-physics, multi-scale HI systems, developers will be able to leverage both RP (bottom-up) and AI (top-down) approaches to estimate these failure rates. In turn, this will lead to unique opportunities to ensure system robustness and resilience, reduce time to market and minimize cost of ownership.

Figure 3a provides a sample listing of the dominant multi-physics degradation mechanisms in electronic systems, divided for convenience into two categories: (i) 'Overstress' mechanisms are triggered by the action of sudden catastrophic stress events; and (ii)'wearout' mechanisms that cause gradual damage accumulation throughout the life cycle because of routine operational and environmental sustained stress exposures. For convenience, mechanisms in both categories are further grouped by the dominant stress type that activates each mechanism: (a) Mechanical stresses; (b) Temperature; (c) Electrical stresses; (d) High-energy particle radiation; (d) Harsh chemical contaminants.



(a) *(b)* *(c)*

Figure 2a: Bathtub Curve showing system-level hazard rates for 3 phases ('infant mortality' stage in red, 'usable life' in blue and 'end-of-life' stage in white);
Figure 2b: Three phases of the Bathtub curve replotted as scaled probability density functions;
Figure 2c: Schematic illustration of underlying competing failure distributions (due to competing failure mechanisms) that constitute the bathtub curve.

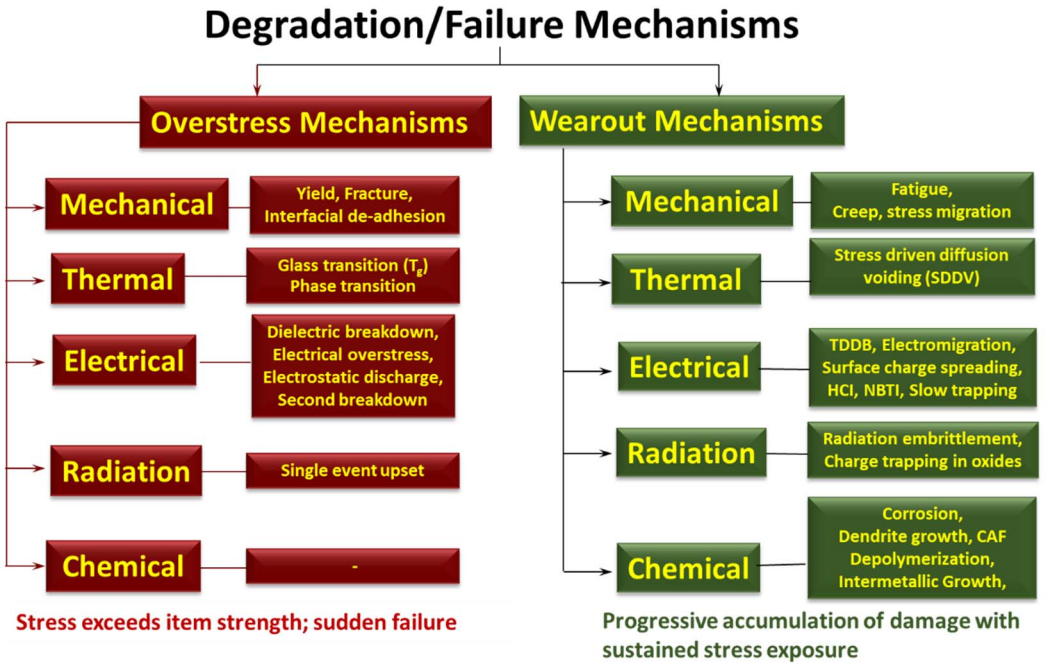


Figure 3a. Examples of dominant multi-physics degradation/failure mechanisms in electronic systems. (TDDB = Time-dependent dielectric breakdown; CAF = conductive anodic filament formation; HCI = Hot carrier injection; NBTI = Negative bias temperature instability)

In many cases, multiple stress types may interactively and synergistically contribute to accelerating a particular degradation mechanism. For example, both mechanical stress and temperature can accelerate creep in solder microbumps. Similarly, both electrical current density and temperature can accelerate electromigration in gate metallization. However, in the interest of simplifying the chart, only one dominant stress type is identified for each mechanism. Furthermore, there may be interactions between different wearout mechanisms that are not indicated here. For example, creep voiding in solder microbumps can accelerate cyclic fatigue failures. Similarly, there may be interactions between overstress and wearout degradation mechanisms that are not indicated in this simplified chart. For example, partial delaminations in die-attach materials due to overstress events can reduce their subsequent fatigue durability; and conversely, cyclic fatigue can make die attaches more vulnerable to subsequent delamination fracture under overstress events. Each of the listed degradation mechanisms represents a rich body of expert knowledge, including: quantitative models for assessing design margins and acceleration factors; model constants for many existing microelectronic material systems; and methods for quantifying the model constants for new materials. These models need to be integrated seamlessly within multi-physics co-design simulation tools so that reliability margins can truly become a concurrent design constraint along with functional criteria, in a fully integrated environment for: (i) Assessing design margins when designing for reliability (DfR); (ii) assessing the role of manufacturing defects on design margins, when manufacturing for reliability (MfR); (iii) developing acceleration factors for accelerated stress testing, when qualifying for reliability (QfR); and (iv) assessing prognostic metrics, e.g. remaining useful life (RUL), when sustaining for reliability (SfR).

In contrast, the top-down concept of data-driven approaches based on an artificial intelligence (AI) algorithmic approach for managing the reliability of complex systems is schematically illustrated in Figure 3b. This figure presents a flowchart of the process: (i) collection of system data (performance data and environmental stress data); (ii) smoothing and de-noising of the data using filtering methods; (iii) anomaly detection, using supervised and unsupervised machine learning algorithms; (iv) pattern identification with diagnostic algorithms to identify the root-cause source of the anomaly; (v) pattern extrapolation with prognostic algorithms to assess the remaining useful life (RUL); (vi) actionable responses to RUL estimates (e.g. design support decisions, self-healing actions and feedback for improving the data acquisition-analysis cycle).

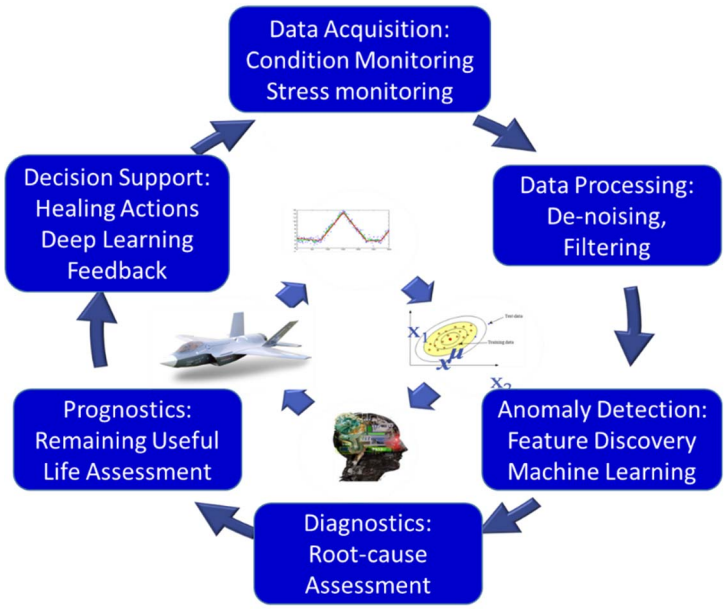


Figure 3b. Flowchart of data-driven methods for reliability assurance, using artificial intelligence (AI) algorithms.

As discussed above, the success of future hybrid reliability assurance methods will rely on judicious fusion of the RP and AI methods of Figure 3a and 3b. This fusion prognostics approach is schematically shown in Figure 3c.

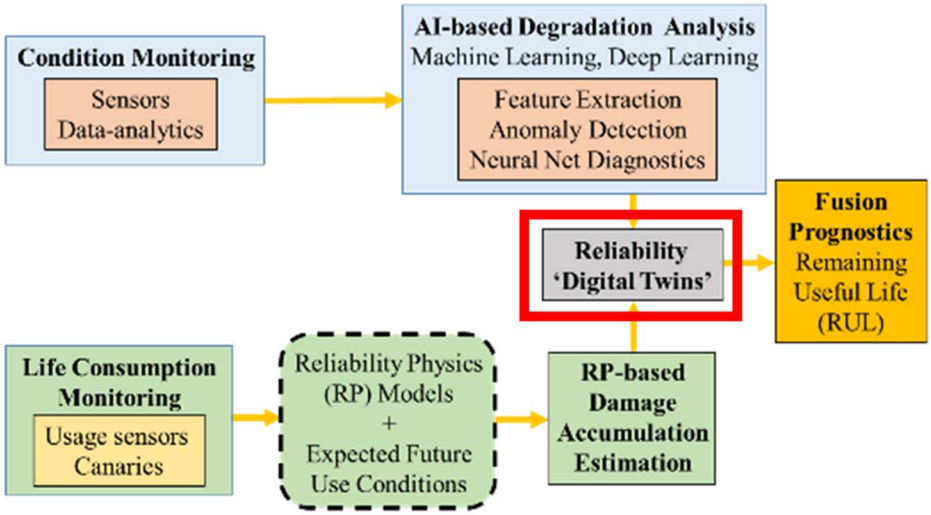


Figure 3c. Flowchart showing conceptual schematic of fusion prognostics using combinations of top-down data-driven artificial intelligence (AI) algorithms and bottom-up reliability physics (RP) models.

Making complex HI systems reliable will require a systematic and pro-active cradle-to-grave approach. Typical reliability tasks/disciplines related to quantifying and managing the stress and strength distributions are grouped for convenience under 7 headers shown in Figure 4 and listed below:

(i) Identification of customers' reliability targets for different market segments and different technology segments

(ii) Identification of life-cycle user models that include expected life-cycle environmental and operational stress profiles and understanding of system configurations

(iii) Design for reliability (DfR) tasks using reliability physics (RP), artificial intelligence (AI) methods (based on data analytics and machine learning), materials-centric approaches, co-design simulation methods and resilient, fault-tolerant design approaches

(iv) Manufacturing for reliability (MfR) using knowledge of the effect of processing conditions on material behavior; understanding of process quality, defects and yields; use of appropriate process metrology; AI-based process control; and stress screening approaches, as needed

(v) Qualification for reliability (QfR) which includes knowledge-based accelerated stress testing approaches for engineering verification testing (EVT), design verification testing (DVT) and process verification testing (PVT)

(vi) Supporting for reliability (SfR) which includes personalized in-situ prognostics and health management (PHM) for high availability and system resilience, using fusion of RP models and data driven AI models, based on: real-time detection of early anomalies and failure precursors; system diagnostics and prognostics; and dynamic adaptive healing/reconfiguration

(vii) Integration and managing of reliability best practices across the supply chain.

These are the topic areas where new difficulties and challenges are expected (and new solutions are needed) in the heterogeneous integration roadmap. These topics are discussed further in the remainder of this Chapter.

Figure 4: Activity areas for managing reliability risks

Figure 5 shows a sample flowchart of the activities necessary for developing and fielding reliable IC technologies, grouped by the reliability activity areas shown in Figure 4. The sample in Figure 5 covers the entire spectrum of tasks (grouped by the activity area) for single-chip and multi-chip IC components of HI system-in-package architectures – commencing from product concept and covering all phases such as volume production and field support. The knowledge-thread that connects these tasks for each physical product will have to be embodied in a corresponding digital twin, which will allow reliability engineers to access individualized real-time data and complete health history for each HI system. Similar charts will be presented in future editions of this chapter for developing and fielding reliable Substrate/Board Technologies and Interconnect/Assembly Technologies.

The activities shown in Figure 5 for developing and sustaining reliable HI systems involve cross-cutting activities within the HIR Team and require extensive interactions of the Reliability TWG with the remaining TWGs. The cross-TWG interactions for managing hardware reliability in the Reliability Roadmap are schematically mapped into a 2D matrix, as shown in Table 1. The vertical axis shows the various segments of the stake-holders involved in the HI roadmap (Application Domain Segments; HI Segments and Technology Segments). The horizontal axis shows the 7 main reliability activities listed above. The various cells of this 2D matrix are color-coded to show the interactions and cross-fertilization of the Reliability road-map with the different Technology Working Groups (TWGs) in the Heterogeneous Integration Roadmap (HIR) Team.

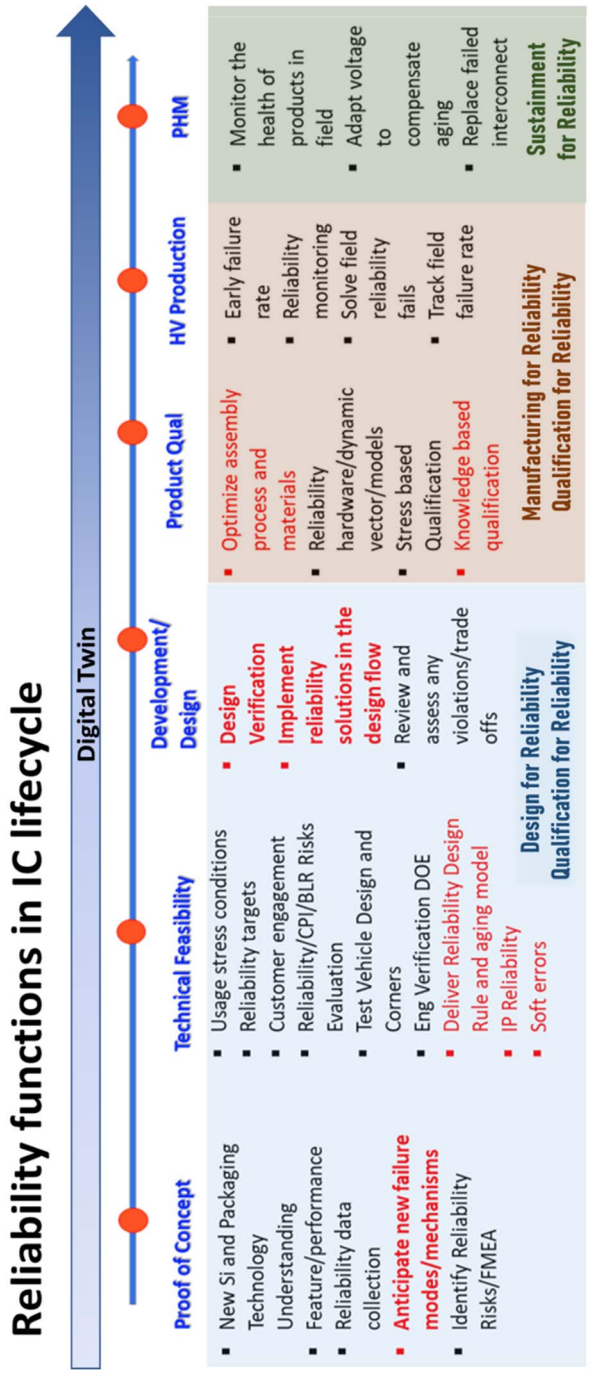


Figure 5. Sample flowchart for hardware reliability tasks for IC manufacturers

3. Reliability Assurance Activities for HI Systems

As depicted in Figure 3, reliability assurance activities require a cradle-to-grave approach, beginning with concept development and continuing on throughout the entire product development, implementation and sustainment phases of the life-cycle, until the product is retired from service. In fact, it is often argued that a cost-effective reliability management program will require a cradle-to-cradle approach, where the lessons learned from development of one generation of products should inform the development of the next-generation product. The seven activity phases described in Figure 4 are discussed in more detail below.

3.1 Reliability Targets and Life Cycle Conditions

Reliability targets for future HI systems will have to evolve in ways that enable the transformative HI Roadmaps proposed by relevant stakeholders in the application domains listed below: (i) Automotive; (ii) Aerospace and Defense; (iii) High-performance Computing and Data Centers; (iv) IoT; (v) Mobile; and (vi) Medical, Health and Wearables. The reliability activities need to be customized for the differing needs for each of these six communities. As an illustrative example, we will briefly discuss the needs of the Automotive community. In future years, this chapter will be expanded to address the special reliability needs of the remaining communities.

3.1.1 Automotive HI Systems

The unique aspects of the reliability challenges faced by the automotive community are discussed here. For example, Figure 6 (adapted from Figure 10 of the HIR Automotive Chapter, 2020) shows a comparison of several key reliability attributes across the automotive and consumer electronics communities. This data illustrates the more stringent reliability expectations in automotive applications. The requirement of 'zero' failure rates is to be interpreted within the context of health-management to mean 100% availability of repairable and reconfigurable systems, rather than a strictly 100% 'failure-free' system.

There are three key requirements in the automotive community: (i) introduction of highly complex packaging for *processors* used in autonomous driving, integration of advanced communications, and the associated challenges with ensuring higher levels of reliability in all components based on new use cases for automobiles and general transportation going forward; (ii) Numerous advances expected in *sensor technologies* with advancements of Radar, LIDAR, and other sensing techniques; and (iii) Integration of *power systems* as cars continue to electrify. Artificial Intelligence (AI) and Machine Learning (ML) will be central to both the

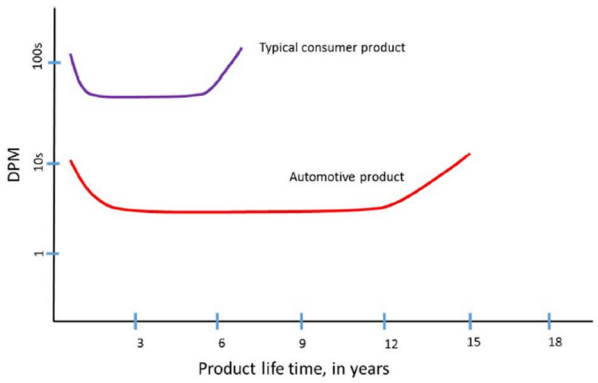
Table 1. Cross-TWG Interactions of Reliability TWG

		Reliability Targets	Life Cycle Conditions	Design for Reliability				Manufacturing for Reliability				KBT[4] for Reliability Qualification: EV/DV/PV[6]						PHM[5]		Supply Chain	Life Cycle Economics
		Identification of customer goals	Environmental & operational conditions	Reliability Physics (RP)	Materials characterization for Reliability	RP/AI[2]-based co-design rules & standards	RP/AI-based co-design methods and tools	Effect of process on material properties	Defects (from RP perspective)	Process metrology & sensors	Process control & yield (AI and feed-forward)	Stress screens & NDI[3]	RP-based acceleration models	Test methods (test structures, sensors, metrology)	RP/AI-based margin testing	RP-AI-based accelerated stress testing	Failure analysis methods	Test standards and guidelines	RP/AI-based Fusion prognostics	PHM Standards and guidelines	Reliability across supply chain	Managing risk-cost tradeoffs
Applications	Mobile	Mobile	Mobile	Mobile	Mobile	Mobile	Mobile	Mobile	Mobile	Mobile	Mobile	Mobile	Mobile	Mobile	Mobile	Mobile	Mobile	Mobile	Mobile	Mobile	Supply Chain	No TWGs ??
	Internet of Things	IoT[20]	IoT	IoT	IoT	IoT	IoT	IoT	IoT	IoT	IoT	IoT	IoT	IoT	IoT	IoT	IoT	IoT	IoT	IoT		
	Medical, Health and wearables	MHW[16]	MHW	MHW	MHW	MHW	MHW	MHW	MHW	MHW	MHW	MHW	MHW	MHW	MHW	MHW	MHW	MHW	MHW	MHW		
	Automotive	Automotive	Automotive	Automotive	Automotive	Automotive	Automotive	Automotive	Automotive	Automotive	Automotive	Automotive	Automotive	Automotive	Automotive	Automotive	Automotive	Automotive	Automotive	Automotive		
	HPC[11] & Data Centers	HPC[11]	HPC	HPC	HPC	HPC	HPC	HPC	HPC	HPC	HPC	HPC	HPC	HPC	HPC	HPC	HPC	HPC	HPC	HPC		
	Aerospace and Defense	Aerospace	Aerospace	Aerospace	Aerospace	Aerospace	Aerospace	Aerospace	Aerospace	Aerospace	Aerospace	Aerospace	Aerospace	Aerospace	Aerospace	Aerospace	Aerospace	Aerospace	Aerospace	Aerospace		
Package Integration	WLP (FO/Fi)[12]	WLP	WLP	WLP	WLP	WLP	WLP	WLP, Test	WLP, Test	WLP, Test	WLP, Test	WLP, Test	WLP, Test	WLP, Test	WLP, Test	WLP, Test	WLP, Test	WLP, Test	WLP; 2.5/3D;SCMCI; Interconnects;SIP; Photonics; MEMS/Sensors; Power; RF/Analog; Security	WLP; 2.5/3D;SCMCI; Interconnects;SIP; Photonics; MEMS/Sensors; Power; RF/Analog; Security		
	2.5D and 3D integration	2.5/3D	2.5/3D	2.5/3D	2.5/3D	2.5/3D	2.5/3D	2.5D and 3D integration, Test	2.5D and 3D integration, Test	2.5D and 3D integration, Test	2.5D and 3D integration, Test	2.5D and 3D integration, Test	2.5D and 3D integration, Test	2.5D and 3D integration, Test	2.5D and 3D integration, Test	2.5D and 3D integration, Test	2.5D and 3D integration, Test	2.5D and 3D integration, Test	2.5D and 3D integration, Test	2.5D and 3D integration, Test		
	Wafer Singulation and Thinning	SCMCI[13]	SCMCI	SCMCI	SCMCI	SCMCI	SCMCI	SCMCI, Test	SCMCI, Test	SCMCI, Test	SCMCI, Test	SCMCI, Test	SCMCI, Test	SCMCI, Test	SCMCI, Test	SCMCI, Test	SCMCI, Test	SCMCI, Test	SCMCI, Test	SCMCI, Test		
	Chip-package interactions (CPI)																					
	Interconnects (TSVs, µbumps, wirebonds, Flip Chip joints)	Interconnects	Interconnects	Interconnects	Interconnects	Interconnects	Interconnects	Interconnects, Test	Interconnects, Test	Interconnects, Test	Interconnects, Test	Interconnects, Test	Interconnects, Test	Interconnects, Test	Interconnects, Test	Interconnects, Test	Interconnects, Test	Interconnects, Test	Interconnects, Test	Interconnects, Test		
	Substrates/Interposers	SCMCI	SCMCI	SCMCI	SCMCI	SCMCI	SCMCI	SCMCI; Test	SCMCI; Test	SCMCI; Test	SCMCI; Test	SCMCI; Test	SCMCI; Test	SCMCI; Test	SCMCI; Test	SCMCI; Test	SCMCI; Test	SCMCI; Test	SCMCI; Test	SCMCI; Test		
	Board Assembly	SCMCI	SCMCI	SCMCI	SCMCI	SCMCI	SCMCI	SCMCI; Test	SCMCI; Test	SCMCI; Test	SCMCI; Test	SCMCI; Test	SCMCI; Test	SCMCI; Test	SCMCI; Test	SCMCI; Test	SCMCI; Test	SCMCI; Test	SCMCI; Test	SCMCI; Test		
	SOC/SiP/SOP[3] formats	SiP	SiP	SiP	SiP	SiP	SiP	SiP; Test	SiP; Test	SiP; Test	SiP; Test	SiP; Test	SiP; Test	SiP; Test	SiP; Test	SiP; Test	SiP; Test	SiP; Test	SiP; Test	SiP; Test		
Technologies	Microelectronics > 5 nm	SCMCI	SCMCI	SCMCI	SCMCI	SCMCI	SCMCI	SCMCI	SCMCI	SCMCI	SCMCI	SCMCI	SCMCI	SCMCI	SCMCI	SCMCI	SCMCI	SCMCI	SCMCI	SCMCI		
	Microelectronics < 5 nm																					
	Photonics & optics	Photonics	Photonics	Photonics	Photonics	Photonics	Photonics	Photonics	Photonics	Photonics	Photonics	Photonics	Photonics	Photonics	Photonics	Photonics	Photonics	Photonics	Photonics	Photonics		
	MEMS and sensors	MEMS[14]/Sensor	MEMS[14]/Sensor	MEMS[14]/Sensor	MEMS[14]/Sensor	MEMS[14]/Sensor	MEMS[14]/Sensor	MEMS/Sensor	MEMS/Sensor	MEMS/Sensor	MEMS/Sensor	MEMS/Sensor	MEMS/Sensor	MEMS/Sensor	MEMS/Sensor	MEMS/Sensor	MEMS/Sensor	MEMS/Sensor	MEMS/Sensor	MEMS/Sensor		
	Power electronics	Power	Power	Power	Power	Power	Power	Power	Power	Power	Power	Power	Power	Power	Power	Power	Power	Power	Power	Power		
	Energy souces (Batteries/PV/FC)																					
	RF/Analog Devices	RF[15]/Analog	RF/Analog	RF[15]/Analog	RF[15]/Analog	RF[15]/Analog	RF[15]/Analog	RF/Analog	RF/Analog	RF/Analog	RF/Analog	RF/Analog	RF/Analog	RF/Analog	RF/Analog	RF/Analog	RF/Analog	RF/Analog	RF/Analog	RF/Analog		

Digital Twin

	Consumer	Automotive
Ambient temperature range	0 to 85 °C	-30 to 150 °C
Expected Operating Life	2-3 years	>10 years
Acceptable Failure Rates	300 ppm	'ZERO' (!!)
Supply Lifetime	2-3 years	15-20 years

Figure 6. Key reliability attributes showing the severity of the automotive life-cycle, compared to consumer products (from HIR Automotive Chapter, 2020).



functionality and safety of the automobile, as well as in techniques used for advancing reliability of the electronic components. These three technology streams are needed for achieving four major trends of the automotive community:

- **Drive Electrification**: New power electronics technologies, utilizing WBG compound semiconductors (e.g. SiC or GaN) and silver sintering bonding will allow higher operational temperatures (200°C and above), thus reducing weight, complexity and cost of cooling subsystems. However, new high-temperature packaging materials are needed. In addition, sensors and microelectronic components will increase the heterogeneity and complexity. Assuring reliability, while reducing time-to-market, will require new break-through approaches
- **Autonomous vehicles** are expected to increase safety and improve traffic flows, thus leading to reduction in overall emissions, especially when using electrical powertrains. Utilization is expected to therefore significantly increase (including the charging time for the HV/EV), leading to longer duty cycles and higher reliability expectations, especially for the safety-critical sub-systems.
- **Connectivity** will introduce commercial components to harsh environments. For example, the functionality and performance of advanced packaging solutions, such as SiPs based on advanced semiconductor node technology, will be needed soon in 15-year automotive life-cycles. Hence, connectivity will increase the operational time of IC packages and ECUs used in automotive (e.g. software upgrade, dynamic updates and interactions with the cloud during parking, using WLAN instead of expensive GSM connections).
- **Smart mobility (and associated changes in business models)** are expected to lead to sharing services. Instead of being the owner of a car, we will simply rely on a mobility service provider. The end 'owners' for reliability considerations will no longer be individual owners,\; instead they will be fleet owners. Fleet owners will try to customize cars they offer for different applications (e.g. short urban business commutes vs recreational long-term use). Fleet owners will therefore look for customized reliability and availability solutions for different customer segments.

Examples of the milestones presented in the HIR Automotive Chapter are discussed next. The dominant degradation/failure modes and mechanisms for these technology milestones are discussed later in this Chapter.

(i) Processor roadmaps for automotive applications are based on advances in Si nodes, increased graphic and memory bandwidth, optical I/O and increased processor power, using a combination of 2.5/3D assemblies, as shown in Figure 7 (Figure 4 from HIR Automotive Chapter).

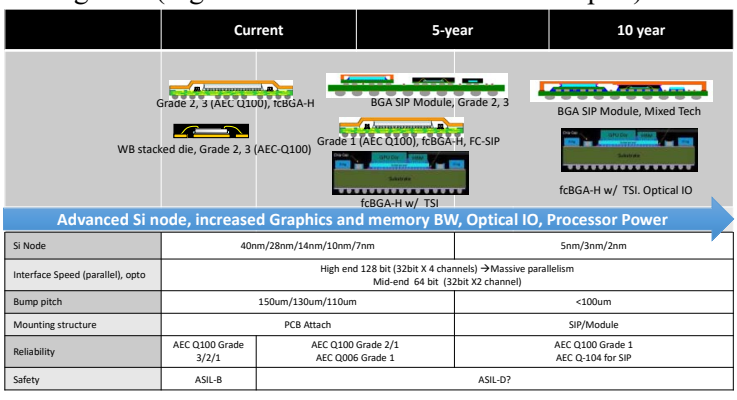


Figure 7. Automotive processor roadmap (Figure 4 from HIR Automotive Chapter, 2020)

Sensor Objective	Camera	RADAR	LiDAR	Ultrasound
Adaptive Cruise Control		X	X	X
Emergency Braking	X	X	X	X
Pedestrian Detection	X	X	X	X
Collision Avoidance		X	X	X
Traffic Sign Recognition	X			
Lane Departure Warning	X		X	
Cross Traffic Alert	X	X	X	
Surround View	X			
Blind Spot Detection	X	X	X	
Park Assist	X	X	X	X
Rear Collision Warning	X	X	X	X
Rear View Mirror	X			
Drowsiness Detection	X			

Figure 8: Automotive sensor technology matrix (Table 1 from HIR Automotive Chapter, 2020)

(ii) Multimodal sensor systems required in autonomous automotive platforms include high-resolution fast digital cameras, high bandwidth RADAR, LiDAR, and Ultrasound, as shown in Figure 8 (Table 1 from HIR Automotive Chapter, 2020). Heterogenous integration will require co-packaging, into the same system, of one or more of these technologies, depending on the automation level. The automotive community categorizes drive automation in 6 levels – No automation (Level 0) to Full automation (Level 5). System complexity is expected to progressively increase as drive automation progresses to Level 5 in future vehicles. Reliable performance will be critical, especially since some of these sensors are categorized as safety-critical. Reliability physics of advanced sensor technologies will be key to assuring safe operation.

For example, RADAR modules will have to be pushed to near-140 GHz speeds to achieve the bandwidths needed for internet ubiquity, sensor fusion, compute power advances, mobility, and data analytics. Device-level challenges will include reliability physics of Si-Ge MMIC and RF-CMOS semiconductor nodes, as well as older nodes based on more classical GaAs technologies. Package integration will require novel antenna-in-package solutions that will be able to survive the harsh automotive life-cycles described in Figure 6 above. The automotive RADAR roadmap is shown in Figure 9 (Figure 23 from Automotive Chapter in HIR roadmap, 2020).

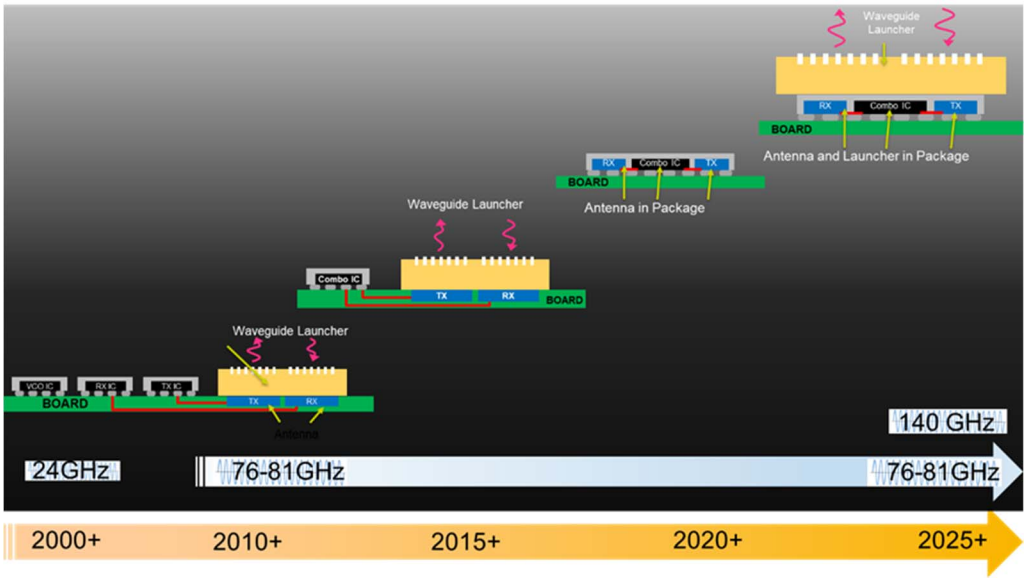


Figure 9. RF module roadmap (Figure 23 in HIR Automotive Chapter, 2020)

Packaging Architecture	Current	5-Year	10-year	15-year
LiDAR Module/SiP	LiDAR SiP Stacked die, FBGA, AEC Grade 1, 2		LiDAR Integrated Sensor, AEC Grade 0	LiDAR Integrated Sensor, AEC Grade 0, High Density Si Interconnect
LiDAR Detection Range : Short Range (100m) to Long Range (100-250m)				
Package	Detector: C2W, bumped, FC, W/B ASIC: W/B, F/C Package: LFBGA, QFN, LGA, SiP	Detector: FC, PoP, W/B ASIC: W/B, F/C Package: LFBGA, QFN, LGA , MLP, WLCSP		Detector: FC ASIC: FC Package: WLCSP, FO WLP
Detector/ASIC per pkg Footprint	1 Detector / 1 to 3 ASIC 10x10mm	1 Detector / 1 to 2 ASIC 9x9mm	2-4 Detector/ 3 to 4 ASIC 8x8mm	>4 Dectector/ASIC
Substrate	Laminate, Leaded, Ceramic	Laminate or Ceramic	Laminate or Ceramic	Laminate w/high density Interposer
Optical Grade Window or Filter	Filter, Glass, or Plastic	Filter, Glass, or Plastic	Filter, Glass, or Plastic	Filter, Glass, or Plastic
Ball Pitch	0.8mm	0.7mm	<0.7mm	<0.7mm
Reliability	AEC Q100 Grade 1, 2	AEC Q100 Grade 0		>AEC Q100 Grade

Figure 10. LiDAR detector roadmap (Figure 25 in HIR Automotive Chapter, 2020)

As another example of new reliability challenges, LiDAR detector sensor modules for automotive environments will require reliable integration for performance at distances up to 250 m. This will require integration of high-power LED WBG compound semiconductors (GaN) with MEMS, optical phase arrays and ASICs, using 2.5D high-density organic interposer technologies based on area-array interconnection technologies below 700 µm pitch. Reliability physics of high-power WBG devices, as well as of photonic devices and interconnects, will be key to adoption of advanced LiDAR technologies. The LiDAR roadmap is shown in Figure 10 (Figure 25, of HIR Automotive Chapter,

2020). Similar advances are needed in reliable ultrasonic sensors and in over-sampled multi-modal sensor-fusion technologies to achieve the requisite levels of reliability, resilience and availability.

The automotive community understands that developing and supporting reliable HI systems using advanced technologies will require a phased approach. Systems will use technologies of varying maturity. The mature nodes will be relatively easier to qualify for automotive environments, while the advanced semiconductor nodes (with corresponding advanced SiP technology nodes) will require more work and time. Figure 11 (Figure 9 of HIR Automotive Chapter, 2020) has been provided by the automotive TWG to articulate this phased approach to reliability, using AEC's 4-level reliability maturity scale - least reliable (Grade 3) to most reliable (Grade 0).

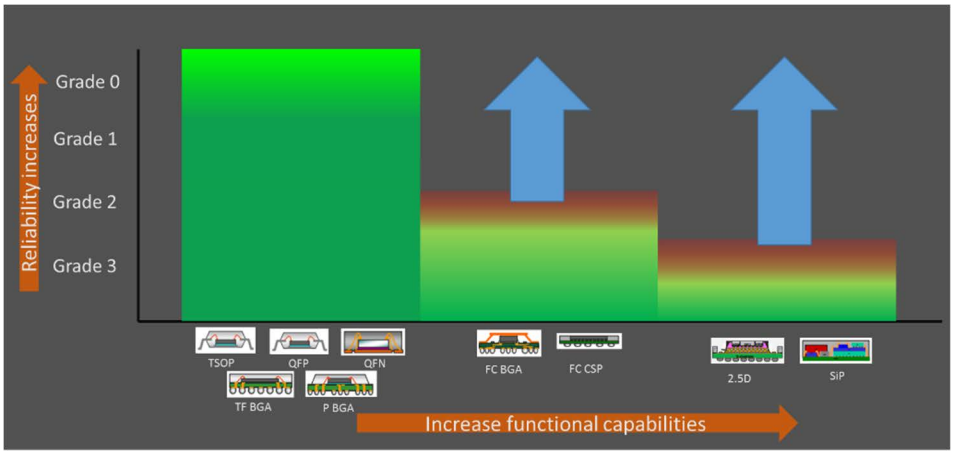


Figure 11. Achieving desired reliability levels requires a phased approach, with advanced nodes and packages requiring longer cycle-time (Figure 9 of HIR Automotive Chapter, 2020)

To achieve sufficient life-cycle reliability and availability, the automotive community intends to adopt a real-time prognostics and health management (PHM) approach that will have to rely on fusion of data-driven machine learning approaches in conjunction with reliability-physics based approaches, by leveraging a digital twin ecosystem. As illustrated in Figure 12 (Figure 30 of HIR Automotive Chapter, 2020), the approach envisions implementation of real-time (i) condition monitoring, (ii) stress sensing, (iii) anomaly detection and classification, (iv) fault diagnostics, and (iv) prognostics for continuous assessment of remaining useful life (RUL).

The automotive community has grouped the top 10 challenges expected over the next 15 years into the following broad topic areas: (i) New materials; (ii) Infotainment and Advanced Driver Assistance Systems (ADAS); (iii) Processor/memory integration; (iv) Thermal requirements and ambient conditions; (v) Qualification requirements, especially safety for ADAS; (vi) Sensors; (vii) Cost-effective packaging; (viii) Performance requirements; (ix) Electric and Hybrid Electric Vehicle (E/HEV) segment; and (x) Highly efficient power packaging (the 2020 edition of the automotive HIR roadmap does not contain much detail on this topic, so this is deferred to a future edition of the Reliability Chapter).

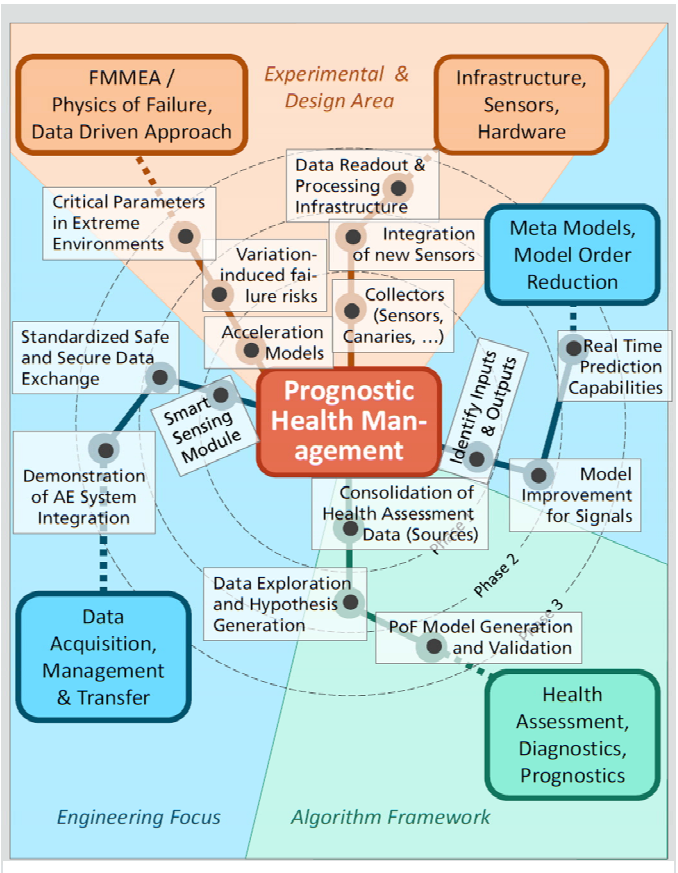


Figure 12: PHM Methodology (Figure 30 of HIR Automotive Chapter, 2020)

3.1.2 Other Application Domains:

There are 5 other major application domains, all with some common shared reliability concerns as well as some unique and special reliability concerns based on different product classes, different life-cycle conditions and different

reliability targets. These stakeholder communities include: (i) Aerospace and Defense; (ii) High Performance Computing (HPC) and Data Centers; (iii) Medical, Health and Wearables (MHW); (iv) Internet of Things (IoT); and (v) Mobile products. The needs of the remaining communities will be addressed in future editions of this chapter.

3.2 Design for Reliability (DfR)

It is well understood that reliability has to be built into a product right from the early stages of concept design, and cannot be retro-fitted into a product after the design and manufacturing processes have been finalized. This will become even more important as the system complexity systematically increases in HI systems. Reliability will have to become one of the key requirements and be specified right from the beginning in a simulation-assisted co-design environment that will have to heavily leverage digital twin ecosystems. DfR activities in this TWG will have to be closely synchronized with those in the Modeling and Simulation and Codesign TWGs. Extensive simulation infrastructure, design tools, design standards and trained design teams are necessary to realize the full benefits envisioned in the chiplet-based approach being explored for highly diverse HI systems.

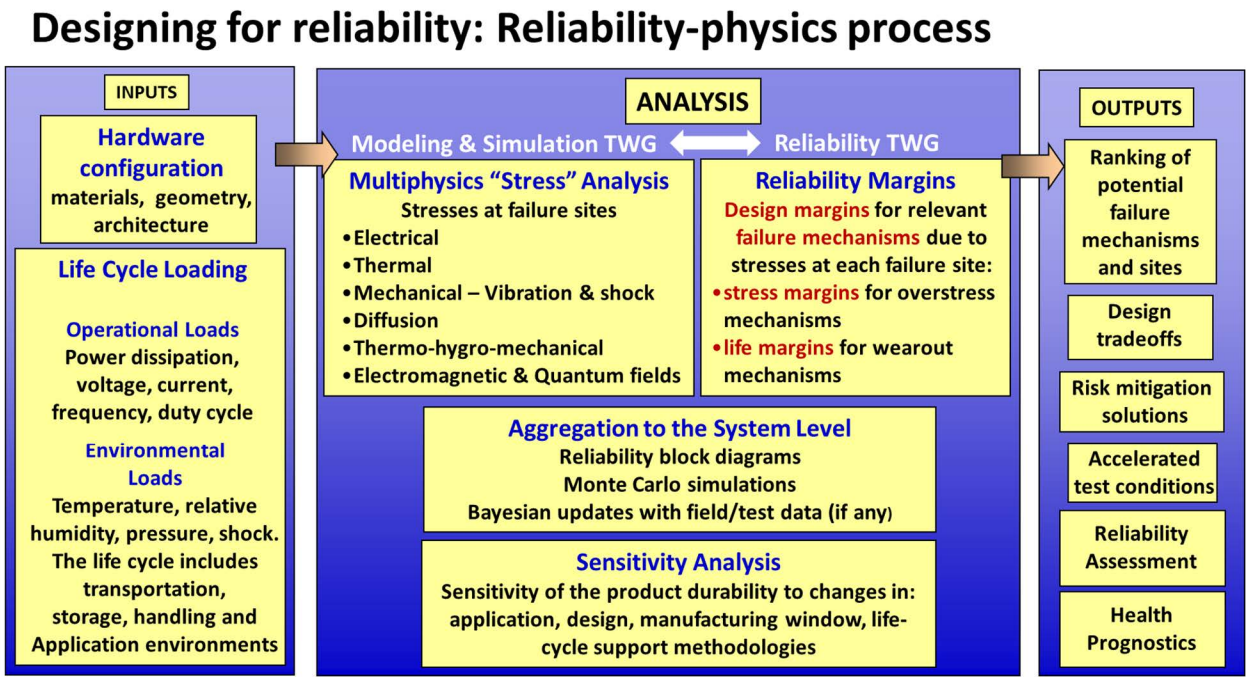


Figure 13. Flowchart for Design for Reliability (DfR).

Figure 13 shows a schematic flowchart of such a DfR environment where multi-physics, multiscale stress modeling and reliability modeling must co-exist and collaborate in order to enable effective codesign for reliability. Some modeling approaches will have to rely on reliability physics approaches while other modeling approaches will have to be developed using top-down machine learning approaches. The reliability models will have to address the dominant degradation, aging and failure mechanisms in ever-evolving HI systems (discussed earlier in Figure 3a) and will utilize the stresses estimated via the multi-physics and multiscale analysis discussed in the Modeling and Simulation chapter. Some of the major reliability concerns expected in HI systems are discussed in the remainder of this section.

3.2.1 Multiphysics Interactions in HI packages

Complex electro-thermo-mechanical mutual interactions arise due to chip package (CPI) interactions, as well as due to Chip-Board-Package (CBPI) interactions. Any failure modes due to such mutual interactions are usually broadly categorized as CPI and CBPI reliability failures. The failure occurs at the weakest link when the chip is assembled into a package. As indicated in Figure 14 (and discussed earlier in Figure 1), risk of degradation and failure arises when the 'stress' exceeds 'strength'. As discussed before, both 'stress' and 'strength' have 'intrinsic' stochastic distributions and any deviations due to anomalous variabilities are termed 'extrinsic.' The extrinsic regions can clearly exacerbate the overlap between the two distributions and thereby increasing the probability of 'stress' exceeding 'strength,' and increasing the CPI failure rate. Four different major CPI failure mode categories are

summarized below. These include the effect of stresses on: chip failures, package failures, transistor performance shift, and three-way chip-package-board interactions.

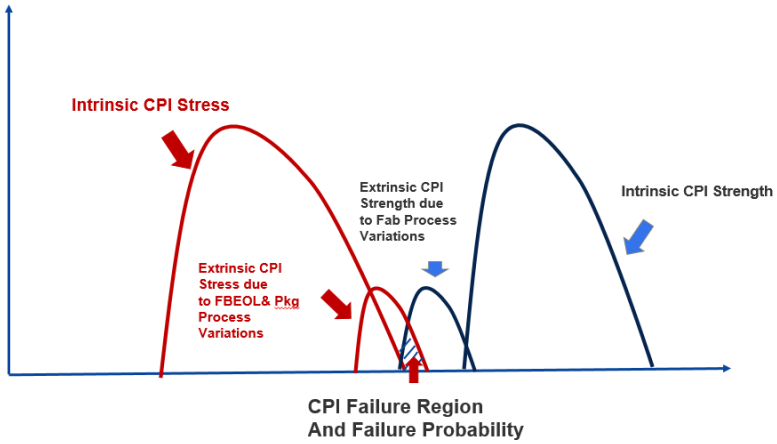


Figure 14. 'Intrinsic' and 'extrinsic' CPI 'stress' and 'strength' distributions

3.2.1.1. Chip failures due to thermal mechanical stresses

Chips are vulnerable to both global and local sources of thermo-mechanical stresses. Global stresses arise from overall thermal expansion mismatches between the chip and the surrounding package. Local stresses arise from gradients of temperature due to self-heating effects in complex 3D transistor architectures, such as FinFET and Gate All Around (GAA) devices. Both effects are discussed below.

a. **Global stress due to CTE mismatch between chip and package:** When the chip is weaker than the package, e.g. due to extremely low-k (ELK) dielectric, then the CPI failure occurs at the chip level. For flip-chip packages, such stress is transmitted from package to chip, and the bump, under bump metallization (UBM), back-end-of-line (BEOL) interconnect and low-k dielectric end up carrying most of the stress. The front-end-of-line (FEOL) transistors are less affected.

- Chip corner/edge cracking
- Under bump or wire bond pad cratering in low-k dielectric
- UBM cracking
- Die backside cracking

Figure 15 shows examples of typical failure modes in this category.

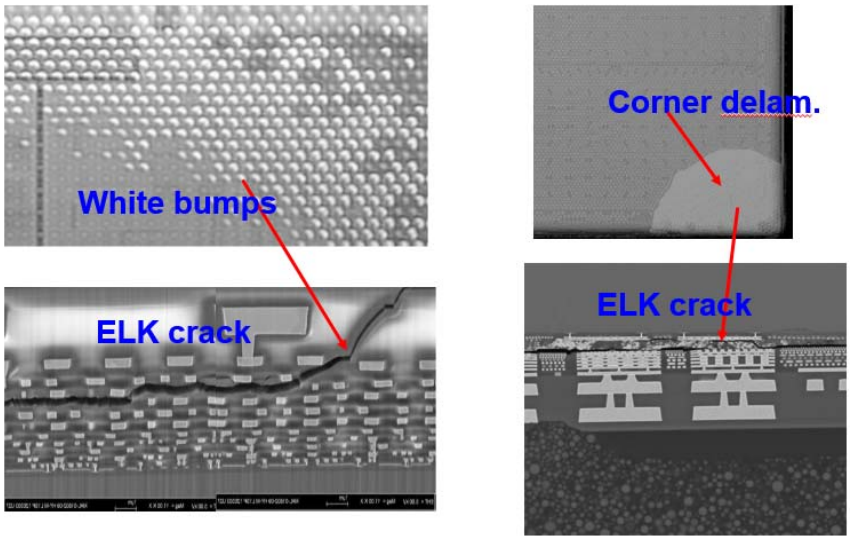


Figure 15. Typical CPI induced chip failure modes [Source: X. Zhang, UT Austin]

b. **Local stress due to FinFET Self Heating Effects (SHE):** SHE is known to generate a localized temperature concentration, and the temperature varies with circuit operation. This creates a localized thermal cycling stress profile on top of the global thermal profile. Such a localized thermal profile may cause BEOL interconnect failures. FinFET geometry exacerbates this problem and the problem is expected to become more severs as future

technology nodes migrate to gate all around (GAA) architectures. These thermo-mechanical stress gradients are generated at the transistor level, so the transistor structures and the bottom layers of the BEOL interconnects end up carrying most of the stress. This results in performance shifts and wearout aging/degradation modes of transistors, particularly Hot Carrier Injection (HCI), BEOL stress and electromigration (EM), and bottom layer Cu/ELK cracking. When the SHE is severe enough, it can also burn out the channel. Some of these issues are discussed further below. In particular, SHE impact is further discussed later in Section 3.2.3.

3.2.1.2. Package failures due to thermal mechanical stress

When the chip is stronger than the package, then the package experiences CPI failure modes, such as:

- Underfill cracking/delamination
- Solder mask cracking/delamination
- Substrate failures
- Bump cracking near substrate

3.2.1.3. Stress induced transistor performance shift

Si is a piezo-electric material and the stress in Si changes the carrier mobility for both NMOS and PMOS transistors. The theory is well established, and a well-controlled mechanical straining technique has been exploited to enhance Si transistor performance since the introduction of the 90-nm process node. However, unexpected/uncontrolled stresses from CPI can also cause a negative effect on transistor performance. The following are examples of potential stresses that can have a significant effect on transistor performance (further SHE discussion is included later in this Section).

- Local stress in stacked die caused by Through-Silicon-Vias (TSVs): TSVs, particularly large diameter vias, generate high stress concentration in Si and directly affect the adjacent circuitry on the die. As an example, Figure 16 shows the TSV stress effect on adjacent transistors.
- Overall package-induced global stress on a thin-die wirebonded package: A thinner die has a higher stress than a thicker die. In a wirebonded and wafer-level package, the global stress is directly transmitted to the die.
- Local stress transmitted by bump and µ-bump: The stresses from interconnect bumps are generally absorbed by the BEOL interconnects if there are enough metal layers. Otherwise, the stress can affect the FEOL transistors.

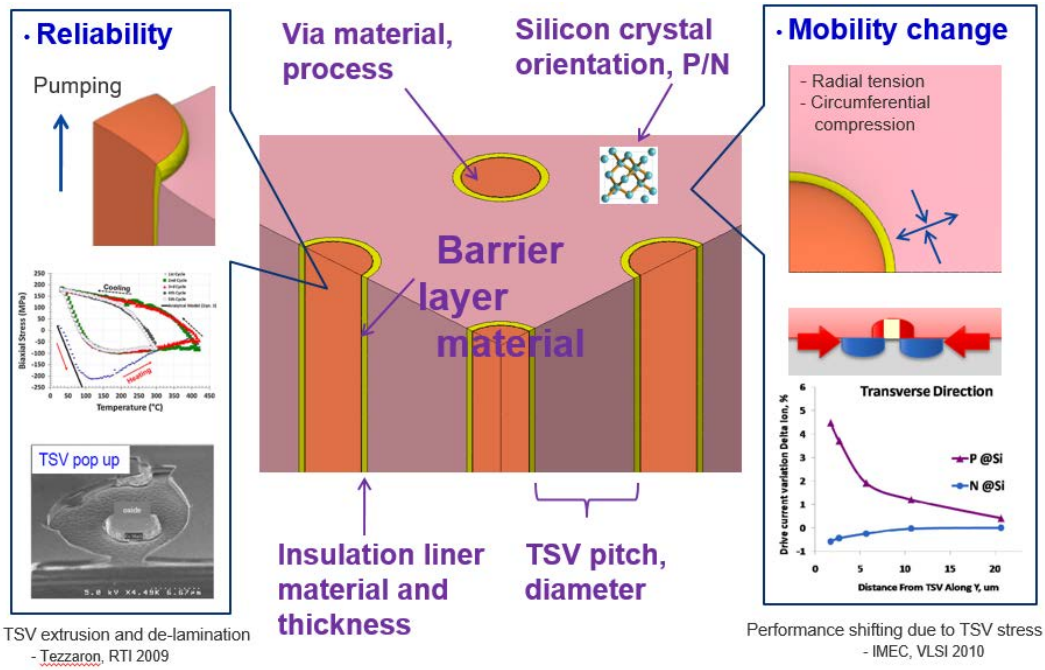


Figure 16. TSV-induced stress effect on adjacent transistors [Source: A. Karmarkar, IEEE TDMR, 2019]

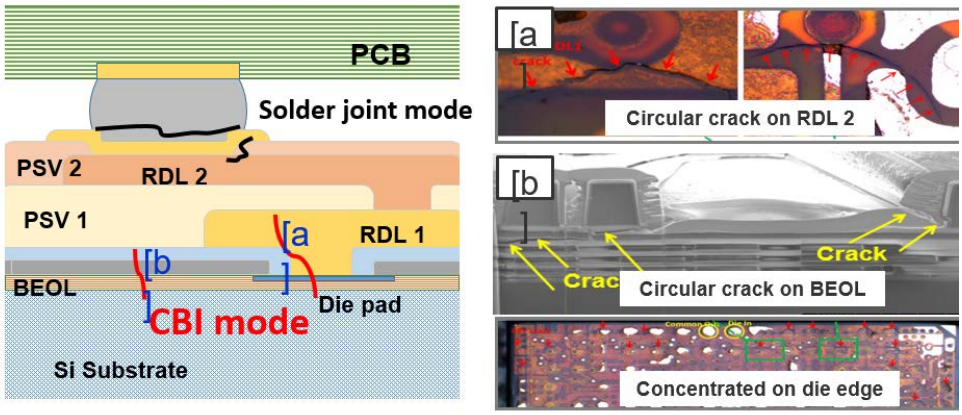


Figure 17. Typical FOWLP CBPI failure modes [Source: Meditek, IRPS, 2017]

3.2.1.4. Chip to Board to Package Interaction (CBPI)

When a package is surface-mounted on a PCB, the board level stresses such as thermal-mechanical stress due to CTE mismatch and shock/vibration stress are absorbed by BGA solder balls, the package substrate or flexible leads. For example, the following package styles are found to be particularly vulnerable to CBPI failures, and the board-level stress can cause additional failures to the package and even to the chip.

- Wafer Level Chip Scale Package (CSP): Die edge cracking after surface mounting
- Fan Out Wafer Level Package (FOWLP): RDL layer cracking
- Large Flip Chip Ball Grid Array (FCBGA) with thin core or coreless substrate: Large size FCBGA packages can experience significant warpage during surface mount assembly. When it is mounted on a rigid PCB, the stress redistributes in the package and a stress concentration may cause underfill cracking/delamination or even chip failures.

Figure 17 shows some typical CBPI failure modes in a FOWLP, e.g. ELK cracking; circular cracks near die-edge in passivation (PSV) layers, redistribution layer (RDL) and BEOL interconnects; initial crack in inner interconnect.

3.2.2 Summary of Degradation/Failure modes expected in HI packages

The sample interactions and resulting degradation modes discussed above need to be categorized and summarized so the dominant mechanisms can be identified based on the technology roadmaps and life-cycle expectation of the six different HIR application segments.

In traditional microelectronic devices, the dominant degradation modes were mostly caused by electrical stresses. However, in diverse multichiplet-based HI architectures, there are additional dominant degradation mechanisms in the BEOL/interconnect architectures. Table 2a provides a listing of these degradation modes while Table 2b provides a grouping based on the dominant source of the stresses that accelerate these modes.

A more general table of possible degradation modes for the entire HI system is presented in Table 3. This table is grouped to highlight the multiscale and multiphysics grouping of the degradation modes. The vertical axis depicts the multiscale grouping at different integration levels (device, interconnects, package, module). The horizontal axis depicts the multiphysics grouping (electrical, moisture, thermal, mechanical and combined degradation modes and their respective stress drivers). The last column on the horizontal axis is dedicated to discussion of the current state and future needs for information flow mechanisms (e.g. PDKs and ADKs) that are needed to enable co-design for reliability. Information flow includes synergies with the Modeling and Simulation TWG to develop the DfR and MfR ecosystems. This matrix of degradation modes will need to be customized in the future for the six different HIR application segments, based on the dominant degradation modes expected for their respective technology roadmaps, life-cycle conditions and reliability goals.

Table 2a. Interconnect/BEOL degradation modes in HI architectures

Solder reliability	• UBM consumption (IMC formation) over time
	• IMC growth (different phases): R change over time
	• Kirkendall voids
	• Brittle IMC: fracture
	• Solder bridging
	• EM
	• Corrosion?
	• CPI: Induces local stress in BEOL (ELK cracks, delamination, SIV)
	• CPI: Induces local stresses in FEOL devices (finfet, HBT, memory,…): change in device characteristics
Hybrid bonding	• Voids near Cu pads
	• Opens/ shorts
	• Cu migration, pumping (creep) (maybe only a processing issue?)
	• CPI: Delamination/fracture
	• Particles: -> voids
TSV reliability (Cu filled)	• W filled?
	• Liner BD
	• Voids? (issue? might affect EM)
	• EM
	• Shorts and opens: more process related than reliability?
	• Cu diffusion
	• Impact on local stress in BEOL due to CPI: SIV, ELK
	• Impact on devices due to CPI: finfets, HBT, memory,…

Table 2b. Stress sources for interconnect/BEOL degradation modes in HI architectures and difficult challenges in addressing them

CPI	• Local stress induced by solder, TSV, Cu pillar (see also above)-> impact on ○ BEOL (SIV, fracture, delam) ○ Devices (finfets, memory, HBT,...)
	• Chip thinning + backside processing: stress + local warpage
	• Global stress induced by stacking thinned chips, packaging, wafer level:
	○ Delamination
	○ chip cracking
	○ impact on devices
	○ Bow: peeling stresses: delamination, cracks
Thermal	• Increased local T (stacked chips, difficult to cool):
	○ increases many (most) reliability issues
	○ Power cycling effects are enhanced: local issues, fatigue, crack growth, EM
	• Thinned Si chips: Thermal properties BEOL become dominating factor
Important related effects:	• KGD: needs in-line wafer level test during processing
	• Failure analysis: Becomes increasingly challenging. Stacked chips, back-side processing, FOWLP, stacked IC: very limited (to no) optical access: PEM, LVP become impossible.
	• Increased need for cooling

Table 3: Degradation Modes/Mechanisms expected in current and future HI systems

Multi Scale and Multi Physics Reliability Failure Modes and Design Simulations, *by Richard Rao*													
Scale of Integration	**Multi Scale and Multi Physics**	**Electrical Stress**		**Moisture**		**Thermal Mechanical Stress**		**Mechanical Stress**		**Simulation/Modeling and Co-Design Flows**		
		Failure Modes	**Failure Mechanism & Reliability Models**	**Failure Modes**	**Failure Mechanism & Reliability Models**	**Failure Modes**	**Failure Mechanism and Reliability Models**	**Failure Modes**	**Failure Mechanism & Reliability Models**	**Failure Modes**	**EDA Flows**	**PDK/ADK**
Transistor	FinFET/GAA IGBT/WBG/SOI device failures	1. FinFET/GAA NBTI/PBTI 2. Hot Carrier Injection 3. Gate Dielectric Breakdown 4. ESD	1. BTI Models with recovery effect 2. HCI Model 3. TDDB Weibull model 4. Oxide and junction breakdown	No known failures	None	1. Self Heating Effect induced localized stress in FinFET channel and in GAA 2. uBump/C4 bump/TSV and package/system level stress transmission to FinFET. 3. Channel stress alter FinFET/GAA characteristics	1. FinFET/GAA SHE Model a. Steady Model b. Transient Model c. Model with heatsink effect 2. e-CPI Model 3. Piezo-electrical models	No known failures	None	1. Transistor aging induced circuit degradation; 2.How the thermal and stress effects be considered in circuit aging simulation? 3. How does the process variation interact with aging for 6nm/7nm? How should this interaction been simulated?	1. Cadence Relxpert 2. Mentor Graphics 3.	1. Device SPICE Model 2. Device aging model 3. SHE model 4. TDDB model
Inter-connects	MEOL/BEOL Metal/Via /ELK	1. Electromigration 2. Inter Layer Dielectric ELK Breakdown 3. MEOL Oxide Breakdown 4. EOS	1. Pad and underline metal corrosion 2. Cu/ELK delamination	1. Electrochemical corrosion 2. Interface degradation due to moisture absorption	1. Stress Migration 2. Joule/SHE effects on the stress in Cu/ELK; 3. uBump/TSV/RDL and package/system level stress transmission to MEOL/BEOL. 4. Cu metal line fatigue	1. Creep induced voiding 2. CTE mismatch 3. CTE mismatch 4. SHE induced localized thermal cycling	No known failures	None	CPI induced Cu/ELK cracking - how will the internal stress due to JHE/SHE and external stresses from bumps/TSV/RDL/ Packaging affect the failure of Cu/ELK over time?	1. Ansys/Mentor	
	FBEOL RDL/ Dielectric	1. RDL Electromigration				1. RDL cracking	ubumps/TSV/Package/Board effects on RDL stress			CPI or CBPI induced RDL cracking/delamination - how will the stress from bumps/ TSV/Package/board level stresse affect RDL failure?	EM- How does the temp and stress affect RDL EM?	
	Au/Cu Wirebonding	1. Electromigration		1. IMC Corrosion		1. Bond wire fatigue		1. Cu/ELK cracking	Bonding force induced			
	uBump/C4 Bump/UBM	1. Electromigration				1. Bump joint cracking 2. Bump joint fatigue	1.Thicker IMC from uBumps			Multi Physics Bump EM - How does local current, temp, temp gradient and stress affect bump EM?	Bump fatigue - How does load temp, temp variation and stress affect fatigue life?	
	TSV/Interposer	1. Electromigration 2. Barrier Dielectric breakdown				1. Cu pumping/TSV pop up	1. Si and Cu CTE mismatch causing Cu extrusion 2. Non reversible plasticity at high temp			1. TSV EM - How does local current, temp, temp gradient and stress affect TSV EM? 2. TSV Pop Out and effects on TSV/Si interface delam	Barrier breakdown - How does voltage/current, temp and stress affect TSV barrier BD?	
	Passivation	1. Passivation cracking	1. EOS induced cracking	1. Passivation cracking 2. Passivation delamination 3. Delamination between passivation and underfill/Molding compound		1. Passivation cracking	1. Stress from packaging 2. Stress concentration in SiN					1. Package material thermal/mechanical properties 2. Die metal stack and thermal/mech properties 3. uBump/C4 bump/TSV thermal mechanical properties 4. Cu/ELK Fracture criteria 5. Void initiation and propagation criteria 6. Interconnect fatigue/creep model 7. Package interface fracture criteria 8. Moisture diffusion and vapor pressure model 9. IMC thermal/mech/electrical properties 10. Photonics optical properties
	Underfill			1. Underfill to die/substrate delamination 2. UF Expansion	1. Moisture degrade bonding interface 2. UF Moisture absorption	1. Bump joint cracking						
	High Density Substrate	1. Metal trace electromigration		1. Metal trace corrosion		1. Metal trace/via cracking				Cu trace EM - How does load current, temp and stress affect Cu trace EM?	Cu trace/Via cracking - How does voltage/current, temp and stress affect Cu trace/via cracking?	
Packaging/ System	Wafer Level Package					1. Warpage						
	Fanout Package					1. Warpage						
	2.x/2.5D Interposer Package					1. Warpage						
	3D Package					1. FinFET Ion shift due to a. TSV/Si CTE mismatch b. uBump stress c. Underfill/EMC shrinkage 2. TSV effects on BTI/HCI 3. BEOL cracking 4. Cu pillar joints failure						
	Laser/Receiver/ Modulator											
	Si/Photonics Chip											
	Co-packaged IC and Photonics					1. Optics misalignment						
	Wafer Level Integration of IC and Photonics											
	Known Good Die	ESD				1. Die edge cracking 2. Under bump ELK cracking						
Module/ System	Printed Circuit Board Assembly					1. Solder joint cracking 2. PCB failure		1. Solder joint cracking 2. Pad damage		Board level Solder Joint Reliability	ANSYS Mechanial	1. PCB thermal/mech properties 2. Solder joint fatigue/creep model 3. Solder joint dynmic/impact properties

3.2.3 Difficult multiscale interaction challenges for HI

HI advances and diverse chiplet architectures will place new emphasis on the degradation modes discussed above. In particular, difficult challenges are summarized below in six categories:

(i) Challenges due to global stresses:

Figures 18 and 19 show the overall CPI landscape for both the CPI 'strength' and 'stress.' 'Strength' distribution includes the 'intrinsic strength' (determined by the technology, material intrinsic behavior and nominal process) as well as the 'extrinsic strength' (determined by fab and die process variations). The corresponding 'intrinsic stress' is mainly determined by the package design, assembly material and process, and life cycle loads.

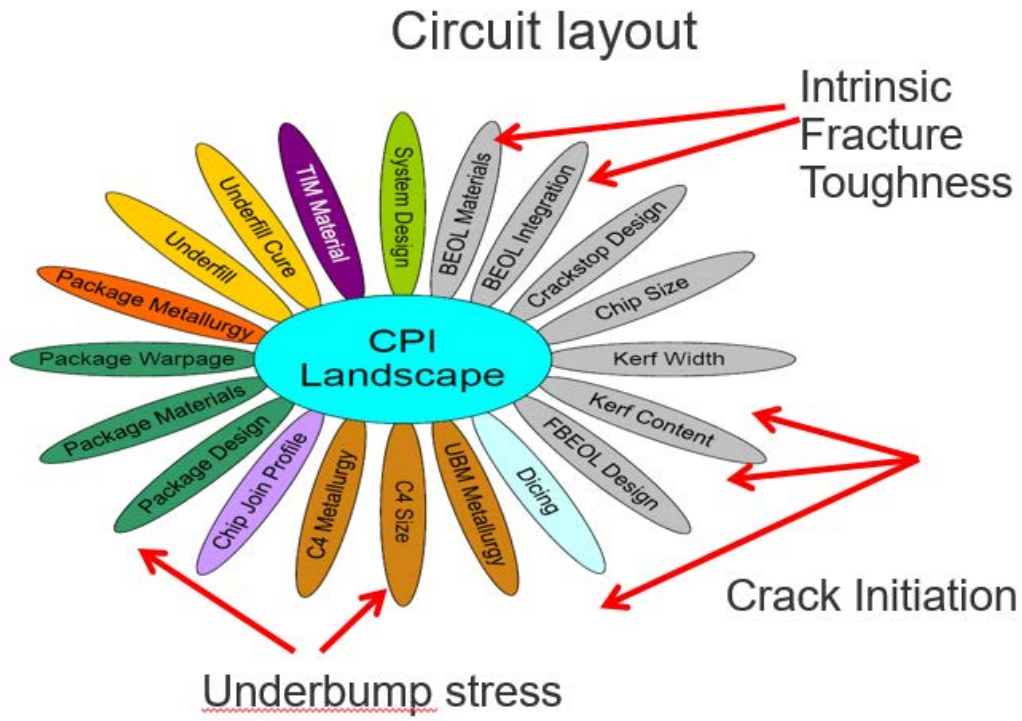


Figure 18. Overall CPI Landscape

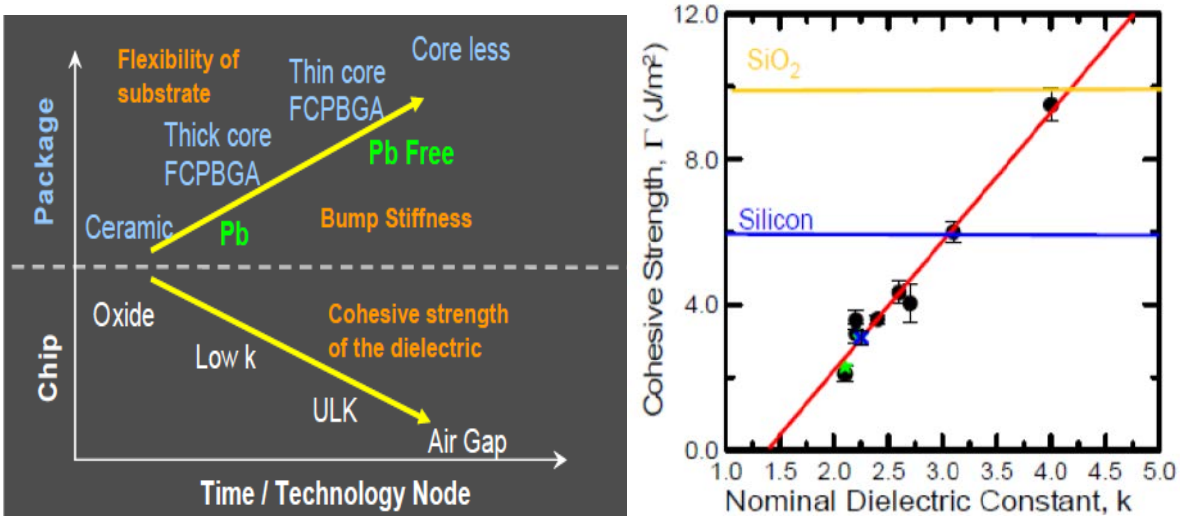


Figure 19. CPI Challenges from both 'Strength' and 'Stress' perspectives
[Source for Figs 18 and 19: IBM IRPS Tutorial, 2012]

The overall CPI challenges come from three aspects in Figures 18 and 19:

a. The 'intrinsic strength' is continuously decreasing due to the scaling of Si technology. The adoption of ELK is one of the major reasons. Both the ELK material strength and the Cu/ELK interface strength are lower in more advanced nodes.
b. On the other hand, the 'intrinsic stress' is continuously increasing due to such factors as increase in die size, adoption of Pb-free interconnection bumps, and use of coreless substrates.
c. Both the fab and assembly process variations are increasing in advanced Si nodes and packages. That causes wider distribution of both 'extrinsic stress' and 'extrinsic strength'.

The above three factors will collectively contribute to a significant increase in the 'stress' vs. 'strength' interference in the more advanced nodes and packages.

(ii) Challenges from FinFET Self-Heating Effects (SHE):

As indicated in Figure 20, the self-heating effect in a FinFET has significant impact on FEOL reliability due to degradation mechanisms such as HCI, Bias Temperature Instability (BTI), TDDB, and BEOL interconnect EM and thermal fatigue performance. The reliability challenges come from the following major factors:

- **FinFET Scaling:** The scaling of FinFETs from 20nm, 16/14nm down to 7nm will significantly increase the SHE due to the increased density of FinFETs. The next-generation Gate All Around (GAA) transistor architecture will further exacerbate the SHE reliability issues due to increased interactions between electrical and thermal/mechanical stresses.
- **Next Generation Interconnects and ELK Material:** Further scaling requires new materials for metal lines, barrier and ELK. Nanoscale material characterizations will be needed to understand the material properties and interfacial fracture toughness. As an example, Cobalt is under extensive research as a candidate for next generation nodes. The Cobalt to ELK interface strength could be a potential reliability challenge. SHE-induced stress will potentially cause failure of Cobalt itself and the Cobalt to ELK interface. Furthermore, the drive for scaling down the dielectric constant for next-generation nodes will introduce more fragile ELK materials with greater reliability concerns.

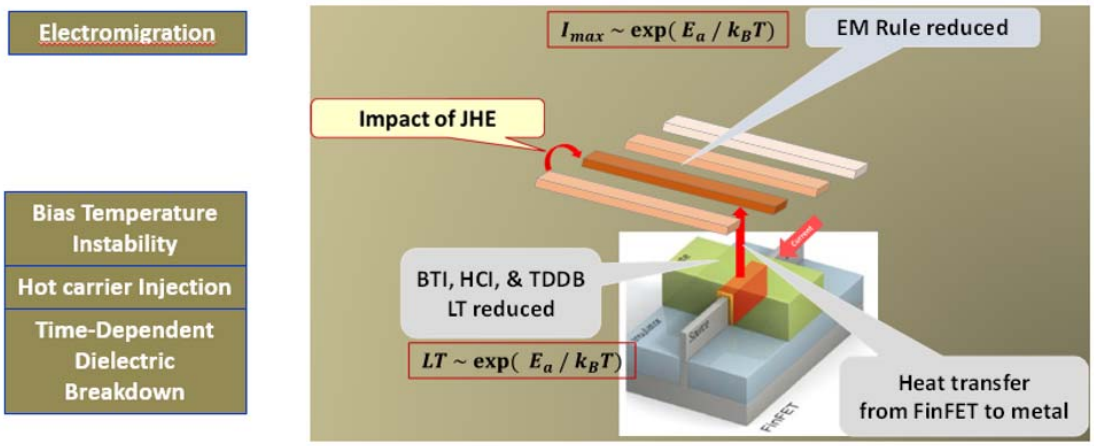


Figure 20. SHE effects on FEOL and BEOL reliability [Source: J-G Ahn, Xilinx, IRPS, 2016]

(iii) Electrical CPI Challenges:

The electrical CPI challenges come from the following major factors:

a. **Thinner Die:** Thinner die are required to reduce the form factor and accommodate 3D die stacking with TSVs. The same amount of warpage on the package can generate much higher mechanical stress in thinner die and thus affect the electrical field in FEOL transistors due to the piezoresistive properties of Si.
b. **Smaller TSV Pitch:** TSV pitch will get smaller to achieve higher I/O density. The current KOZ (Keep Out Zone) may be reduced to enable placement of all the active circuits on the die. The active circuit may therefore be subjected to a higher electrical stress, causing not only initial transistor performance shift but also long-term reliability concerns for both the FEOL, middle-of-line (MOL) and BEOL. These failure modes are HCI/BTI, Gate Dielectric TDDB, MOL TDDB, BEOL EM and BEOL TDDB.
c. **Response of Next Generation FinFET/GAA to Stress:** There is very little data available on transistor performance shift under stress. It is unknown how the sensitivity to stress will increase as FinFET and GAA architectures are further scaled down. This is a potential reliability challenge.
d. **Impact of Micro-defects:** With the form-factor scaling and the global stress challenges, it is critical to understand the effect of micro-defects on the electrical stresses and performance.

(iv) Challenges from Advanced Packages:

The CBPI reliability challenge is likely to become more severe in future generation of denser, larger HI packages. Most of the existing FOWLPs have RDL layers made by assembly equipment and these RDLs are now the weakest link when the FOWLP is mounted on a PCB. When the RDL processes are improved and their strength is ruggedized, then the weakest link could become chip cracking.

WLCSP large die size and ELK die will also pose a significant reliability challenge. Microcracks induced by the die singulation process will grow into macrocracks under mechanical stress and further propagate into the interior of the die from the die edge. With die disaggregation, it is critical to understand the interaction between the dies and its manifestation into reliability challenges. For molded packages with heterogeneous integration architecture, interaction with the mold is key to be characterized. Furthermore, thermal-mechanical concerns for ultra-thin dies/die-stacks in the manufacturing environment need to be considered as well – e.g. cold plate assembly, system testing, etc.

(v) CPI and CBPI Simulation Challenges:

CPI and CBPI stresses are accumulated from different fab and assembly steps. The hard failures such as open bumps are typically on the die BEOL, with soft failures such as transistor aging on FEOL. In order to completely understand these failures, we will need multi-process, multi-scale simulation flow. Existing commercial tools for CPI are not adequate to simulate the transistor/circuit level. Figure 21 shows the desired simulation capabilities from package and bump to the circuit GDSII levels.

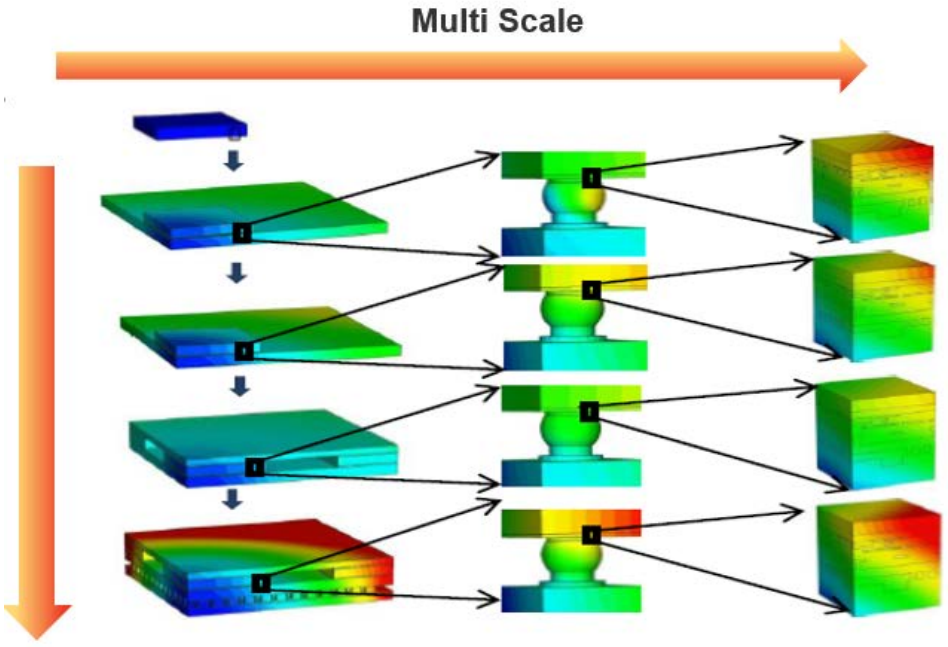


Figure 21. Multi-process and Multi-scale CPI simulation flow [Source: R. Rao, IRPS, 2014]

(vi) Challenges in Managing CPI/CBPI Risk:

With increasing system complexity and density and miniaturization in HI systems, integration of design, manufacturing and qualification processes to manage multiscale risks will become increasingly difficult. Figure 22 presents some of the challenges. For example, CPI reliability challenges include CPI Characterization, CPI design rules, and CPI degradation models based on reliability physics (RP) and machine learning (ML), for risk quantification (including CPI-induced FIT rate prediction).

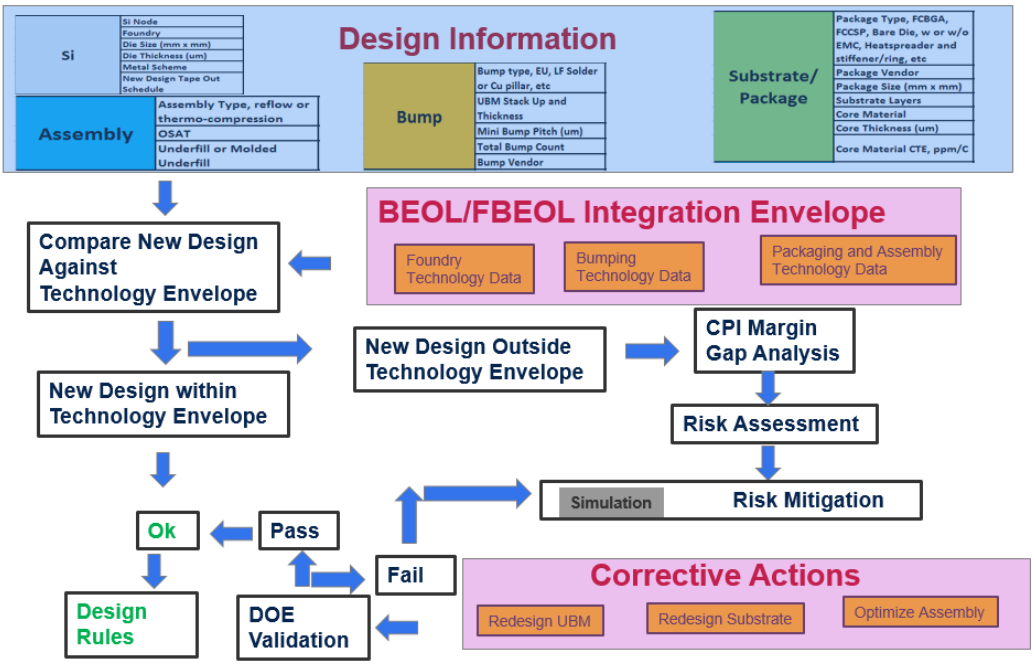


Figure 22. Flowchart for managing CPI risks [Source: R. Rao, IRPS, 2015]

3.3. Manufacturing for Reliability (MfR)

Manufacturing variabilities are directly related to process variability, dimensional tolerances and yield. This is a key aspect of process quality. In turn, process quality can be treated as the initial condition for subsequent reliability outcomes. Furthermore, the manufacturing process has fundamental influence on the resulting material composition and properties, on residual stress fields created in the product and on distributed flaws such as microcracking, voids, porosity, interfacial debonds, etc. All of these attributes have an influence on product robustness and durability. Thus there is a very direct multifaceted relationship between manufacturing process and product reliability.

Microelectronics fabrication already requires a complex multiphysics process flow that is used to control feature sizes down to nanometer length scales. In advanced HI systems of the future, the diversity of the architecture and process will become far more complex, requiring a convergence of semiconductor fabrication processes with packaging and integration processes such as 3D interconnection, high density interposer, redistribution layer (RDL) and substrate fabrication processes. In other words, heterogeneous integration will require continuing innovation with FEOL/MEOL/BEOL/Far-BEOL processes. HI will continue to blur the distinction between FEOL and BEOL steps, merging FEOL and BEOL tool performance for leading-edge, heterogeneous integration technology applications.

Process metrology, process variations and process control will be extremely important for managing and meeting quality and reliability targets. Process metrology and automated inspection capabilities at these length scales are going to be extremely challenging, pushing the capabilities of extreme UV optics, 3D laser interferometry and e-beam multibeam scanning microscopy, for assuring sufficient process yield.

Another important enabling technology needed for HI systems manufacturing is proactive simulation-based approaches for innovative process design and process optimization. This will require new multiphysics high-fidelity process modeling capabilities and relevant modeling infrastructure. The Modeling and Simulation TWG addresses this issue in their chapter (see Figure 2 in Chapter 14, 2020).

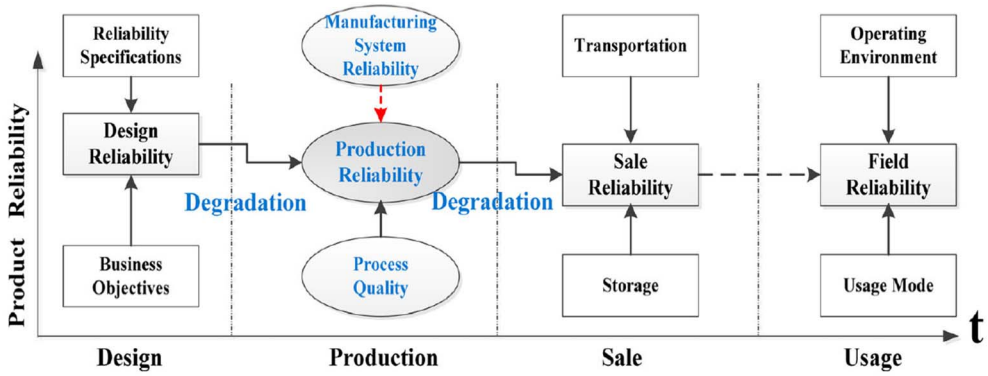


Figure 23. Role of production process on product reliability [Source: He, at al, Total Quality Management, 2016]

With the increasing complexity and diversity of manufacturing processes, the concept of '*zero defects'* may no longer be an affordable goal in HI systems. Innovative concepts of fault-tolerant system design and resilient system design will have to be developed and harnessed, to create highly functional systems that do not have to rely on *zero defect* manufacturing.

There has been increasing attention focused by the research community on the connection between quality and reliability. Recent papers have presented integrated approaches for reliability-oriented quality management. Figure 23 shows one such depiction of the role of the manufacturing process in ensuring product reliability, presented by He and coworkers. While this was a generic study on process quality and reliability, not specifically focused on HI electronics systems, many of the outcomes of this paper are still relevant to the present discussion on HI systems reliability.

Based on this quality-reliability inter-relationship, the authors have proposed a quality management framework shown in Figure 24.

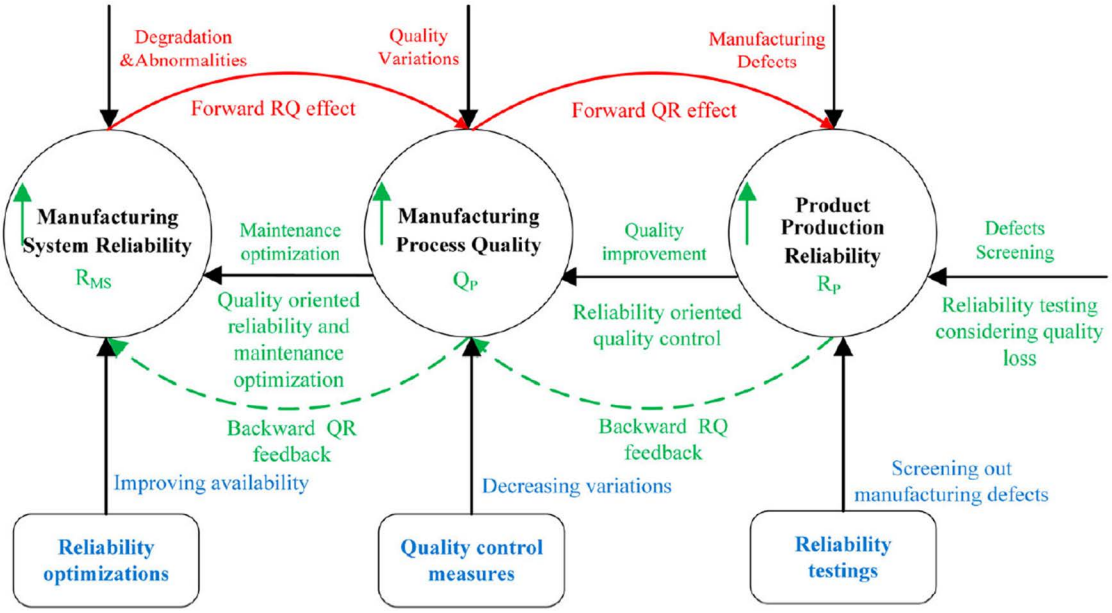


Figure 24. Reliability-oriented process quality management framework [Source: He, at al, Total Quality Management, 2016]

3.4 Qualification for Reliability (QfR)

QfR involves comprehensive testing of a product against all its quality and reliability specifications related to its intended application prior to product release. The process of QfR is absolutely essential since it allows both the manufacturer and the consumer to recognize and characterize the 'useful' life of a given product. As highlighted in Figure 1, unreliability comes from the probability that the applied 'stress' will exceed the inherent 'strength' of the product. Hence, QfR needs fundamental characterization and understanding of these stress and strength vectors. 'Stress' involves life-cycle Use/Field Conditions or Mission profiles (Market Demand) that the products will

experience, whereas 'Strength' involves the inherent design, materials and process variabilities (Technology Capability). Qualification for Reliability is a 'Cliff Dance' between Market Demand and Technology Capability.

A flowchart for product qualification is presented in Figure 25. The activities in this flowchart will have to be adapted for qualifying HI systems. Designing such qualification programs requires a knowledge-based approach to design the tailored test conditions that are relevant to the HI technology in question and to the life-cycle reliability expectation.

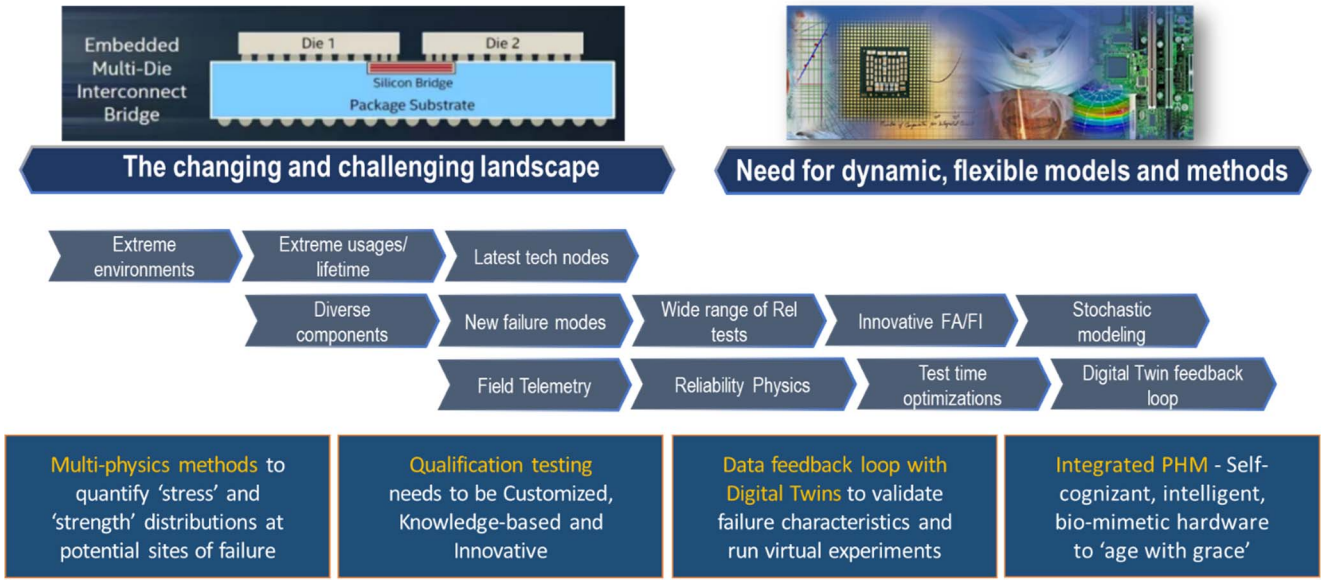


Figure 25. Qualification flowchart for assessing reliability [Source: Sahasrabuddhe, Intel]

Individual elements of the overall flow in Figure 25 are described below:

1) **Life-Cycle Use Condition (UC) characterization:** This refers to relevant environmental and functional loads that the HI system will be exposed to during its life cycle. These depend on the 6 HIR market segments of interest, specifically the specified design, operating limits and the relevant technology roadmap for these segments. UCs will help in 1) Performing realistic assessment of reliability risk; 2) Understanding the environmental extremes the products experience and the respective durations; and 3) Enabling design of accelerated testing of parts (to understand legitimate failure mechanisms). New research is needed to identify the relevant degradation and failure mechanisms for HI systems of the future.
2) **Reliability Testing:** This refers to any type of evaluation to determine product performance over an equivalent of an extended period of time under a given set of conditions. Reliability testing helps in exposing products to appropriate stress conditions to test for quality or reliability issues. Knowledge Based Testing is defined based on the knowledge of UCs so only relevant test conditions and durations that simulate and accelerate UCs are used for qualification. Note that there are also Industry Standards, such as JEDEC (Joint Electron Devices Engineering Council), or market-specific requirements such as AEC (Automotive Electronic Council) for automotive. Some aspects to consider about reliability testing:
    a. Reliability tests are either life tests where testing is conducted at the normal operating conditions, or are accelerated life tests where testing is conducted beyond the normal range of operation to decrease the time to failure. These tests could be executed sequentially to simulate a given stress. It is important to ensure that these tests do not induce overstress leading to extraneous failure mechanisms.
    b. Defining test structures on test vehicles is vital to get appropriate parametric or non-parametric data from reliability testing.
    c. In-situ data monitoring is recommended to get high resolution data, whether it's pass/fail (test to failure) or parametric degradation. It also has benefits of lower samples sizes.
    d. The tests can be at the component, subsystem or system level to ensure the right boundary conditions are captured in the tests.
    e. Test DOEs should be defined to ensure a statistically significant sample size is included and the samples under testing represent manufacturing variabilities.
    f. Quick Turn Monitor or Screen tests can be used for down-selecting materials and designs vs. running a typical test suite.

3) **Failure Mechanism:** This refers to the fundamental reliability physics as determined from failure analysis and/or similarity analysis. Understanding the failure mechanism is critical as it helps in defining the fundamental reason for failures such that materials, design or process can be altered to change the degradation and failure modes at play (See Table 3). Different failure mechanisms are associated with different reliability tests, e.g. Temperature Cycle captures low cycle fatigue, Vibration testing captures high cycle fatigue, Shock captures brittle failures whereas TH/HAST tests capture corrosion, electro-chemical migration and delamination mechanisms.
4) **Failure Analysis Tools and Metrology:** Amazing innovations have happened in the field of FA/FI in the past years from non-destructive analysis using x-ray, acoustics, and magnetic field imaging to destructive analysis using TOF-SIMS, SEM, and materials analysis. With the increasing complexity of heterogenous integration, metrology and root-cause analysis will become even more challenging.
5) **Reliability Analysis:** This involves comprehensive analysis of the data collected with the reliability tests such that individual mechanisms are modeled accurately to project the behavior at UCs. In addition to the statistical analysis, it is key that appropriate acceleration models and reliability models are established based on the understanding of the underlying Reliability Physics (RP). These reliability models can be purely empirical models (e.g. Arrhenius equation for temperature acceleration) or fundamental constitutive law based or Finite Element Modeling based. For FEM-based models it is important that comprehensive materials characterization is done (e.g. mechanical/structural tests like micro-tensile testing, nano-indentation) and the models are thoroughly validated (e.g. via interferometry).
6) **DPM prediction:** This is the quantification of the unreliability risk for the HI product undergoing qualification. Depending on the market demands (criticality of application, cost of replacement, etc.), DPM goals are defined. The objective of QfR is to demonstrate that these DPM goals are met with comprehensive/relevant testing and modeling.

There are different QfR engagement points during the product life cycle – engineering verification testing (EVT), design verification testing (DVT), process verification testing (PVT), and mass production (MP). It is critical that a feedback loop from each of these engagement points via Digital Twins is established to enrich the definition and execution of subsequent qualification milestones. In some cases, ongoing reliability monitors (ORM) are defined to provide this feedback during Mass Production.

QfR Challenges:

Changing and Challenging Landscape: Semiconductor HI devices continue to be introduced in the most extreme environments with extreme usage profiles and long-lifetime requirements. This demands a wide range of reliability testing. Also, the expectation is that the latest technology node will also offer the best reliability in these extreme environments. Furthermore, the diversity of components such as passives, MEMS, optical components, sensors, power, and RF components in a single package pose an interesting challenge not only for designing enveloping test suites for qualification but also for characterizing new failure modes with device interactions.

Need for dynamic, flexible models and methods: It is critical that multi-physics methods are established to quantify 'stress' and 'strength' distributions at potential sites of failure. Innovative FA/FI methods need to be explored with stacked dies and diverse components. Increasing use of field telemetry data with digital twins is vital to have a continuous feedback loop to validate failure characteristics and run virtual experiments.

3.5 Sustainment for Reliability (SfR)

Managing and ensuring system reliability and availability throughout the life-cycle of complex mission-critical products such as avionics, data servers, automotive electronics, and medical electronics, often require real-time individualized active health management. System prognostics and health management (PHM) has emerged as one of the key enablers not only for achieving system availability and reliability, but also for achieving safety, maintainability, supportability, and economical affordability. Real-time PHM monitors reliability of a system in-situ during the actual life-cycle conditions, to pre-empt unexpected failures and to mitigate system risks via timely corrective actions [1]. PHM combines sensor data, performance information and prediction models, to assess severity of system degradation from an expected 'normal' performance baseline. Several PHM methods are possible, such as: (i) methods based on data-analytics and machine learning; (ii) model-based methods; (iii) methods based on canaries; and (iv) hybrid fusion methods that combine several of the above. Researchers [Pecht, 2010; Lall, 2010] have reported successful implementation of fusion prognostics approaches, which combine the data-driven and model-based methods for diagnostics and estimation of the RUL of electronics. For electronic system prognostics, the complex architecture of electronics (both micro- and nano-scale components), the large variety of components,

and limited knowledge about failure precursors for electronic systems present important challenges to maturing the prognostics capability. Reliability physics-based methods offer significant guidance for effective PHM of electronics, relying on a product's actual life-cycle loads along with physics models to estimate the Remaining Useful Life (RUL) of the product. Applications of such methods have been successfully demonstrated in the literature for diverse electronic products, such as notebook computers, electronics in the space shuttle solid rocket booster, commercial off-the-shelf (COTS) devices, and flash memory. The concept of early warning of system degradation via PHM approaches is schematically illustrated in Figure 26a. Figure 26b provides an overview of the many advantages of PHM. For the actual engineering application of PHM, it is necessary to clearly understand the benefits and challenges it can bring. PHM enables users to monitor the health of systems, estimate and predict the RUL of systems, and take corrective action. These benefits are directly associated with system design and development, reliability, safety, maintainability, logistics, and life cycle costs. In this Chapter we are primarily interested in the impact on reliability and safety.

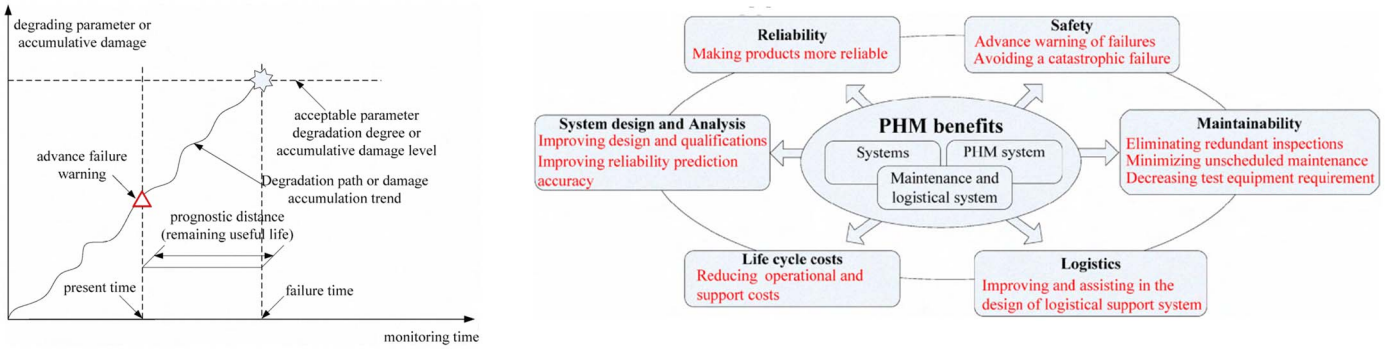


Figure 26. a) Advance warning capability of PHM; b) Benefits of PHM
[Source: Sun, et. al., IEEE PHM Conference, 2010, Macau]

Integrated PHM is expected to enable future HI systems to become self-cognizant, intelligent, aware of self-health and capable to implementing some degree of corrective action such as self-healing and/or modification of performance envelope to 'age with grace'.

4. System Reliability – Software Reliability, Operator Reliability, Interactive factors

Traditional reliability approaches are focused on prevention of hardware failures, but reliability of future HI systems will have to also consider multiple other sources of uncertainty and risk, such as: software reliability, hardware-software interactions, operator reliability and human-machine interactions, especially in systems with embedded adaptive control capabilities. In the 2021 edition of this chapter we briefly discuss software reliability methods. Detailed discussion of these topics is deferred to the 2022 edition.

Software reliability methods are fundamentally different from hardware reliability methods. Software reliability, or robustness, is the probability of failure-free software operation for a specified period of time and environment. Unlike hardware failures, software systems do not degrade over time unless modified. Software failures are not caused by faulty components, wear-out or physical environment stresses such as temperature and vibration; instead by latent software defects that were introduced into the software as it was being developed, but were not detected and removed before the software was released to customers. The best approach for achieving higher software reliability is to reduce the likelihood of latent defects in the released software. Software reliability growth models (SRGM) are based on mathematical functions that describe fault-detection and removal phenomenon in software [9]. These models, in combination with Bayesian statistics, need further attention within the hardware-orientated reliability community in the coming years. The 10-year horizon includes the items listed below to be given central visibility/priority in the HI roadmap:

- Develop software reliability growth models to predict remaining number of software defects (bugs).
- Create main-stream industry eco-systems for approaches for validated bug-finding rates.
- Establish techniques that can combine SW reliability metrics with HW reliability metrics.

5. Difficult Challenges and Disruptive Opportunities

Making new technologies reliable over the next 15 years, in this highly dynamic technology evolution scenario, is going to be a difficult challenge. Reliability tasks must be closely synergistic with the HI technology roadmaps proposed elsewhere by other technical working groups, shown in Tables 1a and 1b. While it is very difficult to assess

what turns technology evolution will take over the next 15 years, it is possible to make some informed speculations. While some segments of the industry will definitely continue to use conventional semiconductors (some industry leaders will progress to sub-5nm technologies and some segments with less challenging needs may continue to use more coarse technologies above 10 nm) and conventional binary digital logic, there is a strong possibility that many segments (especially those needing high-end computing) will switch to more sophisticated quantum processors and quantum computing, as well as molecular-scale electronics that will deploy transistors made from a few-molecules or even from single-atoms. Such a transition will be essential if we are to get past the fundamental limitations of physics and economics that industry has hit in Moore's Law. Large companies such as Intel, Google, Microsoft and Apple have already made significant investments in quantum devices, with results expected in the 5 to 10 year time frame. These technologies are expected to start to see growth in maturation, complexity and field applications, in the 10-15 year time frame. Interconnection advances will include structures made from 2D nanomaterials (like Stanene, graphene) and 1D nanomaterials nanotubes and nanorods made from Carbon and other conductive materials. Rapid advances are also expected in miniaturization and density of photonic/optical interconnections for fast data transfer. Substrates and boards in highly integrated future systems will almost definitely require complex combinations of 3D additive manufacturing technologies and conventional subtractive technologies with ultra-fine feature capabilities.

The developers of leading-edge technologies based on *conventional semiconductor devices* will be looking to continue large-scale advances in heterogeneous integration (HI), such as ultra large–scale SOC integration with multi-core processors containing up to 10^{10}-10^{11} transistors and many multi-physics sensors/devices on a single giant chip, very large scale SIP/SOP integration with 3D stacks enabling up to 10^{2}-10^{3} IC components within a single package, all interconnected with interconnection structures whose sizes will be measured in nanometers rather than in microns. These large systems may have upwards of 10^{4}-10^{5} I/Os. Such large-scale integration and miniaturization will require significant changes in materials and processes and equipment and metrology. An example is the switch today to Cobalt as a conductor material in microelectronics. The biggest reliability challenges will be from the new yet-unknown degradation modes and statistical variability in the new device and interconnect materials used for devices/features that will be of the same length scales as microstructural and nanostructural materials defects. It will be extremely challenging to find highly integrated supply chains that have the know-how, sophistication and ability to understand and manage such complex reliability challenges. Stochastic process/material variabilities will be so significant at such small length scales that 'zero-defects' is likely to become an extinct concept.

The adopters of *quantum devices* will have to solve an entirely different and new set of challenges to make them stable enough and compact enough to compete with length scales and densities and functionalities and reliability of conventional semiconductor device technologies. Another major challenge will be the ability to interconnect a significant number of quantum processors via a single quantum bus to increase the processing power or to interconnect molecular electronics devices (such as single-molecule transistors) together to form functional devices. Quantum processor technology today is at a nascent stage, with many laboratory demonstrations but very few industrial-scale demonstrations, and significant global pan-industry investments are needed to realize these goals. Finally, we do not have adequate software infrastructure today to take full advantage of such quantum processors. One of the primary reliability challenges today in quantum devices is to get such devices to retain their quantum state for reasonable intervals of time (> microseconds), and researchers are working on achieving more stable quantum states. The instability modes and degradation modes are poorly understood and controlling their quantum probabilities in a repeatable manner will be a big challenge.

In addition to technical complexities with dimensional scaling and new materials, short technology development cycles along with fast production ramps behoove the industry to invent and adopt lean and effective reliability design, characterization, assessment and monitoring methodologies. In Section 3.2, we focused specifically on Chip-Package Interactions (CPI) because of the importance of its influence on reliability.

Table 4 provides a tabular discussion of the overall difficult challenges expected in making the proposed new leading-edge HI hardware technologies reliable, dependable and affordable. Table 4 has been separated into 3 sub-tables in this document for ease of formatting. Table 4a addresses reliability tasks that will be important during product design; Table 4b addresses reliability tasks relevant during product manufacturing; and Table 4c focuses on reliability tasks during product qualification and support.

Table 4a: Difficult Challenges and Approaches for Designing Reliable HI Technologies

Reliability Targets	**Identification of customer goals**	**1-5 years** • Evolution of Quality and Reliability (DPPM) goals across different HIR application segments • Identification of customer goals for critical applications - Functional safety, security goals • Cyber security goals for IoT Technologies • Developing industry standards for HI reliability targets **5-10 years** • Update of customer reliability expectations based on technology roadmaps of different HI application segments **10-15 years** • Update of customer reliability expectations based on new technology roadmaps of different HI application segments
Life cycle conditions	**Environmental & operational conditions**	**1-5 years** • Defining environmental & operational conditions for emerging markets already known / on the horizon • Use IoT infrastructure and instrumented fielded products to harvest life-cycle use-profiles • Identification of localized self heating due to power dissipation and chip-package thermal interactions • Identification of localized stress concentrations due to other chip-package interactions • Defining extremes for critical applications • Developing industry standards for environmental & operational conditions **5-10 years** • Update of customer usage models based on new technology roadmaps of different HI application segments **10-15 years** • Update of customer usage models based on new technology roadmaps of different HI application segments
Design for Reliability	**Reliability Physics (RP)**	**1-5 years** • Addressing reliability physics driven by multiphysics SIP integration (e.g. microelectronics, optics/photonics, MEMS sensing technologies, RF, power, analog/digital, quantum computing, • Identifying, prioritizing and modeling reliability physics challenges driven by new system designs, e.g. Thin boards, thick boards, modular applications, system cooling, • Identifying, prioritizing and modeling reliability physics challenges driven by unique market applications • Identifying, prioritizing and modeling reliability physics challenges on emerging transistors, e.g., gate all around and nano sheet, etc. • SHE induced new reliability physics such as the fatigue failure of interconnects and SHE accelerated HCI aging leads to Bias runaway in critical AMS circuits • Multi physics electromigration assessment including temperature, temperature gradient and stress gradient for all interconnects • Multi scale failure interactions among FEOL transistor, BEOL interconnect, TSV/µBump/C4 bump and package. • Board/System level interactions with package, particularly the wafer level and big size packages such as FanOut WLP RDL cracking, die cracking and underfill delamination, etc. **5-10 years** • New reliability physics models and tools for new technology roadmaps of different HI application segments **10-15 years** • New reliability physics models and tools for new technology roadmaps of different HI application segments
	Materials characterization for Reliability	**1-5 years** • Material characterization at the feature scales • Characterization of surface finishes on inter-metallics stability • New material characterization metrologies development • Correlation of material behavior with reliability performance • Next generation interconnect material mechanical/thermal and electrical characterization • Nano scale interface strength characterization • Cu/Cu bonding characterization and molecular level simulation **5–10 years** • Characterization of new materials and correlation of material behavior with reliability performance for new technology roadmap **10–15 years** • Characterization of new materials and correlation of material behavior with reliability performance for new technology roadmap
	RP/AI^2-based co-design rules & standards	**1-5 years** • multi-physics co-design tools based on performance physics, models, reliability physics models and AI models, to enable design for reliability (DfR) for new technologies, length scales and HI system complexity listed in technology roadmap • New resilient and self-healing design concepts to replace 'zero defect' philosophy • AI Rules for Design for Reliability (DfR) based on real-time reliability data obtained from the field via IoT infrastructure • IC and Package co-design of performance and reliability • Thermal/Mechanical/Electrical multi physics design flow **5–10 years** • Improvements in co-design models, capabilities and tools and standards based on technology roadmaps **10–15 years** • Improvements in co-design models, capabilities and tools and standards based on technology roadmaps

Table 4b: Difficult Challenges and Approaches for Manufacturing Reliable HI Technologies?

Manufacturing for Reliability	Effect of process on material properties	1-5 years
		• Evolution of material properties through fab/pkg-board assembly processes (Change in IMCs, residual stress distribution, plating process impact on micro-structure, etc.)
		• Interaction of process materials (Flux, de-flux, media etc.) on the package materials
		• Characterization of effect of new additive and subtrative manufacturing processes on material behavior (and correlation of material behavior with reliability performance)
		• Accumulative stress evolution from the fab processes to assembly/integration
		• Multi process steps stress simulation to understand the process parameters, materials and sequences effects on the CPI/CBPI reliability
		5–10 years
		• Extension of process technology studies to understand impaxct on new materials proposed in technology road-maps
		10–15 years
		• Extension of process technology studies to understand impaxct on new materials proposed in technology road-maps
	Defects (from RP perspective)	1-5 years
		• Effect of dimensional scaling (wafer thinning and handling, chip to chip, chip to wafer, chip to package interconnect misalignment, TSV defects,etc.)
		• Effect of material / process interactions on defects (ESD…)
		• Outlining critical attributes of defects that matter for manifesting into quality or reliability mechanisms. Understanding the physics of defect evolution
		• Metrologies to detect defects
		• Industry standardization for defect characterization?
		• Reliability based on resilient and self-healing systemdesign, to replace 'zero defects' philosophies
		• Characterization of process variabilities, defect structures and defect densities for new additivemanufacturing processes
		5–10 years
		• Extension of process variability/defect minimization technologies and standards based on new technology road-maps
		10–15 years
		• Extension of process variability/defect minimization technologies and standards based on new technology road-maps
	Process metrology & sensors	1-5 years
		• Testing of singulated components with fine geometries (micro-pillar / micro-bumps (sockets, probes))
		• New process (real-time, offline) metrologies (optical, others) to monitor key package attributes throughout the process
		• Innovative use of sensors (resistive, optical, acoustic, etc) to measure key attributes in-situ
		• Process metrology methods needed for new additive manufacturing methods
		5–10 years
		• Extension of process metrology technologies based on new technology and manufacturing road-maps
		10–15 years
		• Extension of process metrology technologies based on new technology and manufacturing road-maps
	Process control & yield (AI and feed-forward)	1-5 years
		• Characterization of interaction of different process modules on key failure mechanisms
		• Models and methods for data analytics/ DFF in process (analyzing critical package attributes data real time in the process and using feed-forward techniques to minimize the damage metrics)
		• Process control methods for new additive and subtrative processes, to minimize defect densities. 'Zero defects' philosophy may have to be replaced with resilient design concepts
		• Re-evaluation of 'zero defects' philosophy may have to be replaced with resilient and self-healing design concepts
		5–10 years
		• Development of new process control technologies based on new technology road-maps
		10–15 years
		• Development of new process control technologies based on new technology road-maps
	Stress screens & NDI[3]	1-5 years
		• New Non-destructive inspection metrologies for monitoring quality of complex package architectures
		• Development of quick / innovative stress screens to weed out early fails or monitor process health
		• Development of methodologies for selecting parts for stress screen based on data analytics to drive lower sample sizes and faster data collection.
		5–10 years
		• Development of new stress screen methods for new technology road-maps
		10–15 years
		• Development of new stress screen methods for new technology road-maps

Table 4c: Difficult Challenges and Approaches for Qualifying and Supporting Reliable HI Technologies

KBT[4] for Reliability Qualification: EV/DV/PV[1]	RP/AI-based acceleration models	**1-5 years**
		• Identifying relevant damage metrics for characterizing reliability physics (class of mechanisms)
		• Identifying relevant damage acceleration models based on RP/AI methods and accelerated stress-test data as well as field reliability data (obtained via IoT infrastructure)
		• Damage acceleration models for concurrent multi-physics stresses, based on reliability physics (RP) and artificial intelligence (AI) methods
		• Damage acceleration models for chip-package interaction (CPI) failures
		5–10 years
		• Development of new RP acceleration models to new technology road-maps
		10–15 years
		• Development of new RP acceleration models to new technology road-maps
	Test methods (test structures, sensors, metrology); RP-AI-based margin testing and accelerated life testing Test standards and guidelines	**1-5 years**
		• New test methods for built-in tests and faster reliability data collection
		• Lab level tests and IoT based field data for characterizing RP and AI acceleration models
		• Sequential / step stressing for interacting fail modes
		• Development of system level validation methodologies based on RP/AI algorithms and test data and field reliability data (obtained via IoT infrastructure)
		• Innovative test structures (resistance, leakage, capacitance measurements)
		• Accelerated testing strategies based on early degradation-rate and PHM methods
		• Metrologies to isolate failures
		• KBT non-proscriptive test standards that can foster innovation
		• Concurrent multi-physics accelerated test methods for interacting failure modes at subsystem and system level
		• Multi level CPI test structures
		5–10 years
		• Development of test methods and standards for new technology road-maps
		10–15 years
		• Development of test methods and standards for new technology road-maps
	Failure analysis methods	**1-5 years**
		• Failure detection for smaller dimensions and complex geometries
		• Failure isolation / detection for new materials
		• Non-destructive methods for isolating failures in 2.5D/3D/WLP
		5–10 years
		• Development of new failure analysis methods to new technology roadmap
		10–15 years
		• Development of new failure analysis methods to new technology roadmap
PHM[5]	RP/AI-based Fusion prognostics PHM Standards and guidelines	**1-5 years**
		• Multi-physics sensing technologies and canaries integrated into the hardware
		• Artificial intelligence methods (based on Data-analytic and machine learning algorithms) integrated into firmware
		• Fusion prognostic methods that combine reliability physics and artificial intelligence methods
		• Monitoring circuit degradation and adapt voltages to compensate the aging effects
		• BIST resistance test for critical interconnects
		5–10 years
		• Evolution of fusion prognostic methods to new technology roadmap
		10–15 years
		• Evolution of fusion prognostic methods to new technology roadmap
Supply Chain	Role of Supply Chain in Managing Reliability	**1-5 years**
		• Knowledge coordination with supply chain to maintain quality and reliability
		• New IP management models for supply chain coordination
		Methods to prevent supply chain contamination and counterfeit
		5–10 years
		• Extension of supply chain coordination methods to new technology roadmap
		10–15 years
		• Extension of supply chain coordination methods to new technology roadmap

6. Approach and Roadmap for Addressing Difficult Challenges

To solve the reliability challenges that are likely to emerge in technologies discussed in the HI Technology roadmaps (and briefly overviewed in Section 3 above), we will need investments in new reliability physics, artificial intelligence models, machine learning algorithms, and data management infrastructure (via IoT), to provide designers the right set of models and tools to allow design for reliability. Such a systematic proactive approach will also offer unique opportunities to reduce time-to-market for new product introduction (NPI) and to minimize the cost of ownership over the product's life-cycle. This is often termed 'cradle-to-grave' cost optimization. In fact, we argue that such a systematic integrated approach also offers the opportunity to use lessons learned from prior product generations to lower the NPI cost for upcoming product generations. For the purpose of this discussion, we term this business case as 'cradle-to-cradle' cost optimization. Table 3 above has provided a tabular discussion of all the solutions that will be needed to address the reliability challenges expected in the HI roadmap.

Implementation of design solutions will require knowledge of the fundamental degradation physics in ultra-complex advanced conventional semiconductor systems as well as knowledge of the quantum mechanics of new emerging quantum device technologies. At the ultra-small length scales in question, designers will have to consider reliability up-front in an integrated seamless concurrent manner during product co-design. Designers will need effective simulation and co-design tools to understand and quantify multi-physics chip-package interactions (electrical, magnetic, optical, thermal, and mechanical) in such complex systems, so that their effects on hardware reliability can be correctly identified early in the design process. Reliability can no longer be a separate sequential assessment process after the functional design is completed.

The effect of process variabilities and materials variabilities on hardware reliability must be characterized using a combination of empirical studies, fundamental RP methods and AI approaches. This will be especially true in the future manufacturing infrastructure where both 3D additive and subtractive process technologies will have to co-exist, since additive manufacturing methods produce an entirely different set of material defects and structural defects, compared to subtractive technologies. Process control strategies must be developed based on such quantitative understanding, in order to minimize defect densities and maximize yield. Since 'zero defects' is likely to remain an unrealizable goal at these length scales and at this level of complexity, product designers and system designers in future HI systems will have to adopt highly resilient system design concepts, in order to field functional devices that have sufficient reliability to meet the customer's reliability expectations.

Accelerated stress testing for design/process verification and qualification will also require special considerations. Tools will be needed for customizing such accelerated test protocols, based on the specifics of individual designs, life cycle usage conditions and reliability goals. Such knowledge-based customized testing must be universally adopted across the supply chain and the customization should be based on acceleration models that are rooted in fundamental RP and AI principles. Over-standardized, one-size-fits-all testing methods will simply not be acceptable or competitive for such complex systems/technologies. The ultra-small length scales and super-high functional density will require systematic planning of built-in-testing strategies and capabilities. New generations of test equipment and testing metrologies will be needed for testing the new complex technologies and systems discussed in Secs 3.3 and 3.4. This topic will be further discussed in the 2022 edition of this chapter. The IoT infrastructure offers unprecedented opportunities to harvest fertile reliability data in real-time from fielded products, to be used to supplement data from design/process verification tests. This will offer powerful opportunities for reducing NPI cost and time-to-market.

Real-time personalized prognostics and health management (PHM) of fielded products will have to become a standard approach for managing and supporting system reliability in the post 'zero-defect' era. Integrated PHM canaries must become a regular feature of self-cognizant, intelligent, bio-mimetic hardware that can survive and function and 'age with grace' instead of failing unexpectedly in-service. Built-in anomaly detection and real-time diagnostics/prognostics (using RP/AI algorithms) should become a regular feature of the firmware design. Systems will have to be developed with extensive capabilities for neuro-morphic adaptive system-reconfiguration as well as dynamic self-healing (where feasible), to cope with degradation of functionality throughout the life-cycle. As the cost/transistor and cost/device is driven down, massive sacrificial redundancy and intelligent over-design may become part of the realistic toolkits available to designers of resilient systems. Table 5 shows the vision of future capabilities of complex HI systems, to continue to perform reliably.

Table 5. Approaches to ensure high reliability and availability of future complex HI Systems

		Reliability Targets	Life Cycle Conditions	Design for Reliability	Manufacturing for Reliability	Qualification for Reliability	Sustainment for Reliability	Supply Chain
Applications	Mobile IoT Medical, Health and wearables Automotive HPC & Data Centers Aerospace and Defense	**1-5 Years**: Multi-physics fusion approaches for reliability assurance • Bottom-up *Reliability Physics* based approaches, tools, infrastructure • Top-down *Machine Learning & AI* based approaches, tools, infrastructure **5-10 Years**: Fusion approaches for co-design (based on 'digital twins') and life-cycle PHM of next-gen robust HI systems • Fault-tolerant systems • Resilient systems **10-15 Years**: Fusion approaches for intelligent, adaptive, reconfigurable products with integrated autonomous life-cycle management capability • Intelligent, self-cognizant systems • Self-healing systems						
Package Integration	WLP (FO/FI) 2.5D and 3D integration Wafer Singulation and Thinning Chip-package interactions (CPI) Interconnects (TSV8s, µbumps, wirebonds, Flip Chip solder joints) Substrates/Interposers Board Assembly SOC/SIP/SOP[9] formats							
Technologies	Microelectronics > 10 nm Microelectronics <10 nm Photonics & optics MEMS and sensors Power electronics Energy souces (Batteries/PV[6]/FC[7]) RF/Analog Devices							

Finally, rigorous supply-chain training will be essential if the industry as a whole has to transition to complex new multi-physics microsystems. Businesses will have to develop new IP models so that critical concepts can be shared with the supply chain, in order to maintain high quality of incoming supplies and contract manufacturing.

7. Summary

This document lays out the potential difficult challenges, potential solution approaches, and necessary infrastructure that we envision as important steps for establishing best practices in making future HI hardware technologies highly reliable, dependable and affordable. Particular attention has been paid to Chip-Package Interactions (CPI). This section has laid out the importance of an integrated approach towards reliable HI systems, based on strategic integration of reliability physics with powerful artificial intelligence algorithms that can leverage the unprecedented level of real-time field reliability data that is becoming available via the IoT infrastructure. The business case for such an integrated approach rests in the tremendous opportunities for reducing NPI time and 'cradle-to-cradle' cost of ownership.

The present version of this document is necessarily generic and lacking in specific details, since reliability practices are dependent on the specifics of the technology roadmap. This TWG will continue to work with other Technology TWGs in the HIR Roadmap team, to continue to add granularity and specificity to this section. Furthermore, in future versions, this document will be expanded in scope to include other aspects of system reliability (including software reliability/security and dependability of human/machine interactions) for the entire HI ecosystem.

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TWG members who have provided inputs and co-authored this section are listed below. In future versions, this section will be expanded in coordination with other TWGs as mapped out in Table 1a. Furthermore, additional co-authors will be added in the areas of software reliability and artificial intelligence.

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