



## HETEROGENEOUS INTEGRATION ROADMAP

**2023 Edition**

# Chapter 9: Integrated Photonics

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## Chapter 9: Integrated Photonics

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### Executive Summary

Global network requirements are changing with the rise of the internet of things (IoT) and the migration to the cloud of data, logic and applications. These changing requirements must be accommodated while maintaining the pace of progress in size, cost and power per function that we have enjoyed for more than 50 years. This progress was based primarily on the benefits of Moore's Law scaling of CMOS electronics. The introduction of photonics into the transmission, processing and even the generation of data through optical-based sensors is a key enabling factor for continued progress in these areas as we reach the limits of the physics, and the benefits of Moore's Law scaling slow.

Packaging is a limiting factor in electronics today since it has not kept pace with Moore's Law in scaling. Today electronics packaging is more expensive than the package contents in many cases, and this lag contributes substantially to increased power requirements and latency. The solution to these limiting factors is a work in process, with innovations such as wafer level packaging (WLP), system in package (SiP) architecture, 3D integration and heterogeneous integration. The integration of photonics and plasmonics into these emerging electronics packaging solutions is a focus of this Chapter. Continued innovation in other aspects of integrated photonics will also be essential and are addressed in this Chapter.

There will be many specific challenges in integrating the benefits of photonics into the fabric of the global network. The solutions, however, cannot come from just the packaging of photonic components. The co-packaging of electronics, photonics and plasmonics will be required to address these substantial new challenges in order to meet the expanding requirement for higher performance, higher reliability, increased security, lower latency and continued decrease in cost per function. The packaging of photonic integrated circuits (PICs) will face the same challenges faced in packaging electronic ICs, with the added complexity of integrating both active and passive photonic elements as well as the necessary electronics. Wherever possible, industry must adopt and adapt the packaging technologies developed for electronics to decrease cost and time-to-market for packaging of individual PIC circuits and incorporating PIC circuits and other photonic components into complex 3D SiPs through heterogeneous integration.

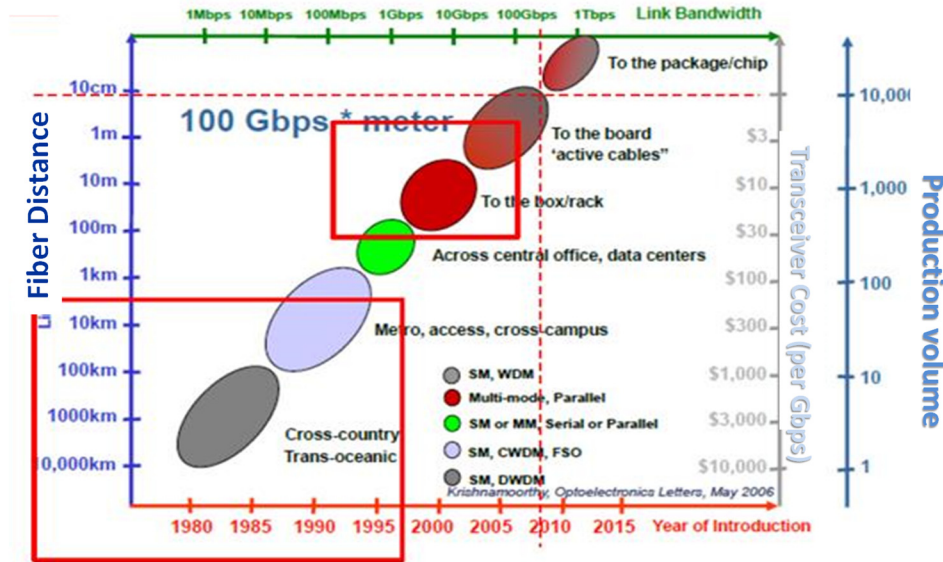
There will be new device types, new materials, new package production processes and new equipment required to accomplish these objectives. Some of these required innovations we know today, but many specifics that must be addressed over the next 15 years are not yet known. The objective of this Roadmap Chapter is to identify challenges with sufficient lead time to allow solutions to be identified and proven before they become roadblocks to the pace of progress for the industry. Although we use the word "packaging" in many places to define the challenges and potential solutions, this term will not be accurate over the life of this Roadmap. The activity is more correctly defined as **systems integration at the package level**. Advanced packaging in the world of complex 3D, heterogeneously integrated System in Package (SiP) products is truly system-level integration.

### Introduction

Photonics dominated long-range data and telephony by the 1970s due to cost and power advantages, but made slow progress during the next 30 years due to small market size and high component cost. Since the turn of the century, much progress has been made due to expanding market size driven by increasing data traffic and the cost advantages of expanding volume. Global internet traffic was projected to reach 2.0 zettabytes by 2019 from 0.7 zettabytes in 2014, a 23% CAGR. Two thirds of this traffic originated from non-PC devices in 2019 with growth coming from TVs, tablets, smartphones and machine-to-machine communication. Each one of these growth sources has some important differences that will impact its packaging requirements. Broadband speeds more than double in the 5-year period from 2014 to 2019.<sup>1</sup>

The introduction of photonics into the transmission, processing and even the generation of data through optical-based sensors are key enabling factors for continued progress as we reach the limits of the physics and the reality that the benefits of scaling are slowing and Moore's Law is nearing its economic end.

<sup>1</sup> This material is from the Cisco web site; similar forecasts are available from other companies active in serving internet markets.  
HIR 2023 version (eps.ieee.org/hir) Chapter 9, Page 1 Heterogeneous Integration Roadmap



Source : Brocade

Figure 1. Growth in volume and drop in cost as photons get closer to the electronics

Integrating components into their packaging is a limiting factor in today’s digital world. Packaging has not kept pace with Moore’s Law in scaling. Today electronic-photonic integration and packaging is more expensive than the package contents in many cases, and it contributes substantially to increased power requirements and latency. The solution to these limiting factors is a work in process with innovations such as wafer-level packaging (WLP), system in package (SiP) architecture, 3D integration and heterogeneous integration and new materials which are dealt with in detail in other Chapters in this Roadmap. There are a rapidly growing number of electronic-photonic products with a wide range of packaging requirements and common requirements for providing a photon path either into or out of a package or both. Many have unique thermal, electrical and mechanical characteristics that will require specialized materials and systems integration (packaging) processes and equipment. They include:

- Light emitting diodes
- Laser diodes
- Active optical cables
- Camera modules
- E-to-O and O-to-E converters
- Optical modulators
- Optical sensors (photo diodes and other types)
- Photonic integrated circuits (PICs)
- Plasmonic photon emitters
- Lidar systems
- MEMS optical switching devices
- New light sources: monochromatic with high-speed switching (quantum dots + plasmons) and many more.
- WDM multiplexers and de-multiplexers
- ..... Many more that have not yet been invented

**Scope**

The packaging of photonic integrated circuits (PICs) will face the same challenges faced in packaging electronic ICs, with the added complexity of integrating both active and passive photonic elements. Wherever possible industry must adopt and adapt the packaging technologies developed for electronics to decrease cost and time to market for packaging of individual PIC circuits and system-level products incorporating PIC circuits, photonics, plasmonic and other components into complex 3D SiP through heterogeneous integration.

The key difficult challenges for integrated photonics are:

**Physical density of bandwidth:** The majority of photonics other than long range communication is served by multimode fiber which does not fully support wavelength division multiplexing. The solution is to move to single-mode photonics with WDM, but adopting this solution has challenges in cost and making connections.

**Thermal drift of photonic component wavelength:** Stable wavelength is essential for integrated photonics. Both laser and ring-oscillator modulators have wavelength drift with temperature change. This limits the number of channels available in WDM and threatens the reliability of photonic communication. There are solutions in use today which require expense and power for stabilizing temperature. The better solution is to replace the components that exhibit thermal drift with new devices that have little or no wavelength drift with temperature change.

**Interconnect for single-mode optical fiber:** The single-mode fiber core is about 8 microns in diameter while multimode fiber is typically greater than 60 microns. This difference makes it difficult and costly to make low loss fiber-to-fiber connections between single mode fibers as the photons reach the printed circuit board, the package and maybe even on-chip. At the PCB level, experiments are under way to characterize an expanded beam solution. The solutions for PCB and package photonic interconnects will be different from those for on-chip applications.

**Test:** Testing of photonic parts is challenging, since the test for system-level integration must include both photonic and electronic testing at the wafer level, package level and system level. Contacting test points in a complex 3D SiP is challenging with electronics alone, and it is made much more difficult by requiring photonic test at each level. This will be addressed on more detail in the test chapter (Chapter 17, Section 2).

There will be many specific challenges to be addressed in implementing solutions to these four key challenges. The benefits of integrating electronics and photonics into the fabric of the global network and all components attached to it will not be fully realized until solutions are defined and implemented. The solutions, however, cannot come from just the packaging of photonic components. The co-packaging of electronics, photonics and plasmonics will be required to address these substantial new challenges and meet the expanding requirements for higher performance, higher bandwidth density, higher reliability, increased security, lower latency and lower cost in the future. There will be new device types, new materials, new package production processes and new equipment required to accomplish these objectives. Some of these required innovations we know today, but many specifics that must be addressed over the next 15 years are not yet known. The scope of this Roadmap Chapter is to identify electronic-photonic integration challenges with sufficient lead time so potential solutions can be identified and proven before they become roadblocks to the pace of progress for the industry. This scope covers integration of these components into emerging packaging solutions to decrease size, cost, power and latency while increasing performance and bandwidth.

This chapter is organized into sections dealing with 6 specific focus areas that are representative of challenges that occur in Electronic-Photonic developments to meet future requirements. The challenges and attributes are grouped by technology in the tables since many are shared across the topical areas and will have entries that cover several focus areas. The special focus areas are:

- Photonic components such as sensors, emitters, modulators, multiplexers, demultiplexers.
- Integrating these components into subsystems and systems
- Special applications:
  - Data centers and the global network
  - Photonics in the automotive industry
  - Photonics for IoT
  - Supply chain requirements

## Difficult Challenges

Packaging and test for photonics have found it difficult to scale their performance or cost-per-function to keep pace with transistors. The top-level difficult challenges in the future will be the reduction of power per function, cost per function and latency, while maintaining or increasing the rate of improvement in performance, physical density, reliability and security. Moving photonics closer to the transistors, and heterogeneous integration of diverse components and materials, will provide solutions compensating for the shortfall from the historical pace of progress we have enjoyed from scaling CMOS. Photonics offers the highest bandwidth density and lowest power requirement for moving data. The integration of electronics and photonics into SiP architecture with MEMS, sensors, RF, plasmonics, integrated passives and other components and devices which are yet to be invented will enable a continued “Moore’s Law or better pace of progress” for decades to come. There are many difficult challenges to be

overcome to achieve this vision. Some of the top-level ones are summarized in this section and they occur within the six topical areas defined above. A more detailed listing and some potential solutions are presented in a later section of this Chapter and in the tables of other Chapters in this Roadmap. Cross-references to these Chapters appear in the text where appropriate. Key attributes of Integrated Electronic-Photonic Systems are defined in separate attribute tables.

Difficult challenges are addressed by specific areas of the technology. The categories listed below are addressed in more detail in their respective HIR chapters:

- Co-design and simulation (Chapters 13 and 14)
- Materials and Emerging Research Materials (Chapter 15)
- Devices and Emerging Research Devices (Chapter 16)
- Test (Chapter 17) and Reliability (Chapter 24)
- Manufacturing including the supply chain (Chapter 18)

Many difficult challenges must be met to increase the rate of progress in packaging and test for the heterogeneous integrated electronic-photonic systems of the future. This will be essential to maintain or exceed the historical pace of progress for data-based industries. The key elements of the integrated electronic-photonic chapter are illustrated in Figure 2.

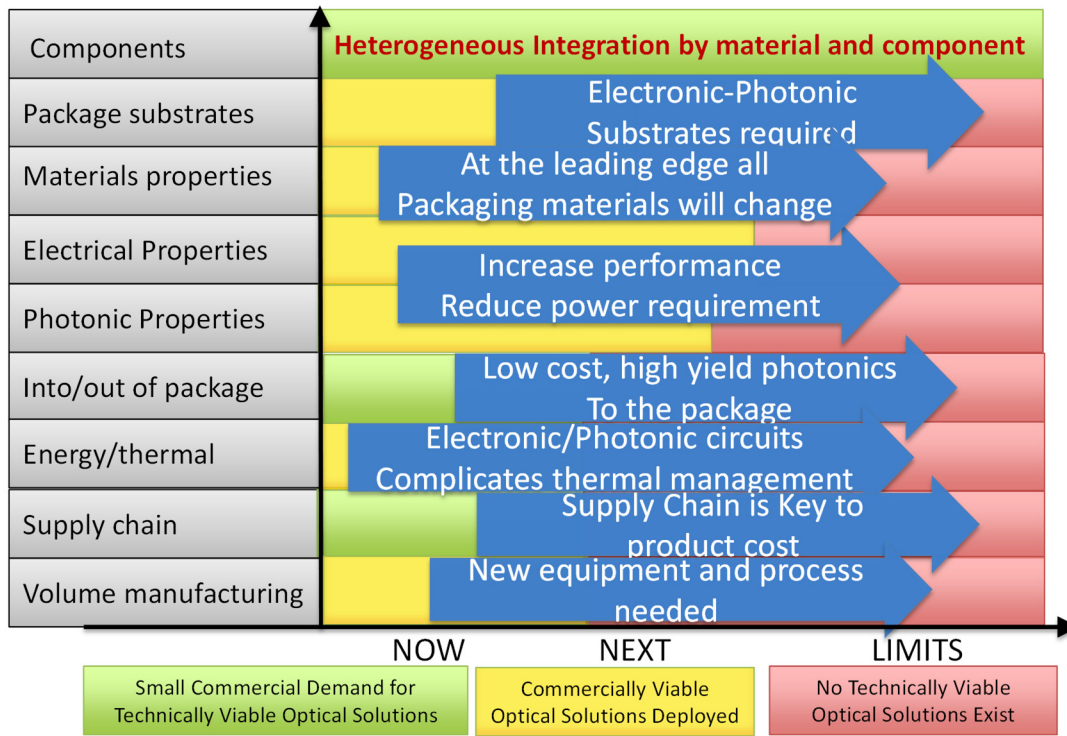


Figure 2. Photonic System Packaging Roadmap

The elements in yellow have known technical solutions that do not meet the full requirements, with cost and power being the primary reasons for shortfall. The elements in red currently have no known technical solutions. Both of these categories pose difficult challenges.

An initial list of difficult packaging challenges is presented in 3 categories; (1) On-chip interconnect, (2) Package assembly and (3) Test. These are analyzed to define the challenges that have the potential to be “show stoppers” for the application areas identified above.

**On-Chip Interconnect Difficult Challenges**

The continued decrease in feature size, increase in transistor count and expansion into 3D structures are presenting many difficult challenges in packaging of electronics. While challenges in continuous scaling are not addressed here, the difficult challenges of interconnect technology in devices with 3D structures are listed. The challenges of incorporating photonics on a non-photonic chip versus the benefits of doing so are not yet clear. There is a power requirement associated with E-to-O and O-to-E conversion that limits power savings for photonics when the distances are as short as on-chip connections. It is possible that on-chip interconnect will be all-electronic due to cost, switching

speed and reducing interconnect length benefits associated with 3D-TSV architectures. There is also the cost challenge of building very large photonic components using process technology capable of current and future electronic feature size. Photons in use today for integrated photonics are  $\sim 2\mu\text{m}$  while transistors are moving to single-digit nm.

The challenges addressed here assume that there is no optical interconnect on non-photonic chips. During the life of this roadmap new technologies may change the economic and power challenges. Potential solutions include on-chip photonics for electronic ICs based on the incorporation of sub-wavelength mechanisms for sending and receiving photon-based data, such as plasmonics and incoherent photon sources for on-chip data conversion from E to O. Potential solutions are known and will be addressed. Another potential solution is to use non-coherent photonic sources on-chip such as quantum dots which are modulated by plasmons to decrease cost, space requirements and resolve the issue of wavelength drift with temperature change.

### ***System Integration (Assembly) Difficult Challenges***

Today the term package assembly is used to describe the integration of heterogeneous components into a complex 3D system-in-package. This term does not clearly reflect that the activity is system integration and requires all the steps associated with developing and producing systems. This begins with product concept and must extend through co-design and simulation to final test.

Package assembly is often the limiting factor in performance, size, latency, power and cost. Although much progress has been made with the introduction of new packaging architectures and processes through innovations in wafer level packaging and system-in-package, a significantly higher rate of progress is required. The complexity of the challenge is increasing due to unique demands of heterogeneous integration of electronic/photonic circuits. This includes integration of diverse materials and diverse circuit fabric types into a single SiP architecture and the use of the 3rd dimension. Many of the problems are the same as those addressed in the on-chip difficult challenges section. The additional difficult challenges associated with electronic-photonic packaging are listed below.

1. **TSV Formation [Cost, Design, Process, Materials]** Aspect ratio (via-last) drives cost higher and the differential CTE causes local stress.
2. **TSV Operation [Reliability, Design, Materials]** “Cu pumping” out of the vias on thermal cycling. Thinner layers and reduced CTE differential will be needed.
3. **TSV Keep-out Area [Design, Materials, Process]** Circuit density and cost are impacted by large keep-out areas due to differential CTE and increased stress sensitivity for photonic components. New materials and lower processing temperature are needed.
4. **Physical Density of Bandwidth [Size, Bandwidth: Design, Process, Materials]** Single-mode WDM replacing multi-mode fiber/wave guides and integrated photonics chip supporting this capability on-package are needed.
5. **Low Cost Reliable Optical Connection to the Package [Design, Materials, Equipment, Processes]** Process, materials and equipment for alignment/placement and bonding process for “waveguide soldering” to make cost-effective and reliable connections to the package are needed.
6. **Low Cost Electronic-Photonic Package Substrates [Bandwidth, Waveguides, Design, Process, Materials]** Mechanical stability, thermal management, warpage control, photonic connections, electrical connections, integrated passive devices and other components will need to be accommodated. There are many candidates for package substrate material that satisfy some of these requirements including glass, silicon, organic and ceramic, but none of them satisfy all requirements. Silicon has the advantages of good CTE match, high electrical bandwidth, compatibility with optical waveguides and the wealth of experience, equipment and process technology from silicon IC fabrication that can be cost-effectively reused. Glass has many electrical advantages but has poor thermal conductivity. Organics lack mechanical stability. Ceramics are expensive and also have thermal management limitations. It is likely that more than one of these substrate types will see use, and the choice will be application specific.
7. **Thinned Wafers/Die at Low Cost [Design, Equipment, Materials, Process]** Today thinned die (Chapter 8 section 5) are typically processed to  $50\mu$  thickness, and at that thickness will be warped to a level that they cannot be stacked without a method for maintaining flatness (Chapter 8, section 4). Low-cost zero-residue adhesive and equipment to use it effectively in the thinning process will be required. Wafers in production will



be thinned to  $15\mu$  thickness and lower during the life of this Roadmap. Techniques that work are known today but are not cost effective.

8. **3D Stacking [Cost, Process, Bonding, Thermal Management]** The processes used today are complex, and can be simplified with some expensive steps removed to lower the cost and improve reliability. New materials and designs will be required for thermal management (Chapter 20). Low-temperature processing will be required to minimize built-in stress.
9. **Stacking Heterogeneous Components [Design, Materials, Process]** There may be applications where the lowest cost and highest performance will require stacking of Si circuits and compound semiconductor circuits in the same stack. Differences in CTE, stress sensitivity and mechanical/thermal properties present limitations that must be overcome. New designs and materials will be needed.
10. **Noise and Crosstalk in SiP [Design, Process, Materials]** The SiP products will contain RF and other components that have low-energy signals and logic that can draw high currents and impact the delivered power. Similarly, as we reduce the physical separation of components in 3 dimensions, crosstalk can prevent proper operation. Some of these problems will become increasingly difficult as we reduce operating voltage due to both smaller geometries and the desire to reduce  $CV^2$  energy requirements of the package. Designs that use optical signals where practical, and shielding where optics is not practical, will be required. New materials and processes will be required to manufacture these elements at low cost.

### ***System Test Difficult Challenges***

1. **Known Good Die [Design, Test Contacts, Materials, Process, Equipment]** The packaging of multiple die in the same package has relied upon known good die to ensure yield after assembly. This will not ensure reliability when transistors wear out, and VLSI ICs today do not produce known good die. When there are billions of transistors per IC and the geometries are measured in nano-meters, all die will have some defects. Intelligently designed redundancy can ensure a high yield of functioning die, as they have for memory circuits for years. The concepts and implementation of testing to ensure functioning die for logic is still a work in process. During the life of this roadmap, both electronic and photonic components will require intelligent redundancy and continuous test while running to ensure reliability of complex systems. Contactless methods for test point access are being investigated but are not yet practical.
2. **Testing Silicon Photonics Chips at Wafer/Panel Level [Design, Equipment, Materials]** Low cost production of Si Photonics will require manufacturing and testing of packages with a high degree of parallelism. Wafer-level packaging will require testing at wafer level to maintain cost. The design of low-cost test solutions for single-mode WDM photonics will be required. These solutions will be dependent on the co-design of the Si photonics chip, the test point contact and the test equipment itself.
3. **Low Cost Optical Test Access [Design, Materials, Process]** The incorporation of WDM single-mode photonic signals on a package will require the ability to test the connections after package assembly. New concepts are under consideration but a cost-effective solution does not exist. There will be design, materials and process changes to provide solutions.
4. **3D Stacking [Design, Testing, Testing Access, Process, Equipment]** Testing and test access will require new designs for test access of stacked components. New test equipment to cost-effectively test logic, memory, analog component, RF and passive devices in a single package will be required.
5. **Test Contactors for Contact Pads Below 5 Microns Diameter [New Contact Methods, New Materials, Design]** The test contactors in use today for electronics damage the pads they contact. This problem will be exacerbated as test pads are driven to thinner metal and sub-micron geometries. New test methods, new contact methods and new access design will be required; all must be low cost.
6. **SiP Reliability [Design, Testing, Thermal Management]** The more difficult challenges are associated with testing in a world where transistors wear out. We will have no known-good die, traditional test access points will not exist, and thermal management will be difficult when areal thermal density is increased by a multiple determined by the number of layers in a stack. These will all require solutions. Innovation in design, materials and test strategy will be required to meet these challenges. New processes and materials will be needed; built-in self-test, continuous test while running, intelligent redundancy and dynamic self-repair will be part of the solution. New materials and modifications to equipment will be required.



7. **Ensuring System Reliability for Electronic/Photonic SiP-based Systems [Design, Software, Fault Localization]** The potential for a single-point fault that prevents operation of data communication and analysis systems does not meet market requirements. There are two paths to reduce the probability of a system-level shut-down due to a single-point failure. One is the use of intelligent redundancy which is identified above. The second is a system capable of quickly obtaining the physical location of a fault during the product qualification process so that revisions can be made to the design to remove or reduce the weak points in the system. The design of such capability for individual electronic integrated circuits has been explored for several years. Extending this capability to cover photonic components in a complex 3D Heterogeneous SiP is a very large task but may become a requirement to contain the cost of excess redundancy in these systems.
8. **Enabling the Software Defined Networks (SDNs) with Real Time Testing [Design, Software]** The diverse needs of users connected to the global network for access to the cloud will require SDN capability. This will not be practical unless the network hardware and software are configured to enable SDNs. This enablement will require low-latency switching to set up the network and test capability to ensure that it is functioning correctly when set up and is reliable during operation. The test challenge will require test resources at various points in the network that involve SiP incorporating FPGA technology.

**Difficult Challenges by Circuit Fabric**

1. **Logic:** Hot spot locations not predictable, high thermal density, high frequency, unpredictable work load, limited by data bandwidth and data bottle-necks. High-bandwidth data access will require new solutions to physical density of bandwidth.
2. **Memory:** Thermal density depends on memory type, and thermal density differences drive changes in package architecture and materials, thinned device fault models, test, and redundancy repair techniques. Packaging must support low latency, high bandwidth, large (>1Tb) memory in a hierarchical architecture in a single package and/or SiP. Memory will have multiple circuit fabric types for various applications and each will have differences in packaging challenges.
3. **MEMS:** There is a virtually unlimited set of requirements: hermetic, non-hermetic, variable functional density, plumbing, stress control, and cost-effective test solutions.
4. **Photonics:** Extreme sensitivity to thermal changes, O-to-E and E-to-O, optical signal connections, new materials, new assembly techniques, new alignment and test techniques.
5. **Plasmonics:** Requirements are yet to be determined, but they will be different from other circuit types. There is a section following that addresses this emerging technology.
6. **Micro-fluidics:** Sealing, thermal management and flow control must be incorporated into the package.

There are many other components that will be integrated into SiP for electronic-photonic systems. Some of them are listed in table 1.

*Table 1. Components integrated into electronic-photonic systems*

<p>Components that will be assembled into complex 3D-SiPs may include:</p> <ul style="list-style-type: none"> <li>• Monolithic photonic ICs (incorporating photonics, electronics and plasmonics)</li> <li>• Other discrete optical components that are not integrated in the Silicon/photonic integrated circuits (SiPh-ICs).</li> <li>• Si based logic and memory ICs</li> <li>• MEMS devices</li> <li>• Sensors (including a growing list of photonic sensors)</li> <li>• GaN power controller circuits</li> <li>• RF circuits</li> <li>• Compound (direct bandgap) semiconductor lasers</li> <li>• Optical interconnects to and from the outside world</li> <li>• Electrical interconnects to and from the outside world</li> <li>• Passive components (including integrated passive devices)</li> <li>• New devices and new materials that will enter the area over the life of this Roadmap.</li> </ul>
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Most if not all of these will require new materials, new processes and new equipment for package assembly and test to meet the 15-year Roadmap requirements for electronic/photonic systems.

***Difficult Challenges by Material*** (more detail can be found in Chapter 15, Materials and Emerging Research Materials)

1. **Semiconductors:** Today the vast majority of semiconductor components are silicon-based. In the future both organic and compound semiconductors will be used with a variety of thermal, mechanical and electrical properties, each with unique mechanical, thermal and electrical packaging requirements. Photonics and power management ICs will incorporate compound semiconductors with different thermal and mechanical properties.
2. **Conductors:** Cu has replaced Au and Al in many applications but this is not good enough for future needs. Metal matrix composites and 2D ballistic conductors will be required. Inserting some of these new materials will require new assembly, contacting and joining techniques.
3. **Dielectrics:** New high-k dielectrics and low-k dielectrics will be required. Fracture toughness and interfacial adhesion will be the key parameters. Packaging must provide protection for these fragile materials.
4. **Molding compound:** Improved thermal conductivity, thinner layers and lower CTE are key requirements.
5. **Adhesives:** Die attach materials, flexible conductors and residue-free adhesives needed do not exist today.

***Package Substrates for electronic-photonic systems***

The dominant package substrate today uses organic laminate materials with limitations in mechanical stability, large CTE differential with silicon and limited wiring density. Today there are four different classes of material competing to be the package substrate of choice. They are:

1. **Organic laminates**  
Organics have the lowest cost but have limitations in lack of mechanical stability, limited thermal conductivity and a large differential CTE with semiconductors. This material accommodates embedded active and passive components much easier than any other package substrate material. Composites of organic laminates are continuing to make progress but do not meet future needs for photonic packaging. It is the solution of choice for single and multichip CMOS packages.
2. **Low temperature co-fired ceramics (LTCC)**  
This material has excellent mechanical stability, acceptable CTE match with semiconductors and good thermal conductivity, but has limitations in wiring density, I/O pitch and cost. It is the solution of choice for harsh environments.
3. **Glass**  
This material has advantages in high breakdown field strength; it is a true insulator, which means essentially no leakage current and no variable capacitance. It does not match the bandwidth density of silicon and it has the worst thermal conductivity of candidate materials. There are several applications with low thermal density for which glass may eventually be the material of choice. There is a concerted effort to develop glass interposer technology for selected applications and it is likely that there will be high-volume applications in the future where thermal density is not high. An example of the production flow for through-glass vias (TGVs) is shown in Figure 3 below.

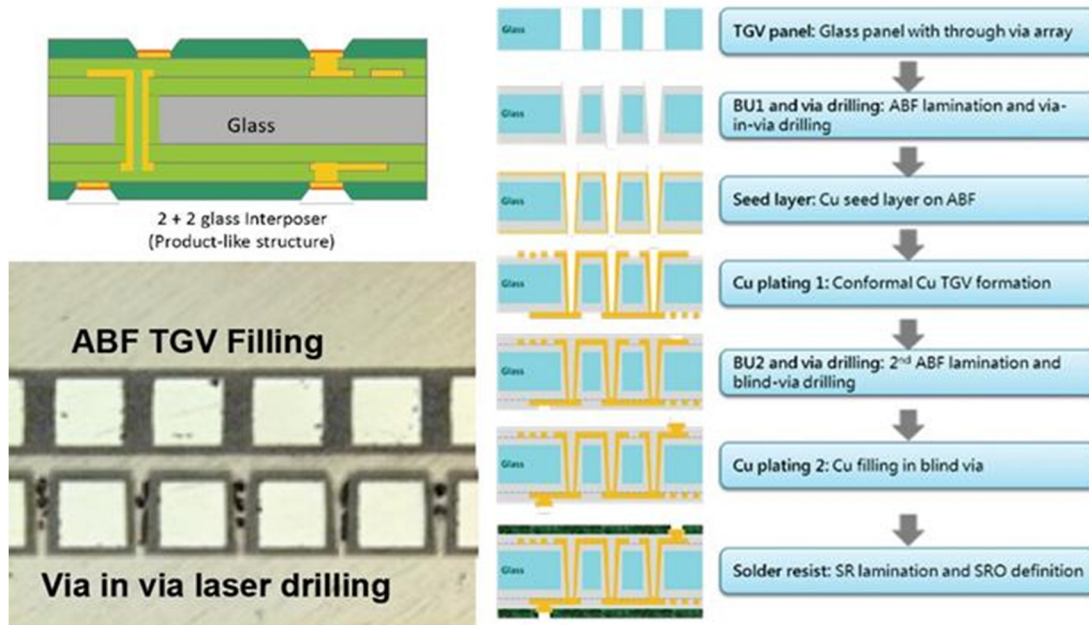


Figure 3. Glass TGV package substrate process flow

#### 4. Silicon

Silicon has excellent CTE match, excellent mechanical stability and the best wiring density. Its limitation is in cost. On a total cost per bandwidth basis, this limitation should be resolved as we come down the learning curve. It has better thermal conductivity than other substrate materials with the exception of some of the LTCC materials. It also has the limitation of a being a semiconductor, which means variable capacitance and lower breakdown field strength. It is rapidly becoming the solution of choice for package substrates with very high bandwidth requirements, and it is the mainstay of the 2.5D integration currently in volume use for FPGAs.

The introduction of the silicon interposer has changed the package substrate for the most advanced packaging to silicon. This technology has been known for many years but was not adopted due to high cost. At the leading edge, the interconnect density available using obsolete manufacturing equipment for 90-65nm-node ICs became cost effective for very high bandwidth interconnect. Silicon has the further advantage of embedding optical waveguides into the silicon substrate for heterogeneous integration of photonics, electronics and plasmonics into a single package. There are 2 tables following that address the silicon package substrates and the organic package substrates. There are no tables included for the other package substrate types since at present the other two seem to be limited to lower volume specialty packages.

In some cases, based on warpage considerations and/or minimum pitch on a system-level printed circuit board where the package is to be mounted, a combination of both a silicon substrate (interposer) and an organic package substrate are employed between the active devices; the silicon interposer may be mounted on a lower-cost organic-package substrate with a larger pad pitch. Figure 4 illustrates this architecture, which is in high volume production today. Note that it does not contain any photonic elements. Prototypes of electronic-photonic interposers have been demonstrated but many challenges are yet to be resolved before this technology will appear in high-volume products.

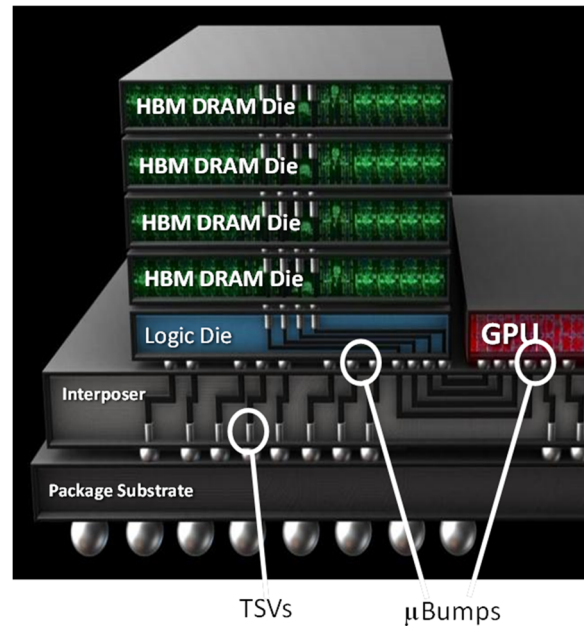


Figure 4. 3D-SiP Package using Silicon Interposer and Organic Package Substrate

The example above illustrates the use of a silicon interposer as a substrate for logic, memory and a graphics processor connected by  $\mu$ bumps to the interposer. The organic package substrate is joined to the interposer through silicon vias (TSVs) with solder balls. The entire image constitutes a ball grid array (BGA) package with large solder balls on the bottom for connection to a system-level printed circuit board. This product is the Fiji graphics processor from AMD and the package is in high-volume production today. It represents the state of the art for 3D SiP packaging in 2015. This architecture is in high volume today and will continue to expand bandwidth through tighter pitch, wider buss structures, with some increase in frequency. Higher frequencies are possible with electronics but the power penalty is large.

The requirements for decreases in power and increases in physical density of bandwidth can only be resolved through incorporation of photonic interconnects in the package and, ideally, on logic and memory circuits. For these applications, coherence may not be required and photon sources other than lasers may be used. This use of emerging technology such as microLEDs and quantum dot sources may avoid the space and energy costs of O-to-E and E-to-O conversions on chip.

The Roadmap assumes that there will be no need for significant changes in geometries for this category since the first level of I/O count reduction and pitch translation will take place on the silicon interposer. The addition of photonic components may be embedded or may be mounted to the package substrate surface.

#### ***Replacements for the CMOS Switch will be Incorporated in 3D-SiP Electronic-Photonic Packages***

The range of devices and subsystems in 3D SiP with Heterogeneous Integration includes a wide variety of system components with varied packaging requirements. The variety will continue to expand over the life of this Roadmap as new devices and materials with improved characteristics for specific functions are introduced and the use of 3D-SiP architectures expand to maintain the pace of progress as Moore's Law scaling continues to slow.

Silicon integrated circuits have now been demonstrated with single-digit nanometer geometries. The materials, equipment and processes available have enabled transistors that are near the limit of the physics. This continued scaling has not delivered the cost, power and performance improvements enjoyed historically through Moore's Law scaling. The ultimate demise of further scaling is an economic question rather than a technology limitation. When the cost of delivering a unit of performance is greater as we scale to lower geometries, then scaling will stop. Many believe we are at that point today. This is a driving force to replace the silicon CMOS switch, and there are several candidate materials and device architectures. The paragraphs below show a number of devices made with materials that are candidates to replace silicon. This subject is discussed in more detail in Chapter 16 (Emerging Research Devices).

By adding black phosphorous over silicon, researchers at the University of Minnesota were able to achieve the on-chip detection performance level of germanium-based optical circuits. This high level of performance occurs because a layer of 2-D black phosphorous significantly increases the optical circuits' interaction with light due to its narrow but finite band gap.

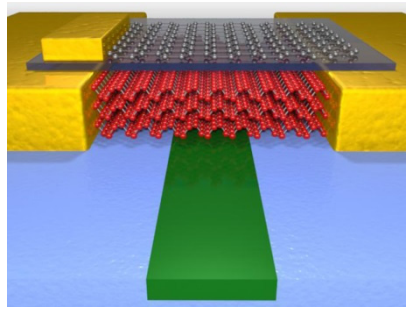


Figure 5. Black Phosphorous on silicon.

Illustration from University of Minnesota College of Science and Engineering

Efforts continue to maintain the benefits of scaling. This example from IBM’s T.J. Watson Research Center has reported scaling the 1.8 nanometer node and beyond to the angstrom level eventually. It uses the same extreme-ultraviolet (EUV) lithography CMOS process technologies already in place. They identify the main issue for scaling being the contact rather than the ability to scale active area geometry.

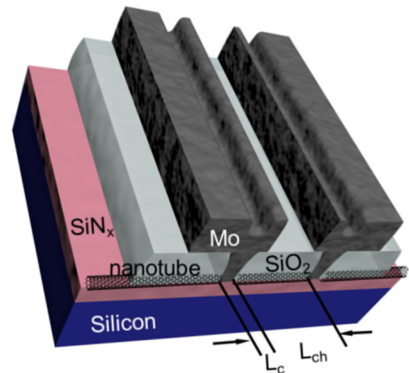


Figure 6. Nanotube transistor schematic with contact length <10nm.

Source: EE Times

The list of two-dimensional semiconductors with properties that are being investigated for replacing the CMOS switch is growing (see Chapter 16). This is relevant for packaging since packaging requirements may be different for each one. As these options are developed, we will need to update the Roadmap to incorporate those new devices and materials that are successful. Some of these materials already have the ability to generate and sense photons.

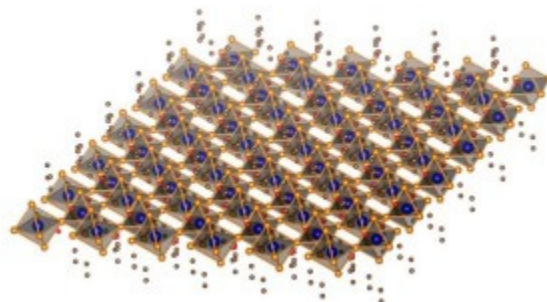


Figure 7. Structural illustration of a single layer of a 2D hybrid perovskite  $(C_4H_9NH_3)_2PbBr_4$

Today the list includes:

- Carbon nanotubes
- Graphene
- Black phosphorous
- Molybdenum ditelluride
- Molybdenum disulfide
- 2D perovskites
- Boron nitride

## Emerging Technologies for future Electronic-Photonic Products

### *Plasmonics in Electronic – Photonic Integration*

This section reviews opportunities afforded by using plasmonic technologies in next-generation circuits to replace the wiring system that distributes clock and other signals to the various functional blocks of a CMOS integrated circuit. This section also describes how plasmonic technology can complement and eventually replace existing Si Photonics technologies that are used in System-in-a-Package (SiP) architectures. Potential roadblocks that may impede these implementations will also be reviewed. Existing capabilities and expected performance improvements by adopting plasmonics will be discussed. In addition, the expected dates of availability for the various milestones for incorporating plasmonics will also be listed.

#### *Introduction to Plasmonic Devices*

Optoelectronics interconnects, which are based on Si-photonics, were developed to circumvent bottlenecks that relate to power consumption, functionality, packing density and speed of electronic interconnects, initially for data centers and high-performance computing. Today they are reaching the printed circuit board level and, for future generations of VLSI, they will be at the package level and eventually on integrated circuits. They have made undeniable contributions towards these aims. However, the footprint associated with such devices, when normalized to their functionality, leaves room for substantial improvement, especially when compared to the footprint associated with electronic devices.

In existing versions of Si photonics there are limitations dictated by diffraction in the transverse direction and by wave-matter interaction in the longitudinal direction, which hinder the miniaturization of Si-based interconnects. At present, average dimensions of such devices are on the order of 100s to 1000s of micrometers<sup>2</sup> in area per device, while transceivers require millimeters<sup>2</sup> in area (depending on the modulation format).

Emerging data communication applications require much denser integration of optoelectronic devices within electronic circuits compared to what existing Si-based interconnects can provide, despite the extensive systems-in-package approaches. For an alternative approach to be viable in next-generation circuits, thereby eliminating/alleviating the need for 3D integration, true athermal operation, with substantial device miniaturization and improved energy efficiency of existing optoelectronic transceivers, are mandatory for meeting the required specifications. New optical materials and architectures that can deliver the necessary leap in performance need to be developed.

Surface plasmon polaritons (SPP) are quasi-two-dimensional surface electromagnetic waves that propagate along dielectric-metal interfaces with field components decaying exponentially into both media. Field penetration into the dielectric typically ranges between 100s to 1000s of nanometers, while confinement in the metal is limited to tens of nanometers and is determined by its skin depth. These attributes have inspired significant research effort pertinent to nano-scale plasmonic effects and devices for applications such as sub-wavelength waveguiding, modulation and detection. One of the prominent properties of plasmonics has to do with the complex permittivity of metals in the optical frequency regime, which results in small skin depths and significant absorption losses. This leads to a strict trade-off between propagation length and modal field confinement.

Many techniques and design methodologies have been proposed and deployed to reduce losses in plasmonic waveguides. One approach attempts to use a gain medium to compensate for the losses. This method is impractical due to the high current densities involved and large waveguide dimensions required. The other approach reduces the attenuation by reducing the mode field overlap with the metal at the cost of reducing the field confinement. Truly low propagation loss can be achieved using this route; however, this comes at the cost of larger waveguide dimensions with micron-scale mode areas that are often larger than those of single mode Si-based dielectric waveguides.

Recent developments have almost eliminated these trade-offs and managed to demonstrate losses in the 10s of dBs/cm for plasmonic waveguide with mode areas smaller than existing Si-based waveguides. These modes are called hybrid plasmonic waveguides, with the field engineered across the metal layers to achieve symmetry. Using this approach, devices that rival and outperform their Si counterparts are now a reality. These will likely require one to two orders of magnitude less area.

Given the recent developments and current state of the art in the field of plasmonic devices, it is imperative for us to examine what exactly would be gained by migrating to this platform from the well-established Si-based photonics. The advantages offered by plasmonics relative to other solutions for these functions are reviewed below.

#### *What Superior Features Can be Introduced using Plasmonic Device Technologies?*

The following proven plasmonic attributes have been demonstrated and they highlight how plasmonics can be used to develop the next-generation optoelectronic transceiver devices on CMOS. It is important to note that



plasmonic devices in this context will only be used to implement the functional devices, while all-dielectric waveguides will continue to be used as linking conduits between the modules communicating through light on chip.

**Athermal capabilities:** Current modulator and detector designs using a hybrid plasmonic device offer non-resonant operation with optical bandwidth of operation exceeding 100s of nanometers. This in turn offers a tolerance in the temperature swing while operating within specs exceeding 150 degrees C. Current filters using plasmonics, however, do use resonant structures and may pose some limitations.

**Bandwidth of operation:** The electrical bandwidth of a hybrid plasmonic device is dictated predominantly by the device capacitance/resistance. Transceivers that are based on On-Off keying (amplitude modulation), which is predominant for this mode of communication, require device sizes on the order of 1  $\mu\text{m}$ . As such, the inherent BW of operation exceeds 100s of GHz. When the need arises for a transceiver's coherent communication modalities, the device sizes will increase but remain in the 10s of micrometers scale.

**Wavelength of operation:** Hybrid plasmonic devices do not rely on Si for operation. They use an array of CMOS-compatible materials such as poly-Si and 2D materials. As such, the wavelength of operation is not limited to the regimes where Si photonics performs within specs. Operation in the IR regime is possible via the use of 2D materials such as Phosphorene. Operation in the visible band is possible by using materials other than Si.

**Packing density and Photonics VLSI comparable to electronic VLSI:** Given that hybrid plasmonic devices require dimensions which are at least a factor of 50 smaller than their Si counterparts, the packing density of functional devices using this technology will provide much more effective utilization of the Si real-estate when implemented on the VLSI platform. In addition, the ability to place individual devices closer together when compared to Si is afforded by the tight field confinement offered by hybrid plasmonic architectures.

**Role of 2D materials:** The architectures of the best performing hybrid plasmonic devices can be significantly enhanced with judicious design to optimally utilize 2D materials. This is due to their ability to concentrate the optical modes in an even smaller cross-sectional area when compared to plasmonic devices using conventional materials.

**Power consumption:** Given the modulation approaches deployed in hybrid plasmonic devices, it is projected that power per bit (for modulation only) will not exceed 1-5 fJ. However, the detectors implemented using this technique will prove to be more power hungry. The contribution of power by the various transceiver elements, and the fact that it will be dominated by the receiver in optical transceivers, will still remain the same for plasmonics as is currently the case with Si photonics; however, the overall power consumption is expected to be reduced by a factor of 10.

More importantly, given the truly athermal nature of this architecture, the power and real-estate required for the entire control circuit, heaters and tracking circuits will no longer be needed, eliminating accordingly a substantial portion of the exiting transceiver power budget.

**Insertion losses:** In order to have a truly improved power budget, the insertion loss of plasmonic-based devices needs to match or be better than those of existing devices. This is a challenge given the size mismatch between the sizes of such devices and the waveguides which will transport the light signal between modules. The insertion losses included the In/Out Coupling as well as the propagation losses inside the devices, to reduce total power budget.

The propagation losses can be misleading due to the excessively high losses associated with plasmonic structures. However, on the other side, as can be seen in Table 4, the length-scales over which devices are implemented, and the insertion length of such devices, with appropriate design, can be made less than those incurred by Si devices. Recent research has reduced the broadband low insertion losses of these devices below  $\sim 2$  dB per junction.



Table 4. Attributes of device technologies showing superior plasmonic performance.

	Cross-section [nm <sup>2</sup> ]	$n_{eff}$	$\gamma$ [dB/ $\mu$ m]	mode area [ $\mu$ m <sup>2</sup> ]	FOM
Plasmonic slot waveguide [34]	50 × 340	1.43	0.609	0.05	13.0
LRSPS strip	20 × 775	3.49	0.025	3.5	37.9
Hybrid plasmonic waveguide	200 × 492	1.26	0.068	0.23	54.4
Hybrid plasmonic strip waveguide [38]	200 × 2100	1.59	0.024	0.23	154.4
Asymmetric dual-hybrid waveguide [36]	200 × 520	1.60	0.025	0.23	147.8
Asymmetric hybrid-SPP waveguide	200 × 434	1.81	0.021	0.15	220.1

### Summary of Plasmonic section

In the medium term, plasmonic technologies can improve the size, power consumption, yield, packing density, range of wavelength of operation, electrical bandwidth and capacity of photonics in VLSI. For the longer term, plasmonics can replace Si photonics in SiP architectures. Given the possibilities plasmonics afford, they may also shape the future generations of SiP by integrating a larger portion of the photonics devices on the same VLSI die with no need for SOI.

### Manufacturing Challenges Associated with Plasmonics Device Technologies

The following are the known challenges involved in incorporating plasmonic devices.

Table 5: Summary of the expected materials/packaging requirements for plasmonics.

Issue / topic	Summary	Actions to address the issue
Device fabrication (hybrid plasmonic architectures) using standard CMOS processes	While the materials required for the plasmonic device discussed here are all CMOS compatible, the order, thicknesses and stress involved needs to development in order to ensure the compatibility with the fabrication	Process development for basic building transceiver blocks is necessary.
Stress management to maintaining layer and interface integrity for plasmonic device architectures	Thin layers of contact metals are required for these plasmonic devices as some of them are three and four terminal devices.	Development of layer deposition processes and electrical contact formation technologies to ensure the operation of these devices within specifications within a CMOS work flow is essential.
Interfaces with other photonics components such as dielectric waveguides for transport	Architectures with optical interfaces that are compatible with existing and future optical transport waveguides can be a challenge.	Design and co-simulation of both classes of devices (plasmonic devices and conventional Si waveguides/devices) is needed.
Interface with electronic devices.	Architectures with electrical interfaces that are compatible with existing and future electronic devices can be a challenge.	Design and co-simulation of both classes of devices is needed.

LED	Equ.	Modulation	Data rate	receiver	distance	institution	Data source
White light	Pre	OOK-NRZ	40Mbit/s	PIN	2m	Oxford University	PTL2008
White light	-	OOK-NRZ	100Mbit/s	APD	3m	Nakagawa Laboratories	OEPT2009
Blue light	-	DMT-QAM	200Mbit/s	PIN	2m	Fraunhofer HHI	PTL2009
RGB LED	-	DMT-WDM	803Mb/s	APD	12cm	Fraunhofer HHI	OFC2011
White light	Post	CAP	1.1Gb/s	PIN	23cm	National Chiao Tung University	PTL2012
RGB LED	-	DMT	3.4Gb/s	APD	10cm	Scuola Superiore Sant'Anna	OPEX2013
RGB LED	Post	SC-FDE	3.75Gb/s	APD	1cm	Fudan University	COL2013
Micro-LED	Pre/Post	HW OFDM	3 Gb/s	APD	5cm	Edinburgh University	PTL2014
RGB LED	Pre/Post	SC-FDE	4.22Gb/s	APD	10cm	Fudan University	OPEX2014
RGBY LED	Pre/Post	DMT	5.6Gb/s	PIN	1.5m	Scuola Superiore Sant'Anna	ECOC2014
RGB LED	Pre/Post	CAP	4.5Gb/s	PIN	2m	Fudan University	PJ2015
RGBY LED	Pre/Post	CAP	8Gb/s	PIN	1m	Fudan University	PJ2015
RGBY LED	Pre/Post	CAP	9.5Gb/s	PIN	1m	Fudan University	Globecom2015
RGB micro	post	DMT	10.4Gb/s	PIN	1m	Oxford University	PTL2016

**Design tools for silicon photonics are available today and expanding rapidly**

AIM Photonics announced a Process Design Kit and multi-project wafer available in October of 2018. They also announced the addition of laser and CMOS integration with a silicon interposer.

**Integration Processes**

Cost reduction depends on reducing the amount of material used, reducing process steps, increasing the parallelism in the manufacturing process and improving yield. Each of these factors is addressed below.

**Reducing the Amount of Material Used**

As we move everything closer together, the volume of material used is automatically reduced. Improving the conductivity of the interconnect material reduces the amount of conductor required. Thinner layers for all materials in the package from the substrate to the encapsulant reduce the amount of material used. New materials with improved electrical, mechanical and photonic properties will allow these reductions in layer thickness without compromising quality. The packaging industry has been doing this for several years and it is working but there is much more to be done. Currently silicon products are shipping at 50µm thickness, and layer thickness for the extreme case of built-in memory has already reached a thickness of less than 10 µm.

**Reducing Process Steps**

The current standard practice is to use underfill materials to improve the reliability of copper solder balls and pillars by improving the rigidity and strength of the electrical connection. The technology is available today to allow underfill to be removed, thereby reducing the materials use and the number of steps in the process while improving reliability relative to the underfill process. The process flow is the following:

- Use a direct interconnect bonding process from Experi, which results in bonding at temperatures as low as 100°C for both the copper and the surrounding insulator. This distributes the interfacial adhesion across a higher percentage of the surface.
- Use composite copper to reduce the CTE differential between copper and the semiconductor material.
- Assemble other layers in the package and attach to the system printed circuit board with copper nano-solder.

The result is reduced material use, reduced number of process steps, joining at use-case temperature of ~150°C to minimize stress, and increasing the area of interfacial adhesion for improved reliability.

## Photonic components such as sensors, emitters, modulators, multiplexers, demultiplexers

Photonic components may be sensors, emitters, modulators, multiplexers and demultiplexers. The challenges and potential solutions for these components over the next 15 years are covered in the sections below.

### Photonic Sensors

Research and development for optical sensors is progressing rapidly, with 4 categories of sensors listed below that have different packaging requirements.

- Spectroscopy based
- Capture based (functionalized capture surfaces or volumes)
- Gas based detection (atmospheric and other gases)
- Liquid based
- Energy based

The technology of the sensors will be discussed in more detail in Chapter 11 of the Roadmap. This chapter will only address the packaging requirements. The R&D systems in use today are still in the bench-top prototype phase as shown in Figure 8.

## Integration of microfluidics and temperature control

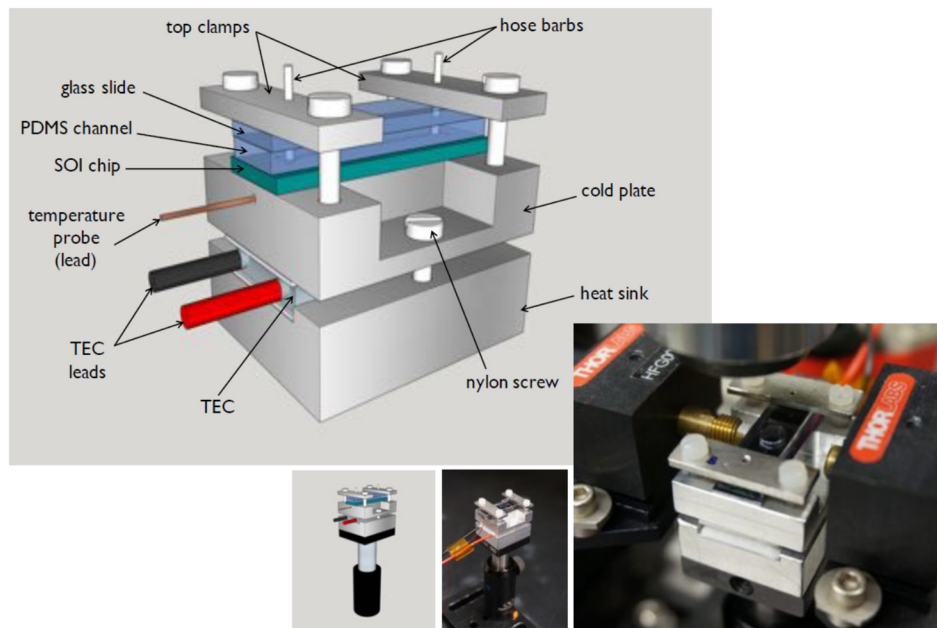


Figure 8. Fluidics sensor with temperature control used in R&D today<sup>2</sup>

This technology can be converted into a PIC chip using the processing techniques used in manufacturing of MEMS devices today. The challenge will be with the photonic connection to the package and the fluid connection to the sample source, along with the cost and reliability required in the application. The most probable solution for the photon source is to fabricate the lasers needed on the PIC chip as illustrated in Figure 9.

<sup>2</sup> “Making good on our promises: Optical sensing from the lab to the real world”, Benjamin L. Miller, Departments of Dermatology, Biochemistry and Biophysics, and Biomedical Engineering, University of Rochester

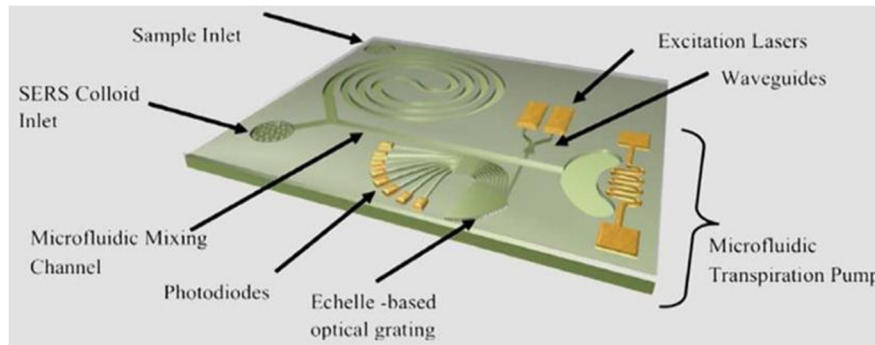


Figure 9. Photonic microfluidic-based sensor on a PIC chip with no off-chip optical connection

The packaging of fiber optics initially was very simple, consisting of a laser diode (a photon emitter), a fiber and a photo diode (a photon sensor). These elements will be replaced during the 15-year lifetime of this edition of the HIR with replacement sensors and emitters that are smaller, lower noise, stable with temperature change, more energy-efficient and lower in cost. There had been no motivation to integrate, and the introduction of wavelength-division multiplexing (WDM) did little to change this since the transmit lasers were all on a different line card.

The typical laser diode packaging used in Telecom is shown in Figure 10.

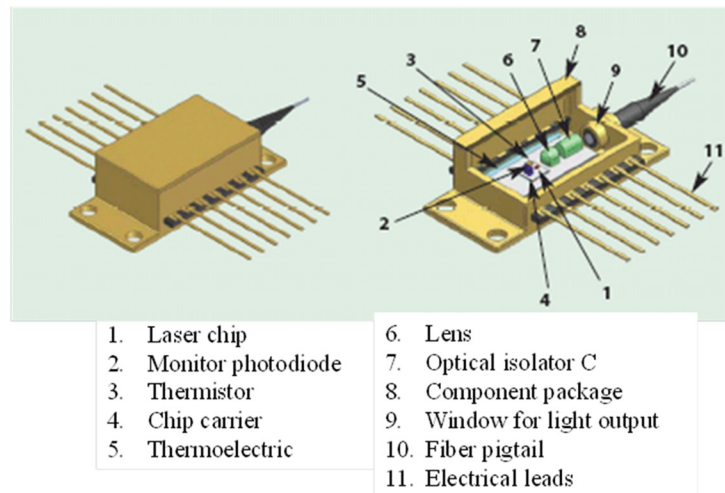


Figure 10. Butterfly laser package used in long haul telecom

The problem with this technology is evident from the figure. There are expensive components (gold), there is a high assembly parts-count and it is very large in size. This approach is too expensive and too large to meet the requirements of low-cost photonic systems.

The introduction of 100G Datacom has dramatically changed the situation, since this requires multiple optical components in a small module which requires PIC integration. An example is shown in Figure 11.

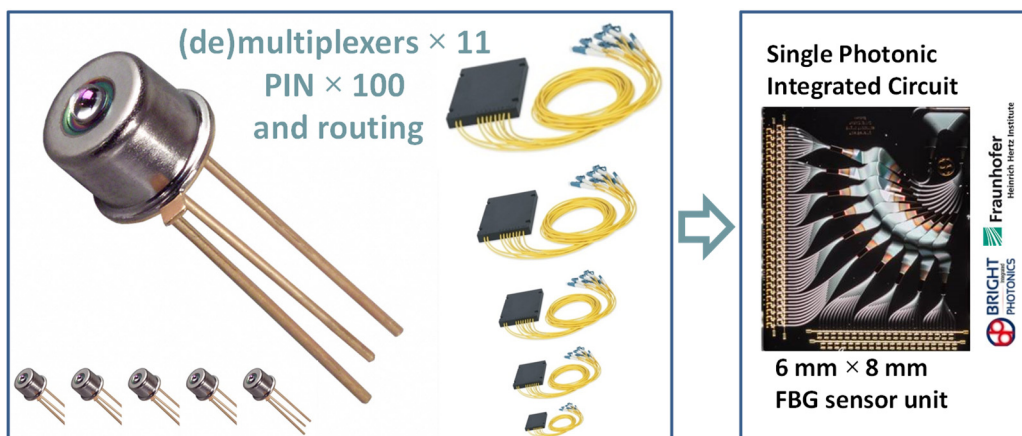


Figure 11. A Photonic Integrated Circuit combining multiple components (Source: Fraunhofer Institute)



This PIC enables smaller size, lower power and lower cost, and it is available for use as a component of the 3D-Heterogeneous SiPs that will emerge during the lifetime of this Roadmap. Combining photonics and electronics in SiP products addresses the critical performance issues for the industry. Today there are many alternatives in use as stand-alone diodes for either emitters or sensors in electronic/photonic SiP. The explosive growth in demand, driven largely by consumer products, has stimulated investment in smaller form factors, lower cost, and lower power.

Figure 12 shows the current state of the art for Photonic/Electronic 3D SiPs in cell phone camera systems. The figure is representative of what is already installed in many high-end consumer products. Future evolution of this technology will support increased functional density (small size and weight with improved performance) and continue cost reduction at a rate equal to or greater than that of Moore’s law.

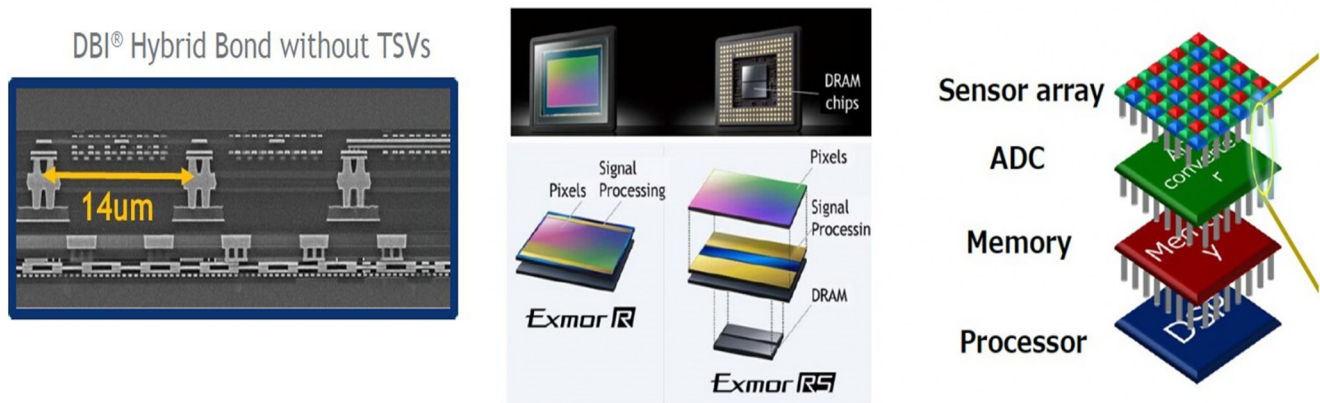


Figure 12. Photonic/Electronic SiP camera system in Galaxy S7

There are many limitations for integration of photonics into complex SiP based systems. The major limitations and potential solutions are shown in Figure 13.

- ✓ Higher bandwidth density
- WDM single mode Photonics to the package**
- ✓ Lower latency
- Flat photonic network- replace tree architecture**
- ✓ Increased data processing speed
- Increased parallelism- more cores & software to match**
- ✓ Expanded data storage
- 3D memory, expanded bus width, hierarchical architecture**
- ✓ Ensured reliability in a world where transistors wear out
- Intelligent redundancy**
- Continuous test while running**
- Dynamic self repair**
- Graceful degradation**
- ✓ Improved security while maintaining process speed and latency
- Hardware and software combined-distributed over the global network**

Figure 13. Potential Solutions to Support the Photonic/Electronic Roadmap of the Future

**Integrating these components into subsystems and systems**

Integration of photonic components into a sub-system or system may require accommodation of diverse materials including Si, InP, GaAs, and SiN with differences in fracture toughness and CTE. The interconnect for photonic systems has to achieve low cost with low losses (less than 1dB per connection) and high bandwidth density, which may require 10s of WDM channels. There is the further limitation already mentioned of wavelength drift with temperature change using laser diodes along with up to 1THz electrical interconnects which represent high thermal density sources.

The complexity of today’s system integration processes is such that the assembly (packaging) and test are the majority of total device cost.

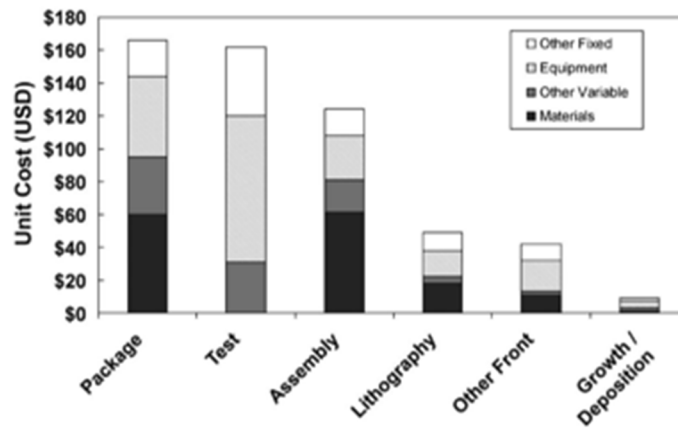


Figure 14. Cost breakdown for an InP photonic device, showing the majority of product cost (> 80%) can be attributed to packaging and test.<sup>3</sup>

Integration is already combining PIC chips with existing electronic components into a single assembly (package) to reduce cost and size while improving performance. Figure 15 is exemplary of that approach, combining a Rockley PIC switch with an electronic switch ASIC into a single package.

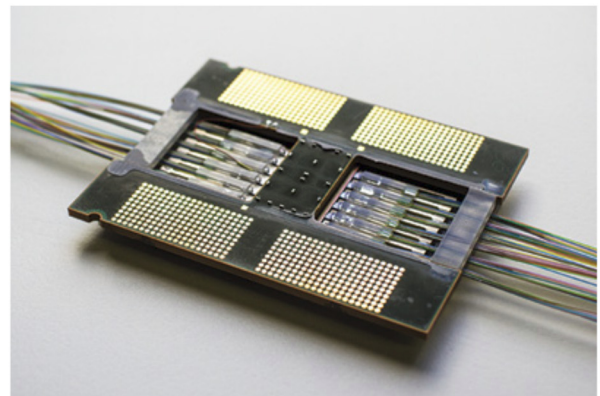
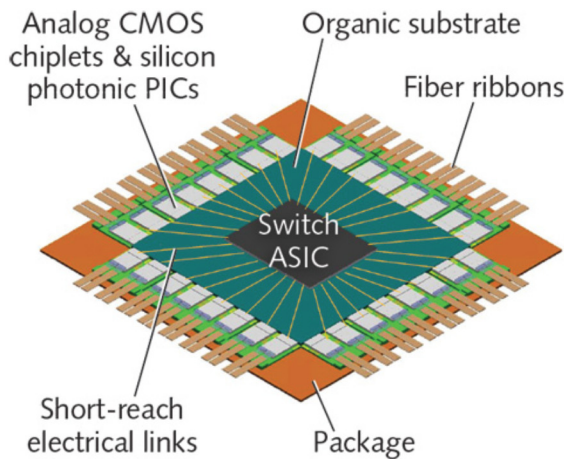


Figure 15. PIC combined with electronic switch into a single assembly (package)

## Selected Applications for Photonics

### Visible light Communications

High bandwidth, low power data communication at low cost using LEDs has been known for some time but has not yet seen broad adoption. The state of the art was reported by Nan Chi in PGC July 2017 shown in figure X below. Additional progress using beam steering with multiple beams may find applications for internal office communication such as projecting 5G into internal office spaces that cannot receive the 5G signals directly.

### The global network

An example of the impact of combining new packaging architectures with state-of-the-art components is illustrated in the work of Ronald Luitjen of IBM in rethinking the server. Using conventional packaging techniques, he was able to produce a micro-server in a single board with all the components other than memory, reducing board area by an order of magnitude and volume by a greater number. The addition of 3D integration in a SiP architecture enables adding the required memory while reducing area by an additional factor of 7 and further reducing the volume. The result is lower power, high bandwidth, smaller size, and higher logic performance as illustrated in Figure 16.

<sup>3</sup> “Process-Based Cost Modeling of Photonics Manufacture: The Cost Competitiveness of Monolithic Integration of a 1550-nm DFB Laser and an Electroabsorptive Modulator on an InP Platform”, IEEE Journal of Lightwave Technology, Vol. 24, No. 8, 2006.

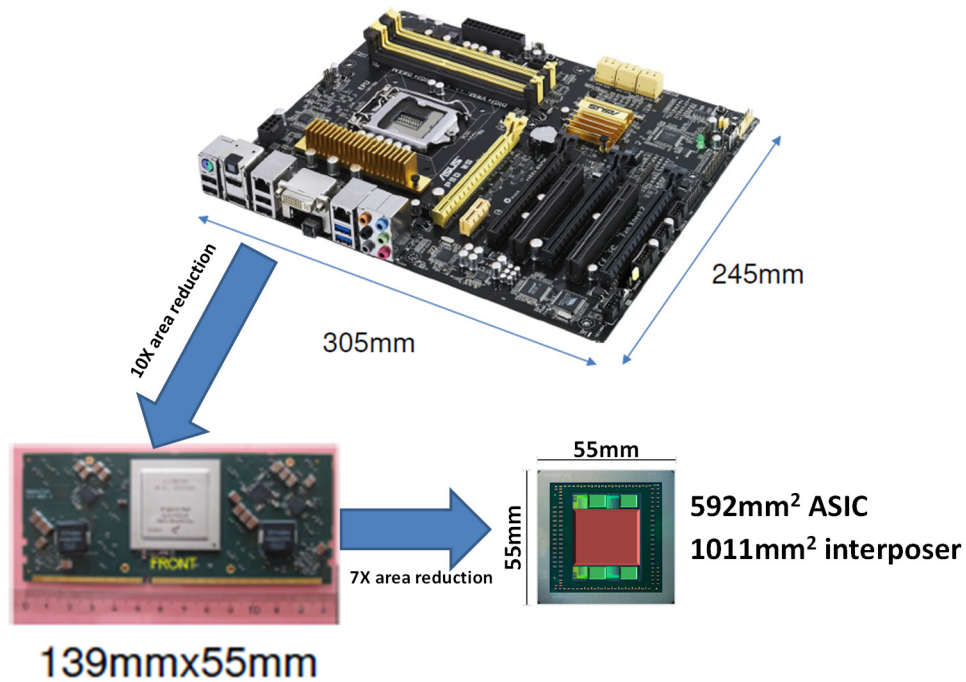


Figure 16. Micro-server size and power reduction using 3D integration

The migration from the current server to the 3D SiP  $\mu$ server can reduce area by 70X and volume by an even greater amount. This results in lower power, higher performance and eventually lower cost as high volume allows investment in automation. The next logical step is to add a photonic layer to the package to further reduce power and latency.

The current state of the art for photonics, approaching the transistors, is illustrated in Figure 17, with optical engines on cards with optical interconnects to the outside world and electrical interconnects to the packages mounted on the card.

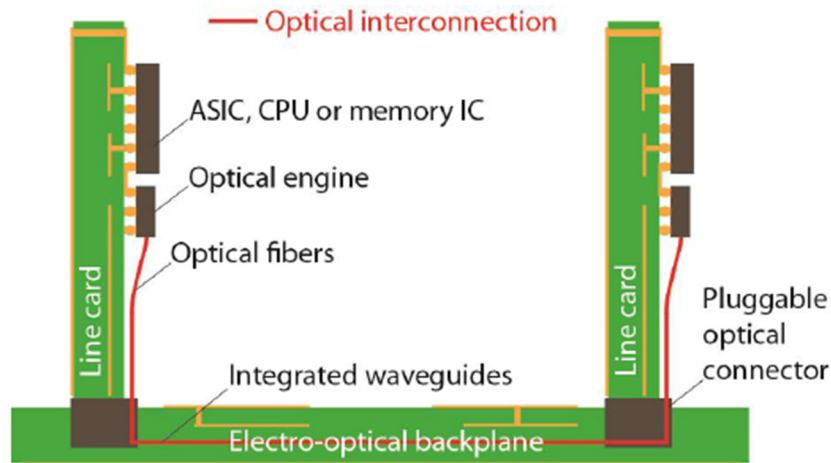


Figure 17. State of the Art for photonics, close to transistors in 2016

The server or high-performance computer system of the future will integrate PICs with electronic ICs and mixed-signal components for RF and power control. The future systems will have both optical and electrical I/O, as illustrated in Figure 18.



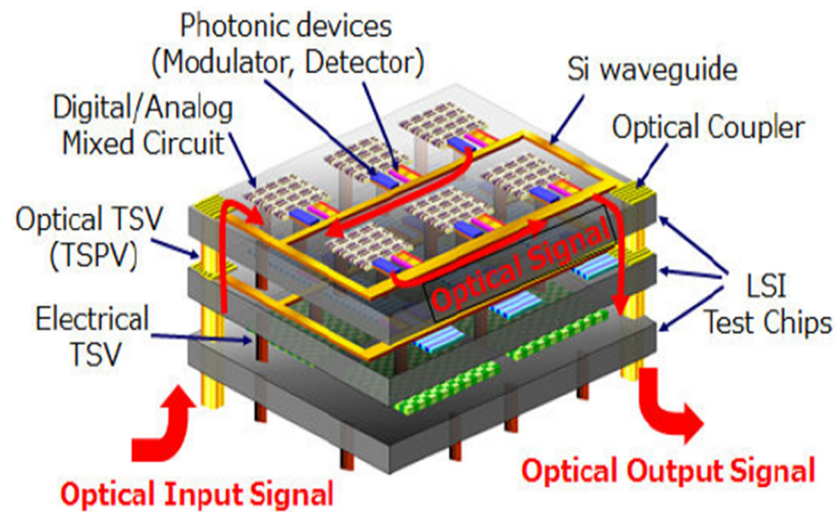


Figure 18. Future photonic/Electronic 3D-SiP with electro-optical package substrate.

### Photonics in the automotive industry

Photonics was first introduced into the automotive industry as an alternative to provide optical fiber communication and sensors internally in the 1990s (see also Chapter 5). Today photonics is used in the automotive industry for multiple critical functions. They include:

- Internal communication networks
- Specialized internal sensors
- Infotainment applications
- Cameras
- Lidar
- Infrared sensors

With the emergence of the autonomous vehicle, vehicles must now include a “super computer” internally to collect data from multiple sensors, provide low-latency sensor fusion, establish situation awareness and make decisions in time to control events when vehicles may be approaching each other at velocities of more than 300 km per hour in certain parts of the world without breaking any speed limits. The use of photonics for communication, which is used for high performance computing, will be migrating to individual printed circuit boards in high-performance computers and eventually to the package and perhaps into integrated circuits.

MOST – Media Oriented Systems Transport – is the de-facto standard for multimedia and infotainment networking in the automotive industry. Formed in 1998 by BMW and DaimlerChrysler, among others, the MOST Cooperation was established principally to define the MOST technology – a multimedia fiberoptic network with standard hardware and software interfaces optimized for automotive applications. The technology was designed from the ground up to provide an efficient and cost-effective fabric to transmit audio, video, data and control information between any devices attached, even in the harsh environment of an automobile. Its synchronous nature allows for simple devices to be able to provide content and others to render that content with the minimum of hardware. At the same time, it provides unique quality of service for transmission of audio and video services. Although its roots are in the automotive industry, MOST can be used for applications in other areas such as other transportation applications, A/V networking, security and industrial applications.

Plastic optical fiber can also be used for seat-occupancy recognition, resulting in cost reduction as well as increased safety. A sensor in the seat identifies whether the seat is occupied. If the seat is empty in the event of a collision, for example, the air bag will not deploy, saving the expense of repair and replacement. Seat-occupancy recognition could also be used to lower the headrests for improved driver visibility if the surrounding seats are not occupied.<sup>4</sup>

<sup>4</sup> MOST references: O. Ziemann et al., Proc. 14th POF Conf., Hong Kong, China (2005); D. Kalymnios et al., Proc. 13th POF Conf., Nuremberg, Germany (2004); M. Miedrich and H. Schober, ATZ Worldwide107, 15 (March 2005); B. L’Henoret, Proc. 13th POF Conf., Nuremberg, Germany (2004); G. Kodl, Proc. 12th POF Conf., Seattle, WA (2003).

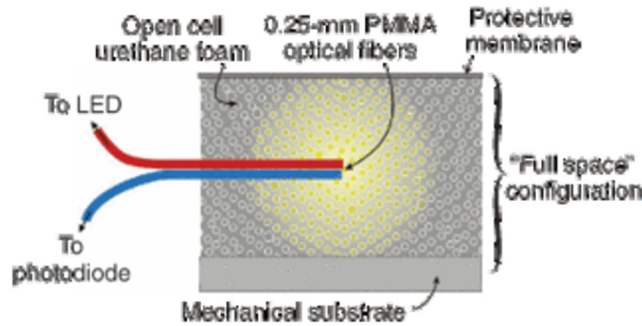


Figure 19. Seat occupancy detection is useful to prevent expensive repair and replacement of air bags in the event of a collision. One available method is the use of special foam that responds to pressure, changing the amount of light transmitted to a plastic optical fiber for occupancy detection.

One approach for seat-occupancy recognition is the Kinotex cavity sensor from Canpolar East (St. John's, NF, Canada). The principle behind this method is light-scattering that is dependent on the compression of the scattering medium, such as special rubber foam. The transducer operates by detecting a change in energy intensity in and around an illuminated integrating cavity. Deformation of the integrating cavity by an external influence, such as pressure, results in a localized change to the illumination energy intensity, which can be transmitted by a plastic fiber and then measured (see Figure 19). In addition to single-point occupancy detection, an embedded array of point sensors within the seat can be used to reveal information on the pressure load distributed over the area, allowing seat-pressurization and/or cushioning to establish the status of occupancy. When a vehicle collision occurs, information from force sensors within the vehicle is interpreted and communicated over the POF network to the individual air bags to control their inflation.

In just the past three years, European automotive manufacturers have installed 25 million nodes of plastic optical fiber (POF) in more than 40 vehicle models. When the European auto manufacturers were looking for a replacement for copper-wire harnesses in automobiles, they wanted a technology that was readily available, easy to terminate, immune to radio frequency and electromagnetic interference, and low in cost. Step-index POF was readily available and even though the losses were high compared to glass, it was a proven commodity and definitely cheap. Further, low-cost light-emitting diodes (LEDs) could be used, and simple connectors could be molded. The use of glass was considered but rejected because of its high cost, connector issues, and limited bend radius.

Today, MOST systems are requiring higher data speeds (up to 150 Mbit/s), higher operating temperatures (to 125°C), and tighter bend radii. Though POF suppliers are scurrying to meet these requirements, plastic-clad silica fibers and multimode glass fiber bundles are also being considered.

An area of concern when using POF in automotive applications is the availability of light sources that deliver the needed modulation speeds. Because standard LEDs have inherently low modulation speed, resonant-cavity LEDs have been developed with higher bandwidth and improved coupling efficiency that are capable of modulation speeds of up to 200 Mbit/s and more. Several suppliers, including Firecomms (Cork, Ireland), TrueLight (Hsinchu, Taiwan), and Astri (Hong Kong, China), are now offering these devices commercially.

In many instances, safety requires communication between sensors embedded in the vehicle and other devices, such as air bags, that are used to ensure safety. While using POF for other non-safety-oriented applications is becoming more prevalent, automakers typically reserve these uses for the automotive aftermarket—those (usually optional) devices that replace initial factory-installed equipment.<sup>5</sup>

From this study on the use of optical fibers in automobiles, we conclude that photonic technologies are superior to electronic solutions in terms of data rates, bandwidth, reliability, and robustness. However, it is not easy to achieve integration and miniaturization in photonics as easily as in electronics. Although optical sensors and communication protocols have demonstrated their performance capabilities, they still need to prove they are capable of replacing their electronic counterparts. The industry is relying on light/image or optical sensors to develop a wide range of safety technologies for occupant safety, intruder detection, lane departure warning, and blind-spot detection. Meanwhile, fiber optic sensor's rigidity and resistance to electromagnetic interference has made them well suited for automotive applications. The major application areas of optical sensors are driver assistance systems and traffic monitoring systems. The optical sensor (rain sensors), used for automatic wipers in cars, is a typical illustration of

<sup>5</sup> Some material is from [www.mostcooperation.com](http://www.mostcooperation.com)

the suitability of optical sensors for hostile environmental conditions. In the case of driver assistance systems, cameras with image sensors are used to alert the driver about the driving environment and the possibility of collision with other vehicles. Photonic technology has also been associated with lighting systems in automobiles. It not only aids the development of anti-glare lighting but also night-vision systems for safety in harsh driving situations such as darkness, fog, and exposure to blinding light.<sup>6</sup>

LIDAR has been in use for over 60 years in military, aerospace, robotics, and meteorological fields. Today it is experiencing a flurry of interest due to the expectation that it will be one of the key sensors to enable autonomous driving. With more than US\$1.7 billion raised to date, more than 85 companies are developing automotive-grade LIDAR sensors using their unique approaches. The 2019 Automotive Lidar Conference was the only event in the world exclusively focused on automotive LIDAR technologies and applications. The conference's sessions described the various approaches to making a LIDAR system, as well as explaining via physics and math the reasons to choose one approach over another. It also discussed the publicly disclosed methods from each of the known developers, their strengths and weaknesses, and how likely they are to scale in manufacturability and cost. The conference also provided overviews of marketplace projections and business trends. The material presented enabled making well-informed decisions regarding which LIDAR approaches are optimal for solving their challenges and requirements.<sup>7</sup>

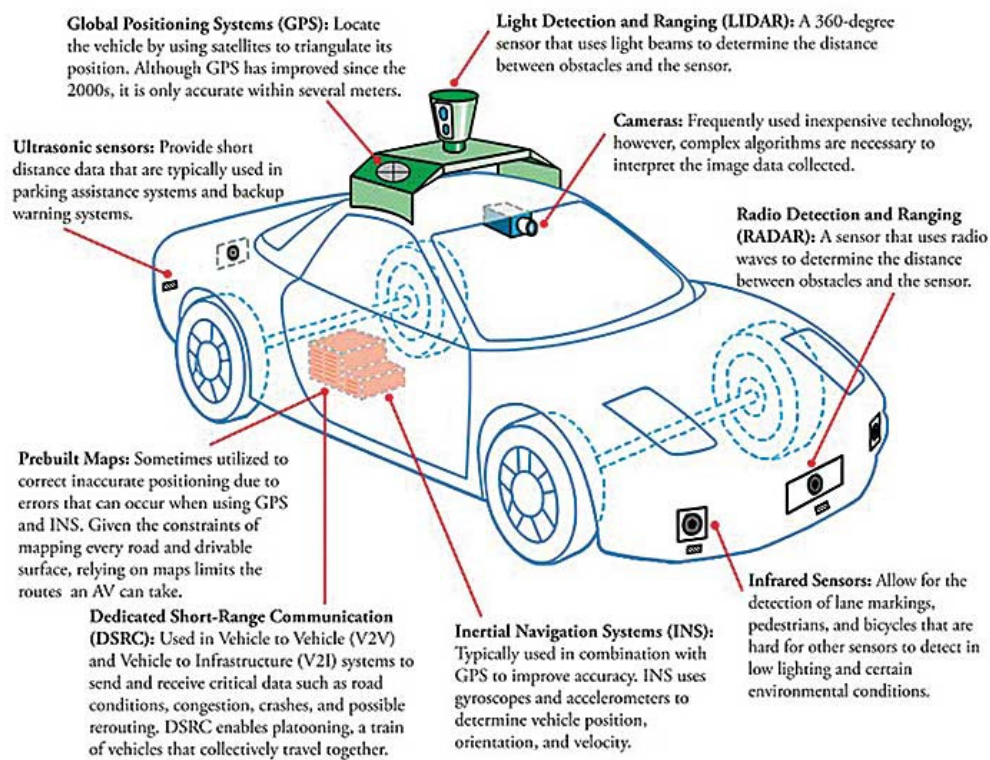


Figure 20. Wiring autonomous vehicles (Assembly Magazine, 5 October 2017)

### Photonics in Data Centers and High-Performance Computing

There is no saturation in sight in the escalating demands from existing and emerging data centers. This demand is driven by user-generated content, IoT, 5G and data-centric applications including AI. Presently the data centers in deployment use separate pluggable modules that are situated on the front panel of the rack-scale data center enclosures, hence the term faceplate-pluggable (FPP) modules. These modules are electrically connected to the system housed in the enclosure through their rear and optically connected through their front with optical fibers to the optical network in the data center. As of 2021, 100 Gb/s is the dominant data rate for such modules deployed in hyperscale data centers. The volumes for the 100 Gb/s modules are in the millions of units per year. The 100 Gb/s modules are being increasingly followed up by 200 Gb/s and 400 Gb/s interconnects with 800 Gb/s and even 1.6 Tb/s data rates predicted for modules in the first half of the 2020s. The challenges for the next-generation 400 Gb/s level

<sup>6</sup> Material from the International Journal of Scientific & Engineering Research, Volume 4, Issue 7, July-2013.

<sup>7</sup> Material from the Automotive Lidar Conference 2019

are defined. Intel demonstrated a 12.8 Tb/s co-packaged optical switch in February 2020. However, these solutions offer large form-factor and power budgets that are compatible with scaling plans for the data center roadmap.

The intrinsic limitations to the photonic data center instrumentation are loss and crosstalk. Another challenge is that the complexity of the central shuffle network scales exponentially with the port count  $N$ , and it has been recognized that the key limiting factor in loss, crosstalk, and footprint is the waveguide crossings. It has been proposed to leverage the Si/SiN multi-layer structure to achieve crossing-free designs, which can substantially improve the performance and scalability. The other challenge lies in the total number of MRRs, which scales poorly at  $2N^2$ . For large port-count numbers, further studies were performed on combining the scalable three-stage  $C_{los}$  network with populated S&S stages. The proposed design offers balance that keeps the number of stages to a modest value while largely reducing the required number of switching elements. The scalability is predicted to be  $128 \times 128$ .

With the scale-up of switch port count, the requirement of efficient calibration/testing methods for such complex integrated circuits is severe and urgent. Power taps are usually utilized with either couplers or built-in photodiodes. The additional components could substantially increase the device insertion loss, complexity, and package cost, leading to a reduction of yield.

Historically, the photonics industry has been strongly influenced by telecom. Because of the difficult operating environment (e.g.,  $-40^\circ$  to  $85^\circ\text{C}$ , RH up to 85%) and thus high cost of system deployment and maintenance, each telecom upgrade cycle is long and carefully planned. The annual forecast visibility from carriers to equipment providers and to component suppliers is fairly good. Sophisticated and expensive photonic components can be accepted during this long cycle. Photonics manufacturers have more time to plan and respond to customer demands, and the unit volume has not been as high as has been seen recently from data center business.

Data center businesses operate the majority of their networks inside of a controlled environment – for example, in temperature- and humidity-controlled buildings (i.e.,  $0^\circ$ – $55^\circ\text{C}$ , RH 40-60%). Photonic components are a relatively small part of capex and opex but are also a significant contributor to revenue generation through bandwidth sales to cloud customers. The quantity of photonic integrated circuits that would be needed for data center applications requires more scalable manufacturing techniques, similar to those already established for electronics. The route to address the aforementioned challenges is to evolve the optical interconnect by integrating the switch optics with the corresponding electronics. This can help provide scalable solutions that meet the energy, density and capacity handling demands. This co-integration can reduce power by eliminating the internal I/O functions, while co-packaging also improves reliability and enables more cost-effective manufacturing.

While in recent years the demand for photonic chips did not justify the investment needed for this co-integration, the demand projection at present will justify starting these investments in the next 18 months.

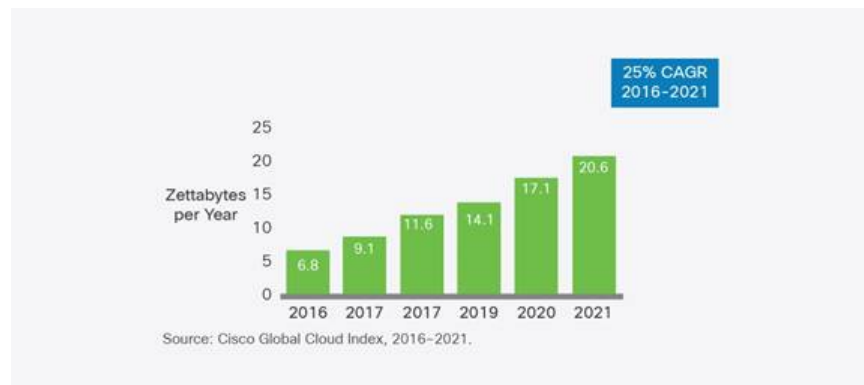


Figure 21. Global data center IP traffic growth



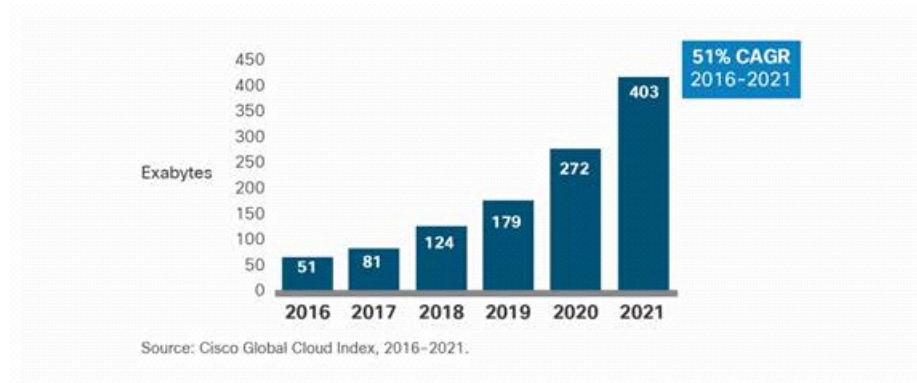


Figure 22. Big data volumes

**Supply chain requirements**

Supply-chain development must include sources for design and prototype manufacturing with advanced capability and low cost. It must also include processing design kits and product design rules for multi-project wafers. This is essential to support low cost, short lead-time prototype production that ultimately leads to industry standards for components and integration methods. These are key to reaching high yield, low-cost production of heterogeneous integration for complex photonic/electronic sub-systems and systems.

**Attributes**

The attributes of Photonic/Electronic packaging technology that must evolve to meet future requirements are listed in the Table below. They include architecture, structure, operating characteristics, etc. The ongoing roadmap activity will check these attributes and project changes that may accelerate the rate of progress in the key parameters of power requirement, performance, and cost. The complexity of heterogeneous integration demands a complexity in the assembly and packaging technologies used. The areas are optical, electrical, mechanical, integration and thermal. This requires new materials and processes and, in many cases, new equipment to achieve high throughput and yield. Figure xx below is an example of equipment designed for assembly of photonic components into PIC based systems.

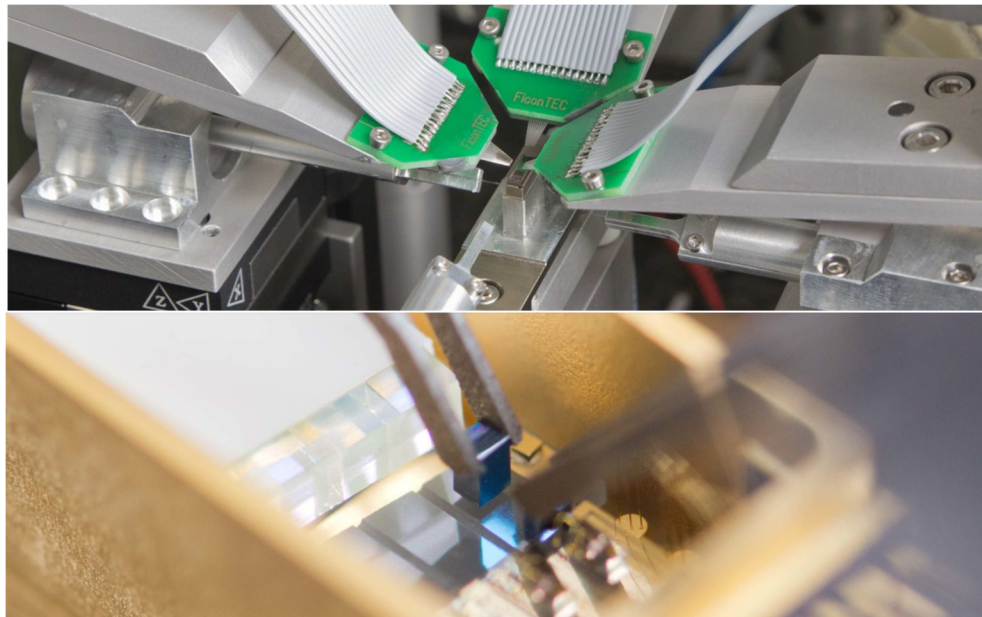


Figure xx: Assembly and test equipment for photonic components (from Ficontec GMBH)

Table 6. Attributes associated with Photonic/Electronic Packaging

3D integration in the package
Co-Design and simulation tools for all components: passive, RF, photonic, electronic, plasmonic, MEMS
Component attach for different materials and component types
Cross talk
Electrical connection into and out of the package
Electrical resistance/inductance/capacitance
Environmental compatibility
Hermeticity
Heterogeneous integration for diverse materials (different CTE, electrical, optical, mechanical properties)
High volume/parallel manufacturing processes
Incorporate changes over life of the roadmap in components and materials available
Low temperature assembly processes
Models for new composite materials
Photons into and out of the package
Physical density of components
Physical size
Reliability under stresses of the use case (thermal, mechanical shock, electrical, chemical)
Reliable power delivery with near threshold operation
Stress management
Test for complex SiP electronic-photonic products
Thermal management
Warpage (thinned components, package substrate)
Yield

Table 7. Photonic Test Requirements

Test Level	Test Need			
	Optical Access	Sources	Detectors	Functions
<b>Wafer</b>	45° mirrors, vertical grating couplers, cleaved fiber, tapered fiber, lensed fiber, focused free-space beam, evanescent coupling	External sources injected via fiber or free-space access  Integrated sources	External photodetectors, potentially in arrays; Imaging sensors (eg. CCD/CMOS FPAs); Optics to collect and/or image light to be detected.  Integrated photodetectors	Wide variety of device characterization and functional tests; media loss/cm, insertion loss, modulation depth/bandwidth, polarization control, wafer uniformity, detector sensitivity/responsivity, temperature sensitivity, die-to-die variation, skew between outputs
<b>Chip</b>	Wafer options plus edge coupling to embedded or surface waveguides.	Wafer options	Wafer options	Wafer options plus edge coupling impacts on loss, spectral bandwidth and polarization

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