Chapter 17: Test Technology

Full Roadmap: **eps.ieee.org/hir**

Section 9: Data Analytics - Appendix A

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Note: This appendix includes the full text of *the Adaptive Test* and *Test and Yield Learning* sections of the *Test Technology* chapter of the 2019 HIR. These sections were merged into the newly-created *Data Analytics* section for the 2020 HIR. This information has been linked to the current HIR Test Technology Data Analytics section as a reference for those who are interested in in-depth analyses on these topics.

Adaptive Test In-Depth Analysis

Adaptive Test is a set of IC manufacturing test methods enabling real-time optimization of the value of production test (in a fully automated way). These methods include the practice of using production test data to reduce/optimize test cost, improve product quality and reliability, drive yield improvements and improve product performance.

To effectively use Adaptive Test, additional development is needed in data infrastructure and data analytics, production test cell design, die traceability, and the coordination between IC manufacturers, IC test and assembly. The top challenges facing industry application of Adaptive Testing are listed in the portion of this section called "Adaptive Test Challenges and Directions."

There is a diverse set of Adaptive Test applications aimed at different product markets and requirements. Companies should target specific Adaptive Test applications aimed at their product requirements and target markets. Thus, the benefits of implementing Adaptive Test will vary based on type of product, manufacturing flow, volumes and technology.

This section provides:

1. A description of Adaptive Test and terminology used by its practitioners
2. Example applications of Adaptive Test as of 2019 and future opportunities
3. A list of challenges for the development and deployment of Adaptive Test.

To ensure the industry can fully exploit the benefits of Adaptive Test, this section describes:

1. The infrastructure requirements for test cells, data systems and device and system designs
2. A description of Adaptive Test challenges and the coordination needed between IC manufacturers, OSATs (Outsource Assembly and Test providers) and fabless system integrators.

Definition

Adaptive test comprises a set of methods for automatically changing manufacturing test conditions, manufacturing flow, test content, test limits, or test outcome to reduce test cost, increase outgoing quality and reliability, reconfigure parts, or collect data to further improve test and manufacturing. Adaptive Test strives to make these changes in a manner that does not significantly increase testing time or increase human involvement in test operations. The decisions on when and how to adapt the tests are made algorithmically by the tester, other test cell equipment, or an automatic data analysis system (given automation – the analysis time is significantly reduced compared with the traditional, engineering-intensive approach).

Adaptive Test Description

Adaptive Test is generally accepted as an advanced test strategy that can be used to achieve quality, yield, and cost goals that might not be reached by normal test methods. For example, Adaptive Test may modify a production test process in a number of ways:

1. **Test Conditions** (modifying test setup conditions or limits – such as voltage or clock frequency)
2. **Manufacturing Flows** (adding or deleting test insertions such as burn-in)
3. **Test Content** (modifying specific patterns or tests such as transition fault or IDDQ, respectively)
4. **Test Limits** (changing the pass/fail limits such as DC power or Vdd-min test specifications)
5. **Test Outcomes** (changing the binning or configuration of some die based on post-test analysis of the die's test results)

Adaptive Test applications are organized by when decisions are made to modify the test flow and to which device(s) the modified test flow are applied. The four most common categories are in-situ, feed-forward, feed-back and post-test. Figure 1 is a flow diagram depicting the relationships among these four categories.

1. **In-situ:** Data collected from the part being tested is used to modify the testing of the same device during the same test insertion. These methods include not only speed-binning and trimming calibration (which are not new), but using data from any test to modify test conditions or device settings for other tests for this specific device. For example, parametric data taken from on-product process monitoring structures may be analyzed – and the results used to drive subsequent test limits or test conditions or test-driven device reconfiguration.
2. **Feed-forward:** Data collected from a previous test step stage (e.g. probe, hot probe, burn-in) is used to change how the same parts are tested at a future stage. An example of the Feed-forward category are statistical methods which identify 'risky' dice or wafers and selects these components (only) for burn-in, or "clean" dice that may be candidates for reduced testing.
3. **Feed-back:** Data collected from a previous part (or parts) is used to modify the tests or limits of different devices yet to be tested. Skipping some test patterns on high-yield wafers, adding more tests to low-yield wafers or refining statistical models used for die classification are examples of this category.
4. **Post-Test:** Data sample statistics or other analysis is performed between test steps and is used to reclassify certain devices or to change future manufacturing flow and test conditions for these devices. Part Average Testing and outlier identification methods are examples of the Post-Test category.

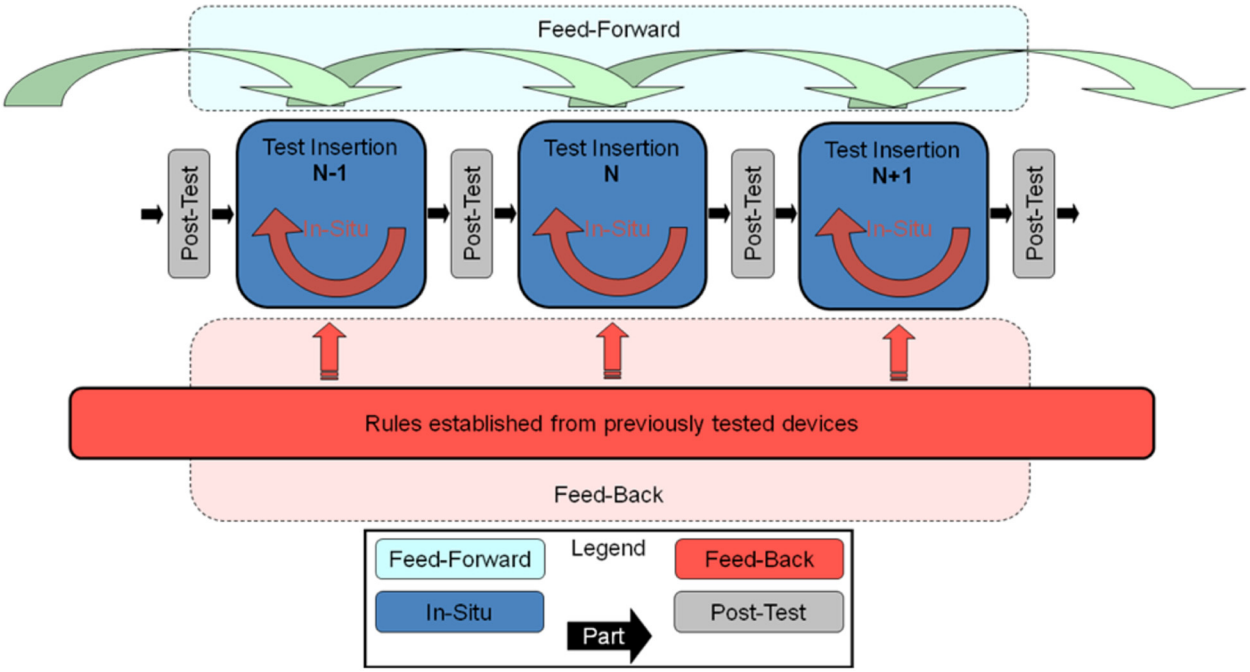

Figure 1: Adaptive Test supports feed-forward and feed-back data flows. Adaptive Test provides for data use for test decisions either in-situ (i.e. during a given test step) or post-test.

Example Applications

Below is a list of example Adaptive Test applications. Each example is labeled by one or two categories outlined earlier. In addition to clarifying the categories, the examples demonstrate the shift from manual and static methods to automatic methods with little or no human intervention during test execution. Note that the use of die ID (e.g., a die-specific identifier such as wafer/XY coordinate and lot information, or a unique identifier that is fused on each die) is a key enabler for many of these applications. There is a list of references that include many example applications at the end of this section.

Some of these applications are more widely used today than others. Common methods include:

- Data feed-forward
- Good die, bad neighborhood
- Post wafer test statistical analysis – e.g., pickmap updates
- Device trimming or reconfiguration

- PAT (Parts Average Testing) and DPAT (Dynamic Parts Average Testing) – for outlier detection
- Burn-in optimization

1. **Dynamic test flow changes (In-situ, Feed-forward):** Die production data is monitored within the test program to add or remove tests, to selectively perform per-die characterization for yield learning, or to collect data for later diagnosis. This application supports many common real-time Statistical Process Control (SPC) methods.
2. **Statistical screening (Post-Test, Feed-forward):** After wafer or lot data collection, identify die which are outliers or mavericks as possible sources of test-escapes spikes or reliability failures. Statistical screening is Feed-forward because results can be used to route target dies through test flows different from the main flow.
   - PAT – Part Average Testing is a statistical technique in which a die is tested against static or dynamic test limits derived from other die in a common subgroup
   - NNR – Nearest Neighbor Residuals is a statistical technique relating a univariate or multivariate test result to a model derived from a local region on wafer of the device under test.
3. **Single-step flow control (Feed-forward):** Data from one test step is used to optimize testing at the next test step to focus subsequent screening on issues observed in the manufactured parts.
   - For example, inline test modifies wafer test; wafer test modifies package test; burn-in modifies final test; or package test modifies card/system test.
   - One method for doing data feed-forward is to store results in on-chip memory (e.g., Flash) that will be read and used at subsequent test steps.
4. **Off-tester optimization of test flows (Feed-back):** Off-tester data analysis drives test flow changes for future devices (fully automated).
   - For example, off-line analysis could optimize test flows, test content and test measurement routines using input from many sources including historical data, test capacity, required turn-around times, DPM (defects per million) requirements, expected yields and parametric data.
5. **Production monitors and alerts (In-situ, Feed-forward, Feed-back):** Data from multiple sources is merged for statistical analysis to control production test optimization beyond what has historically been possible.
   - For example, subtle parametric shifts from marginal wafer probe contacting can be automatically identified and action taken during production testing.
6. **Die matching (Feed-forward, Post-test):** Production data from various sources is used to support the build/test process for multi-chip applications and many of today's board build process to match specific die combinations during assembly.
   - Note die-matching data transfer may require world-wide data sharing, across multiple companies and throughout the entire supply chain.
7. **On-chip test structures and sensors (In-Situ, Feed-forward, Feed-back):** Data collected from auxiliary on-chip test structures such as ring oscillators, selected critical paths, on-chip voltage and thermal sensors, or on-chip reliability monitors is used to modify the die's test content, test limits or future test flow.
   - Sensor measurements can be used at all levels of assembly and test (including system operation) to monitor and adjust functionality.
8. **On-chip configuration (In-situ, Feed-forward):** Production test data (including test structure data) is used to adjust features in the design to improve a die's performance, power, margin, yield or reliability.
   - Emerging ICs have more on-chip configuration and adaptability such as clock tuning, partial goods (redundant spare cores), and voltage and frequency adjustments (including per core).
9. **Component System Level Test (SLT) test optimization (In-Situ, Feed-forward, Feed-back, Post-test):** Test results from current or prior operations are used to customize the test flow or enable test sampling.
10. **Card/System configuration and test (Feed-forward, Post-test):** Component test results (such as parametric data, yield characteristics or partial good data) are used to customize the card/system test flow or customize card/system test conditions.
    - Data feed-forward from die testing are fed-forward and used by the board test program to make decisions on whether to add specific content to test for marginality.
    - Data feedback is used to deliver card/system test results to IC suppliers – who use this data to adjust test content, test condition or test limits.
    - In-situ card/system test measurements (such as on-chip sensors for voltage or temperature) are used to modify board testing (e.g., adjust margins and/or performance). On-chip sensors can also be read during

field usage to monitor aging and perform in-field adjustments and/or send results back to IC suppliers to adjust their test limits.

11. **Adaptive Diagnostics (In-situ, Feed-forward):** Test results drive advanced diagnostic data collection.
    - For example, on-chip BIST (built-in self-test) circuitry can be programmed on-the-fly to localize and characterize specific types of failures. But these methods must only be selectively applied to ensure reasonable test time/cost.
    - Many emerging chips have programmable on-chip test controllers that can interpret test results on-chip – and take action (test, diagnostics, characterization) without requiring extensive data collection being transmitted to/from the test equipment.

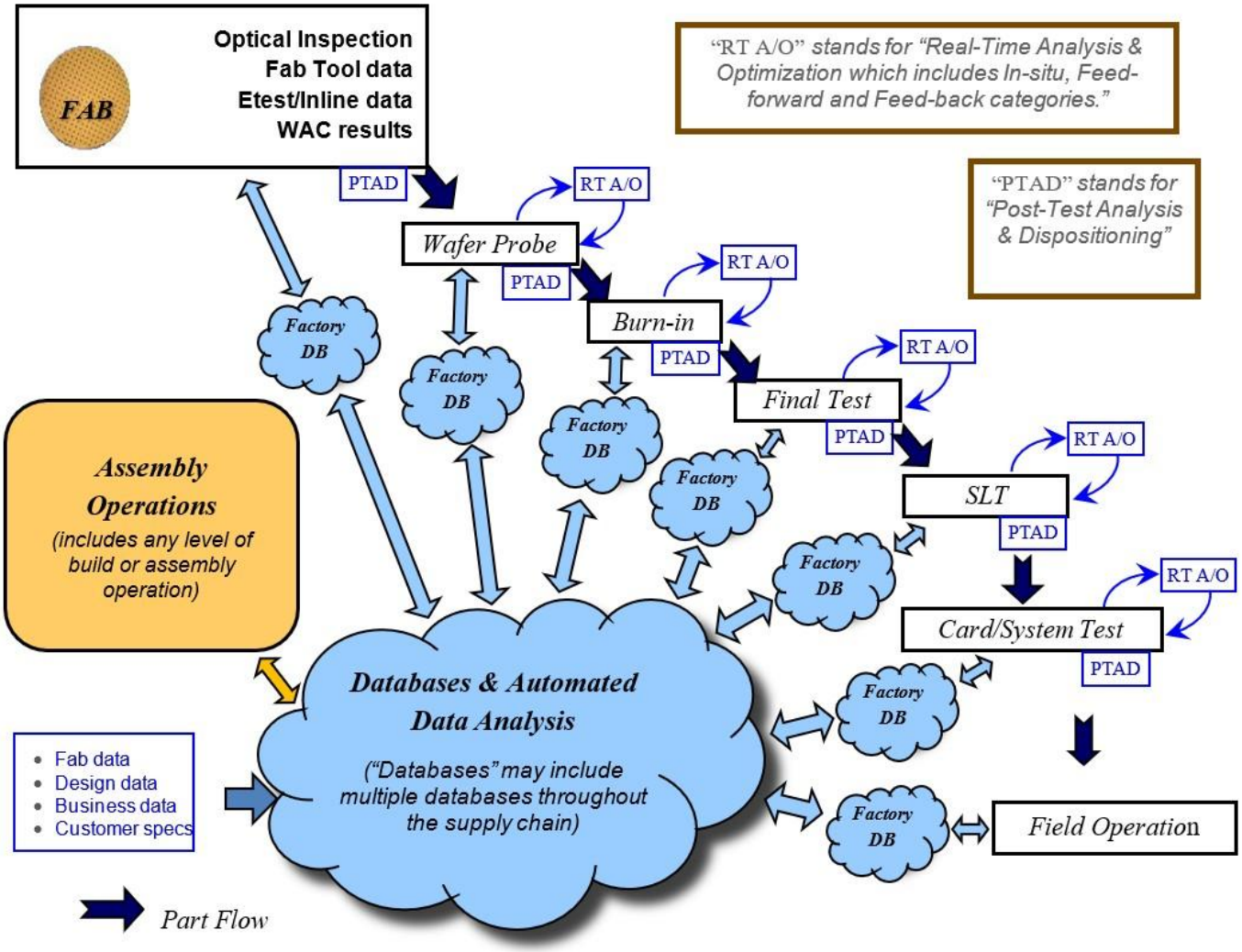

Figure 2: The architecture of Adaptive Test organizes each insertion's test data into one or more databases. A waterfall of manufactured parts may insert, join or query databases for test flow decision-making.

Adaptive Test Architecture and Infrastructure

Adaptive Test makes decisions throughout the manufacturing process based upon data from multiple sources and using data of varying detail and completeness. Before actionable decisions can be made with multiple-sourced data, new data integration requirements are needed. Some integration requirements are unique to Adaptive Test and are different from data requirements used at any of the originating sources.

Figure 2 displays a model of the entire End-to-End flow of parts under test and Adaptive Test applications. Note that in the flows shown in Figure 2; feed-forward, in-situ, feed-back and post-test dispositioning opportunities can occur at each test step. Although Figure 2 shows the total data store as a single database, the actual data structure would probably consist of multiple distributed database hierarchies each with unique capacity, latency and accessibility characteristics.

Overall Data Model Requirements for Adaptive Test

Making the decisions to adapt the test attributes listed above first involves collecting the proper data and then organizing the data into a structured data model so that the right data can be accessed when and where it is needed. At the appropriate time, data of the proper scope – that is data from a particular test run or data from a particular part, wafer, or lot – is accessed from the data model and processed by the applicable decision algorithms. Similarly, the test variables, such as limits, conditions, flow and content, must be changed at the right time to complete the adaptation decision.

The data model can exist entirely in an off-line database apart from the tester, or be distributed between servers and the tester depending on the latency requirements and convenience. To branch a test flow for a particular part (a real-time decision) latency must be short, i.e. there can be no significant impact to test time. To support low-latency requirements, the data needs to either be stored on the tester or be rapidly pulled into the tester. To make an outlier decision such as to re-bin already tested parts, longer latencies are tolerated such as from the time of test until wafer maps are uploaded or the parts are dispositioned. Longer latencies mean an off-line database can be used.

Decisions to adapt a test are often based on comparing the variation observed on the sample of parts in question to a model of the expected variation. In outlier detection, parametric test limits are adapted to track expected variation so as to only discard parts with unexpected variation. Tests can be temporarily dropped from a test flow when their control charts show the manufactured material and test process is in control and within specification. If and when monitoring based on sample testing shows the material or test process has changed and gone out of control, the tests are reinstated on every part. Similarly, diagnostic data collection tests can be added to a test flow when certain types of failures occur more frequently than expected.

Generally, more adaptability means more frequent decision-making in the test flow with the goal of improving the trade-off between shipped product defect level and yield/cost. Adaptability follows a bottom-up progression from the conventional static limit, to a static parameter variance model (static PAT), to a variance model with variable parameters (dynamic PAT), to choosing variance model equations based upon well-grounded principles. Moving up this progression requires not only more data but also a better understanding of the processes that cause the test response to vary. This progression also means the decision-making generally moves from an off-line human activity to an on-line machine activity.

Data requirements unique to Adaptive Test center on the database policies of latency, access and retention period. Latency measures the time between the request for a data item and the availability of the requested item. Access refers to the scope of the user community that can store, retrieve, and act on a data item. Retention period measures the time the data item is electronically available within the required access time period.

- **Local processing in the test cell requires low latency.** For example, access latency should be in a few milliseconds if data is to be retrieved on a per device level – Real-Time Analysis & Optimization (RT A/O). Post-Test Analysis & Dispositioning (PTAD) applications may have latency requirements of a few seconds to a few minutes. Normally data volumes for these steps would be relatively small. Processing in a central database (e.g., "The Cloud") has more relaxed timing constraints (minutes, hours), but typically deals with much larger data volumes.
- **Data access requirements are influenced by the diversity of users "touching" the data.** Applications that bridge assembly or test companies, fabless design companies, and test developers require robust access mechanisms to ensure the correct people and processes access only the appropriate data.
- **Data retention requirements depend on the specific market requirement.** Some requirements drive data retention of all shipped products to 10 years or more.

Many areas of IC manufacturing are increasingly more comfortable with using data from the cloud, but a notable exception is the test cell. Test cell integration of Adaptive Test algorithms is one of the most challenging applications. For example, local test cell actions (such as "clean probe-card now") were the sole responsibility of the specific test floor and were designed to guarantee the test cell integrity and test cell-to-test cell correlation. Adaptive Test changes this paradigm in a number of ways:

- **Algorithms will be owned by multiple involved parties,** including wafer fab, design house and test floor. Some algorithms may originate from commercial providers, others from the involved parties themselves. They all need be executed synchronously in a real-time environment.
- **Data collection as well as data access** (e.g., to upstream data in case of data feed-forward) **becomes a mission-critical task of a test operation as well as the entire supply chain.** This challenges the reliability of the underlying infrastructure, which likely spans multiple companies, geographic areas and cultures.

- **It is required to simulate the impact of algorithms on historical databases** to understand how to maximize the value of Adaptive Test without creating adverse side effects. This requires the exact same algorithm to be executed in as diverse environments as a cloud database and a test cell measuring real-time data.

As a consequence, the industry needs to develop:

- **Provenance models** to allow disparate data sources and users to access and trust data.
- **Data exchange formats** which are flexible, compact and standardized so that only minimal extraction and translation effort is required. A common set of indices is required, such that data remains identifiable and traceable even across heterogeneous supply chains.
- **Recipe management systems** which can handle a diverse set of recipe origins, check for (likely unintended) interactions and maintain consistency across non-synchronized update cycles from the various origins. Version control systems for these recipes are also required.
- **Monitoring and rule-checking systems** must be enabled to monitor the health of Adaptive Test algorithms (are basic assumptions met?) and the health of the distributed data, and escalate errors to the right entities in an actionable format.
- **Distributed data distribution infrastructure** which can handle a diverse set of data origins, monitor data changes, and maintain consistency across non-synchronized updates from the various sources. Data version control systems are also required, as are logging systems able to trace changes.
- **Shared analysis** may be the only way to jointly discover problems and opportunities. The large quantities of proprietary data may require that analysis be performed in a distributed manner with intermediate results shared.

Global Adaptive Test Infrastructure Requirements *(data exchange and archiving, reference Figure 2)*

This section describes the data storage and exchange requirements across the supply chain.

Data requirements that are different but not unique to Adaptive Test include date and time stamping, test naming, and date recording methods. For example, Adaptive Test data stamps should be consistent across all insertions and between companies. Current date stamping practices are ad-hoc with some companies using different date formats and date references at different test insertions. Database standards exist for date stamping such as Coordinated Universal Time. A time and date stamp requirement policy eases integrating test data when some units are retested and simplifies merging two (or more) data sets in an unambiguous time order. Similar issues arise in recording floating point results of the same test from different insertions with different precisions and formats.

The following are important attributes of a global infrastructure:

- **Latency.** Global latencies can be quite long, only needing to satisfy the needs of the typical uses. Data at this level is packaged in some lot-related group so access time in the order of lot processing times are considered adequate. These times (for non-local data) could be in days.
- **Volume.** While data volumes have increased and storage times extended so has the ability to store this data. The real issue is not the storage but the locating and use of this data. Data volumes are in the order of 2-20 Gbytes per tester-week with history storage spanning 4 to 20 years with the longer times being for automotive, medical and some industrial applications.
- **Provenance.** All characteristics of data must be trusted. Who created it, has it been changed, and is it accurate are all facets which must be known.
- **Security.** Adaptive test requires the sharing of data but it must control that sharing to those who have the need and right to use it.
- **Reliability.** Testing cannot stop due to infrastructure equipment or communications failures. Checks are also required to ensure that the required data is collected and stored.

Production Test Floor Infrastructure and ATE (and component/socketed SLT) Requirements

This section describes the data infrastructure requirements local to the Test Floor.

The test cell is expected to deliver a cost-effective means to screen defects for quality, classify devices for performance and collect data for learning. The rate of product complexity is increasing with more clock domains, voltage planes, IOs and configurable fuses followed by the introduction of parallel testing of multiple, dissimilar devices with 2.5D and 3D stack packaging. In parallel, the business demand for higher quality and reduced product cost severely challenges the ability of the test cell to continue to provide an effective test solution and still continue to reduce the cost of test. Adaptive Test methods provide levers to address these additional demands but not without disruptions of their own.

Adaptive Test requires the test cell to be able to accept input from external and internal sources, apply device-specific models to determine test conditions and to evaluate results for flow control and device binning. This materially changes the setup, execution and categorization requirements of the test cell and affects both low-level software capability such as firmware as well as high-level software such as the executable test program. Of particular challenge is the relationship of flow control and binning when the test flow becomes a function of non-deterministic evaluations influenced by dynamic test points, limits and device configuration.

The following are important attributes of a test floor infrastructure:

- **Latency.** Adding Adaptive Test should not impact the throughput for a test cell. Data collection must have minimal impact. In addition, the various equipment in a cell must respond quickly to changes driven by an adaptive test rule. For real-time control, the response time should be in the low milliseconds for each part. Some applications require require that data taken from a part can be used for binning that same part in real time. There is also lot feed-forward which is more of a lot-based time scale, usually hours.
- **Volume.** Required data volume to enable Adaptive Test varies by Adaptive Test method. Incremental data for real time decisions is small whereas data for feed-back applications can be much larger. Data volumes in the range of 2-20 Gbytes of data per tester per week (while archiving this data monthly) are not unusual. The increase in data volume also brings challenges to the network infrastructure supporting the tester with increased demand on both reliability and bandwidth.
- **Provenance.** All data generated from a test cell must be fully trusted. Data should be signed and possibly encrypted.
- **Security.** Within a test floor, this is not usually a concern. With the advent of keys and other sensitive data being stored into parts, it is becoming necessary to comprehend security methods such as selective encryption of data from specific parts.
- **Reliability.** Testing cannot stop due to infrastructure equipment or communications failures. Each test cell must continue at least the current lot without floor communications. This implies that each cell has sufficient data resources (data bases and storage) to continue.
- **Legacy Support.** Support for legacy testers, handlers, probers and products.

In addition, future test cells will have to support the following:

- Per-device test flows (and per-device limits, test conditions and content) based on external inputs, the device itself, and dynamic business rules.
- A move from being the entire cell controller to a test engine with a standard API.
- Asynchronous and distributed (multi-insertion) test flows.

Much work is being done today outside of the semiconductor industry to address the needs for machines to communicate and for the data generated by these interactions to be collected, analyzed and acted on. The semiconductor industry should take advantage of these as appropriate. Groups like SEMI CAST (www.semi.org/en/collaborative-alliance-semiconductor-test) have been organized to stimulate discussion within the industry to standardize around available technologies.

- **IoT (Internet of Things) and MTM (Machine-to-Machine).** Communications protocols, e.g., MQTT (Message Queue Telemetry Transport) must be both secure and extendable.
- **Distributed file systems.** Systems like IPFS (Interplanetary File System) are proposed to handle the distribution of asynchronous data while maintaining trust.
- **Streaming data analysis.** While data mining of large collections of data is a popular topic today, the concept of treating data as a stream is more appropriate to the needs of the semiconductor industry.
- **Replay/simulation capability.** Data systems must have the capability to evaluate the impact of different test rules and flow. For example, there must be a "replay" capability where a user can change test rules – and evaluate the quality, cost and other impacts.

Test results driving reconfiguration of "Adaptive Designs"

More and more designs are being reconfigured during testing. Examples include partial goods (on-chip redundancy), VDD/frequency adjustment per die, and local clock tuning. In most cases this product personalization will be based on either test measurements or data feed-forward from other operations. In some cases, this reconfiguration will be based on "application demand".

Testing resilient features

Resilient features are on-chip structures that can be used to configure the product to work around hard defects or to tolerate latent defects. These structures span a wide range of circuits and architectures, including fuses, redundant memory elements, architectures capable of operating on reduced numbers of logic elements like CPU cores or graphics components, error-detection and retry schemes for hard and soft errors, and the sensing and control circuitry for adaptive designs. Like every other circuit, these structures must be themselves tested and characterized, though these circuits present unique testing challenges beyond standard logic and memory elements, including temporary configurations (for fuses), soft-repair vs. hard-repair validation (for memories), combinatorial explosion of down-cored variants of redundant features, the need for error injection to test recovery circuits, and analog stimulus for sensors (such as voltage or aging monitors).

While resilient features are widely used for memories, it is currently less frequently applied for logic cores. This could change if an automated approach were available to help chip designers employ partial-good die on their chips; this will need to include power-off means for bad cores and functional operation in the presence of non-functional core instances. This is in addition to DFT to isolate such cores and fuses to disable the bad ones once identified by testing. EDA companies need to pursue means to help designers add this to their chips.

Non-deterministic device behavior: Test and run-time availability

Non-determinism is incompatible with traditional cycle-accurate automated test equipment, but is nonetheless becoming typical on modern SOCs. Several new I/O protocols are non-deterministic, as are the standard methods to avoid metastability in clock-domain crossings (which are commonplace in highly integrated devices). Fine-grained power gating and power-state management can change the configuration of a device and its execution profile during test and normal operation. Adaptive designs take this notion even further with architectural features which can perform state rollback and pipeline retry based on events at arbitrary times during execution. The result is that test patterns, particularly functional patterns which execute in mission mode, must either prevent or be tolerant of non-deterministic response. The former raises coverage questions, the latter pattern and ATE interface challenges.

Testing Adaptive Designs

Adaptive designs bring the complexity of dealing with advanced power management such as power gating, variable configuration of IP (such as IO and arrays), self-defining performance bucketing and part-specific reconfiguration (such as redundancy, repair and harvesting) to a test environment traditionally characterized by a linear test flow measuring to fixed corners to verify device operability. Instead, on-chip sensors are used to detect the workload, voltage, temperature, and timing margin of the chip as it operates and dynamically adjusts power supplies, clock frequencies, thermal control, and even the instruction stream. The adaptive features of a design make it much harder to define (and thus characterize) both typical and worst-case use models, which in turn makes it more difficult to test appropriately. Additionally, the removal of excess margin represented by traditional guard-banding increases the risk of exposure to subtle defects, necessitating both higher coverage and better correlation between structural and functional test modes.

An emerging direction is to apply Adaptive Test techniques (which modify the parameters or content of a test program based on information collected about the device under test from the current or previous test insertions) to adaptive designs (which modify their own operating point or execution flows based on internally generated feedback). The proclivity of an adaptive design to compensate for the environment in which it is being (functionally) tested will present challenges for data gathering by the Adaptive Test process beyond opening control loops to test at fixed conditions. A means to record and store the conditions to which the device is tested, organized in a manner for ease of retrieval and consumption, is required.

Online Testing for Automotive ICs

Automotive standards such as ISO26262 are driving the need to perform testing in real-time while the system is in use. Common online testing methods include Logic Built-in Self Test (LBIST) and memory BIST and repair. Results from these online tests will drive reconfiguration – for example, to work around logic blocks that fail the online LBIST. It is clear that, as online testing is used more widely, the industry will need to develop methods to validate these BIST methods and ensure they are defect free. Also, it will be required to verify reconfiguration capability.

Adaptive Test for Fab Process Feedback & Control

There is a long history of defect-related fault information identified through test for use in yield improvement by the fab, but parametric tuning feedback related to performance has been much more limited. The use of data collection and statistical models applied through Adaptive Test methods is showing promise and an increasing level of interest in providing product performance related feedback to the wafer fabs. Example applications include optimizing the "sweet spot" for N and P device targets to meet customer demand distributions as well as providing direction in optimizing process modules for transistor-limited or R/C-limited performance improvement.

Adaptive Manufacturing (Post Fab)

An emerging direction is using test results to drive other IC production steps such as packaging multi-chip products. For example, the card/board assembly operation may require that specific dies or types of dies be used on specific boards based on previous test results. Given the emergence of multi-chip packages (such as 3D ICs) and power constraints, specific bare dies will need to be selected for assembly based on parametric data collected at test such as IDD or power/performance measurements. This opportunity is broader than just focusing on die build, and should include the entire post-fab supply chain including board, card, module and system manufacturing.

Key challenges of End-to-End data feed-forward for assembly operations include:

- Cross-company data management
- Build logistics for selecting specific dies/packages
- Robust data availability
- Data security
- Full traceability
- Data format standardization

Adaptive Test for Card/System/Field

Adaptive Test methodologies described in this section for IC-level testing can be equally extended and applied to board and system testing and even field usage. While ICs have traditionally been tested standalone in an almost 'noise-free' ATE environment and/or tested with limited structural tests to see whether they perform to their specifications, the board/system environment can be quite different in terms of noise, timing margin, voltage and functional test trigger conditions that structural tests were unable to produce. Improved board yield and IC DPM can be improved significantly where adaptive test that includes the board/system level performance is able drive enhanced screening both at the IC suppliers test and/or board/system manufacturing test.

The four types of Adaptive Test described (In-situ, Feed-forward, Feed-back and Post-test) can all be extended to include board and system manufacturing.

One of the difficulties in extending the chip-level adaptive test to board/system or even in-field test is to track their test trigger conditions and be able to convert between them. For example, chip-level scan-based logic gate test may not always be applicable for board/system/in-field tests due to the difficulties or impossibilities of controlling the scan chain data, clock pulse, non-stoppable in-field online function executions, etc. Similarly, a functional execution, which can be treated as a functional test, may be hard to convert to a chip-level ATE test because the function execution could involve memory contents, their transactions, logic and I/O data flow, etc. Therefore, tracking the test/failure conditions and the capability to convert between them is the key for adaptive test extension to board/system level.

A key emerging requirement is to enable full end-to-end correlation analysis – e.g., from fab data, through product die test, board/card/system test and field operation. The infrastructure to enable this capability broadly is one of the industry's key challenges.

Extending Adaptive Test applications to the board and system level requires extensive data infrastructure, analysis, exchange and security. Companies providing ICs, board design and test need to openly collaborate on a technical and business level to be successful.

The color scheme of the table below is:

- White – Manufacturing solutions exist today.
- Yellow – solutions are known – but there are still adoption hurdles
  - Solutions may be widely accepted or solutions may only be company-specific.
- Red – Research & development is needed to develop solutions
  - Or some solutions may only be proprietary and not generally available.

Challenge	Status	Needs
Recipe (Input variables, data treatments, output variables/ responses)	Many good outlier recipes exist. Spatial interpolation over a wafer is becoming popular for sample testing. Opportunity to branch test flow for only fault coverage required by current defect rate	Guidance on best measurements to make
		Guidance on which recipes to apply
		Fault or defect coverage metrics
		Higher level of adaptability where best variance model is automatically discovered instead of chosen beforehand
Decision Rule (Define actions resulting from recipe output)	Actions defined for gross outliers; loosely defined for less extreme events such as downgrade or reconfigure or escalation/ de-escalation of decisions (such as test sampling)	Where to set outlier thresholds
		How to combine the results of multiple outlier definitions (e.g., develop metrics for Quality or Reliability)
		Criteria for rejecting vs. downgrading or reconfiguring
Infrastructure (Foundation to enable execution of recipes and decision rules)	Part traceability enables feed-forward, feed-back but robust environment for data transport, storage and providence is lacking (no commercial solutions currently exist).	Standard data formats amenable to adaptive test
		Move from working with files to working with databases
		Ability to feed data and decisions both forward (with the parts to future stages) and backward (future parts at given stage) in test & assembly manufacturing flow
		Full traceability of adaptive test parameters for each part: limits, content, flows, decision rules, model parameters
		Full part configuration as tested (e.g., redundant cores, partial goods, on-chip tuning, multiple die such as 2.5D/3D in a package)
		Real-time communication among test cell machines and data storage and analysis engines
Evaluation (Execution of test cases to prove viability and benefit)	Receiver-operator curve concept understood by most practitioners but standard methods for experimental definition and ROI interpretation do not exist.	Clear evaluation criteria to build trust in adaptive test methods
		"Gold standard" against which to compare outliers (including all variations of adaptive test flows & settings)
		Good metrics for continuous monitoring of recipe effectiveness.
		Replay capability to evaluate new rules/recipes.
		Quantification of cost of shipping a bad part
Deployment (Implementation and release into production use)	Company-specific implementations currently utilized. But current deployments vary widely in their capabilities and there are still significant implementation hurdles to apply at all Test steps.	Commercial adaptive test platform into which methods can be plugged and recipes specified
		Connections to Manufacturing Execution Systems & Product Data Management systems
		Real-time (unit level) decision making that requires decisions based on off-tester analysis using broad set of data. (and update die result in real-time on the tester)
		Complete visibility across supply chain: fab, test, assembly both internal and external
		Supply chain data integration and processes which automatically detect supply chain issues and implement corrective actions in near real-time

Adaptive Test Challenges and Directions

This section highlights the key challenges that the industry must address to fully exploit Adaptive Testing across the supply chain.

Summary

Adaptive Testing has the opportunity to improve product quality & reliability, reduce cost and improve product yield beyond today's capabilities. Almost all companies are starting to use some forms of Adaptive Testing, but there is not a sequential roadmap for implementation and many applications are created in an ad-hoc way.

Adaptive Test methods are evolving over time as new technologies (<10nm, SOI), design methodologies (multichip/stack packaging) and supply chain support models are introduced.

There are a number of challenges that are today limiting the industry's ability to fully exploit Adaptive Testing across the supply chain. These are highlighted in the table in a previous section.

Test and Yield Learning In-Depth Analysis

In the normal sorting function, test provides the essential feedback loop for yield-learning. Product-based diagnostics, product-like test chips and parametric-sensitive test structures all play a key role.

Key Cost of Test Trends

Value derived from diagnostics of actual product hardware is driven by systematic defect mechanisms that are now increasingly complex functions of neighboring shapes, local pattern densities, etc. As a result, some failure mechanisms may be visible only on product. In addition, product-based diagnostics automatically places focus on key yield-limiting failure mechanisms. Volume-based diagnostics are important since individual occurrence of any given systematic defect mechanism may be rare. The pooling of data across many failing die can be important to identify true systematic defect mechanisms.

Product-like test chips can provide some of the same insight for yield-learning, but have the advantage of being available earlier, even when design is on-going. Specifically, rapidly designable, scalable and 100% testable & diagnosable test chips, with and without embedded memory and other key IP blocks, including fast automated design methodologies, are required to accelerate yield ramps and first-time yield success of complex SOCs. Such test chips should play the role of "send-aheads" and be designed on early foundry testsites even while the product design is ongoing. The test chip should be scalable, in that a complete SOC-style (optionally, timing-closed) design is possible with tens or hundreds of standard cells and with a small or large compiled memory and other IP blocks. The test chip should enable both logical and physical layout diversity in order to capture layout topologies found on real product chips. Finally, the test chip must be able to maintain a stable test and diagnosis infrastructure, meaning the same set of ATPG, diagnosis and failure analysis capabilities should be enabled whether the test chip is tiny ($<1mm^2$) or huge ($>100mm^2$).

In addition, parametric-related feedback is needed for (1) device and interconnect parameters and (2) design-process interactions. Measurement of device and interconnect parameters have traditionally relied upon test structures, especially scribe-line FETs and interconnect resistance and capacitance monitors. Increasing across-chip variation (intra-die variability) increases the negative impact of scribe-line-to-chip offsets. Moreover, test structures are limited by the number of configurations they can cover. Variations in configurations include both physical variations and electrical variations, such as different gate types and differences in load characteristics. As circuit parametrics are increasingly affected by such configurations, including within-standard-cell and transistor-layout configurations, it becomes necessary to base learning on product test or test of product-like layout configurations. Embedded, distributed monitor circuits such as thermal and VDD sensors, process-monitoring ring oscillators and critical path proxies are now standard on microprocessor-class ICs and can be used to help diagnose parametric fails and understand variability. Understanding variability includes unraveling the structure of variations into spatial and cross-parameter components (variation in transistor length, Vt, source-drain resistance, etc.) The spatial component includes both die-to-die and within-die components.

Cross-parameter variations, potentially including a spatial component, are important to analog/RF circuits, as well as digital. Methods for understanding/characterizing the manufacturing process and operating environment that are sufficiently sensitive for analog/RF are needed. Moreover, product test is uniquely well-suited to provide feedback on design-process interactions, including those leading to noise-related fails, such as power-grid droop and crosstalk fails.

Top challenges for test-based yield-learning include:

- Better resolution for cell-internal defects. Latest advances in structural testing and scan-based logic/layout-aware diagnosis methods are adequately addressing interconnect and via defects. Statistical approaches built into volume-based diagnostics are able to predict interconnect-related defect modes without an over-dependence on Physical Failure Analysis (PFA). Innovation is required, however, for cell-internal-defect-targeted diagnostics to be able to identify systematic fail modes inside standard cells. Observations derived from production silicon suggest a shift toward a larger percentage of the defect distribution being cell-internal defects, as opposed to interconnect-related. Current best methods for cell-internal defect diagnostics are cell truth-table and gate-exhaustive model-based, with the truth tables established via SPICE simulations of modeled cell-internal parasitics. These methods suffer from aliasing issues and over-reliance on potentially inaccurate modeling of cell-internal defects used in SPICE simulations. In addition, diagnosis resolution needs to be better due to limitations in the PFA process.
- Managing design data for yield learning. A tremendous amount of design data can be brought to bear for yield learning purposes, but it is often not organized effectively for this purpose. In addition, with hierarchical design and DFT flows, the overall management of this data at most companies today is
- ad-hoc, limiting its effective use.
- Inadequacy of LEF/DEF as the basis of layout-aware diagnosis. LEF/DEF suffices for the purposes of layout-aware ATPG but is too early in the design cycle to be used effectively for layout-aware diagnosis. LEF/DEF is less likely to closely resemble the final mask shapes due to complex OPC, boolean and retargeting steps.
- Yield-Learning in a OSAT/Fabless/Foundry environment. Yield-learning capabilities must be cognizant of the environment that has become the dominant model for our industry. If the technology cannot deal with the security and logistical concerns of this environment, it cannot be effective. Factory integration issues must be addressed. Data capture and management capabilities must support increasing reliance on statistical analysis and data mining of volume production data for yield-learning. Secure mechanisms for yield-data flow for distributed design, manufacture and test, including fabless/foundry and 3rd party IP, are needed. Standard test data formats, such as STDF-V4-2007 for scan fail data, and infrastructure to support their transmittal are needed to support automation and sharing of data. Specifically, data exchange standards are needed between the Fabless and the OSAT/Foundries to share system-level test feedback and correlation to wafer-level test and measurement data to (1) improve IC quality and reliability, (2) correlate process variations and parametric variability, and (3) reduce overkill. Distributed design, manufacture and test also creates an emerging role for methodologies and tools to help determine which areas that problems reside, e.g., design house, foundry or OSAT.
- Test for ZERO DPPM/Automotive in advanced node technologies. A change of mindset away from structural test coverage only is required to guarantee functional safety for automotive ICs. Mission-mode in-situ MBIST and LBIST and Design Failure Mode and Effects Analysis [DFMEA] are already part of ISO26262 (an automotive-specific set of standards for designing and testing electronics that focuses on safety critical components), but test architecture research is required to minimize the die-footprint increase due to added circuit redundancy. Moreover, Automotive may require root cause reports to be produced quickly for field failures. This requirement is another driver for rapid diagnosis and root cause analysis.
- Test and data-collection time increases due to longer scan chains. These increases drive a need for focus on LBIST methodologies and scan compression for both test and diagnosis.
- Faster Memory BIST bitmapping.
- Guidance for trading off test and data collection time against improved failure diagnostics.

References and Industry Links

Below is a list of references that provide information about methods and applications of Adaptive Testing.

Part Average Testing (PAT) is described in the AEC-Q001 documents at http://www.aecouncil.com/AECDocuments.html.

K. Huang, N. Kupp, C. Xanthopoulos, J.M. Carulli, Y. Makris, “Low-Cost Analog/RF IC Testing Through Combined Intra- and Inter-Die Correlation Models,” Design & Test, Volume 32, Issue 1, pp. 53-60, 2015.

A. Ahmadi, K. Huang, A. Nahar, B. Orr, M. Pas, J.M. Carulli Jr., Y. Makris, “Yield Prognosis for Fab-to-Fab Product Migration,” IEEE VLSI Test Symposium, Session 3B, p. 3.3, 2015.
S. Zhang, X. Li, R.D. Blanton, J. Machado da Silva, J.M. Carulli, K.M. Butler, “Bayesian Model Fusion: Enabling Test Cost Reduction of Analog/RF Circuits via Wafer-level Spatial Variation Modeling,” International Test Conference Proceedings, p. 19.1, 2014.
U. Guin, K. Huang, D. DiMase, J.M. Carulli Jr., M. Tehranipoor, Y. Makris, "Counterfeit Integrated Circuits: A Rising Threat in the Global Semiconductor Supply Chain," Proceedings of the IEEE, Volume 102, Issue 8, 2014.
Xanthopoulos, K. Huang, A. Poonawala, A. Nahar, B. Orr, J.M. Carulli Jr., Y. Makris, “IC Laser Trimming Speed-Up through Wafer-Level Spatial Correlation Modeling,” International Test Conference Proceedings, p. 19.2, 2014.
Ahmadi, K. Huang, S. Natarajan, J.M. Carulli Jr., Y. Makris, “Spatio-Temporal Wafer-Level Correlation Modeling with Progressive Sampling: A Pathway to HVM Yield Estimation,” International Test Conference Proceedings, p. 18.1, 2014.
Tikkanen, J.; Siatkowski, S.; Sumikawa, N.; Wang, L.-C.; Abadir, M.S., "Yield optimization using advanced statistical correlation methods," Test Conference (ITC), 2014 IEEE International , vol., no., pp.1,10, 20-23 Oct. 2014
K. Huang, N. Kupp, J. Carulli and Y. Makris "Handling discontinuous effects in modeling spatial correlation of wafer-level analog/RF tests", Proc. Design Autom. Test Eur. Conf., pp.553 -558 2013
K. Huang, N. Kupp, J. Carulli and Y. Makris "On combining alternate test with spatial correlation modeling in analog/RF ICs", Proc. IEEE Eur. Test Symp., 2013
S.K. Devarakond, S. Bhattacharya, J. McCoy, A. Nahar, J.M. Carulli, A. Chatterjee, “Predicting Die-to-Die Process Variations from Wafer Test Data: A Feasibility Study,” IEEE Latin American Test Workshop, April 2013.
K. Huang, N. Kupp, J.M. Carulli, Y. Makris, “Process Monitoring through Wafer-level Spatial Variation Decomposition,” International Test Conference Proceedings, p. 5.3, 2013.
C-K Hsu, F. Lin, K-T Cheng, W. Zhang, X. Li, J.M. Carulli Jr., K.M.. Butler, “Test Data Analytics - Exploring Spatial and Test-Item Correlations in Production Test Data,” International Test Conference Proceedings, p. 5.2, 2013.
K. Huang, J.M. Carulli, Y. Makris, “Parametric Counterfeit IC Detection via Support Vector Machines,” International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems, p. 1.1, 2012.
N. Kupp, K. Huang, J. Carulli and Y. Makris "Spatial correlation modeling for probe test cost reduction", Proc. IEEE/ACM Int. Conf. Comput.-Aided Design, pp.23 -29 2012
N. Kupp, K. Huang, J.M. Carulli, Y. Makris, “Spatial Estimation of Wafer Measurement Parameters Using Gaussian Process Models,” International Test Conference Proceedings, p. 5.1, 2012.
K. R. Gotkhindikar, W.R. Daasch, K.M. Butler, J. M. Carulli Jr., A. Nahar, “Die-level Adaptive Test: Real-Time Test Reordering and Elimination,” International Test Conference Proceedings, p. 15.1, 2011.
Sumikawa, N.; Drmanac, D.G.; Wang, Li.-C.; Winemberg, L.; Abadir, M.S., "Forward prediction based on wafer sort data — A case study," Test Conference (ITC), 2011 IEEE International , vol., no., pp.1,10, 20-22 Sept. 2011
Sumikawa, N.; Drmanac, D.; Li-C Wang; Winemberg, L.; Abadir, M.S., "Important test selection for screening potential customer returns," VLSI Design, Automation and Test (VLSI-DAT), 2011 International Symposium on , vol., no., pp.1,4, 25-28 April 2011
Drmanac, D.; Sumikawa, N.; Winemberg, L.; Wang, L.-C.; Abadir, M.S., "Multidimensional parametric test set optimization of wafer probe data for predicting in field failures and setting tighter test limits," Design, Automation & Test in Europe Conference & Exhibition (DATE), 2011 , vol., no., pp.1,6, 14-18 March 2011
Sumikawa, N.; Drmanac, D.; Wang, Li.-C.; Winemberg, L.; Abadir, M.S., "Understanding customer returns from a test perspective," VLSI Test Symposium (VTS), 2011 IEEE 29th , vol., no., pp.2,7, 1-5 May 2011
W. Zhang "Virtual probe: A statistical framework for low-cost silicon characterization of nanoscale integrated circuits", IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 30, no. 12, pp.1814 -1827 2011
Drmanac, D.; Laisne, M.; Wang, L.C., "Wafer probe test cost reduction of an RF/A device by automatic testset minimization — A case study," Test Conference (ITC), 2011 IEEE International , vol., no., pp.1,10, 20-22 Sept. 2011
S. Reda and S. R. Nassif "Accurate spatial estimation and decomposition techniques for variability characterization", IEEE Trans. Semicond. Manuf., vol. 23, no. 3, pp.345 -357 2010
E. Marinissen, A. Singh, D. Glotter, M. Esposito, J. Carulli, A. Nahar, K. Butler, D. Appello, and C. Portelli, "Adapting to adaptive testing," Design, Automation and Test in Europe Conference & Exhibition (DATE), pp. 556-561, 2010.
Chen, J.; Jing Zeng; Wang, L.-C.; Mateja, M., "Correlating system test fmax with structural test fmax and process monitoring measurements," Design Automation Conference (ASP-DAC), 2010 15th Asia and South Pacific , vol., no., pp.419,424, 18-21 Jan. 2010
Chen, J.; Jing Zeng; Wang, Li.-C.; Mateja, M.; Rearick, J., "Predicting multi-core system Fmax by data-learning methodology," VLSI Design Automation and Test (VLSI-DAT), 2010 International Symposium on , vol., no., pp.220,223, 26-29 April 2010
D. Mannath "Structural approach for built-in tests in RF devices", Proc. Int. Test Conf., 2010
Chen, J.; Wang, Li.-C.; Po-Hsien Chang; Jing Zeng; Yu, S.; Mateja, M., "Data learning techniques and methodology for Fmax prediction," Test Conference, 2009. ITC 2009. International , vol., no., pp.1,10, 1-6 Nov. 2009
Drmanac, D.; Bolin, B.; Wang, L.-C.; Abadir, M.S., "Minimizing outlier delay test cost in the presence of systematic variability," Test Conference, 2009. ITC 2009. International , vol., no., pp.1,10, 1-6 Nov. 2009

K.M. Butler, J.M. Carulli, J. Saxena, A. Nahar, R. Daasch, “Multidimensional Test Escape Rate Modeling,” Design & Test of Computers, Volume 26, Issue 5, pp. 74-82, 2009.
A. Nahar, K. Butler, J. Carulli, and C. Weinberger, "Quality improvement and cost reduction using statistical outlier methods," IEEE International Conference on Computer Design, pp. 64-69, 2009.
A. Nahar, K.M. Butler, J.M. Carulli, C. Weinberger, “Statistical Outlier Method Applications”, IEEE International Workshop on Defect and Data-Driven Testing, 2009.
Wu, S.H.; Drmanac, D.; Wang, Li.-C., "A Study of Outlier Analysis Techniques for Delay Testing," Test Conference, 2008. ITC 2008. IEEE International , vol., no., pp.1,10, 28-30 Oct. 2008
R. Aitken, "Defect or Variation? Characterizing Standard Cell Behavior at 90 nm and Below," IEEE Transactions on Semiconductor Manufacturing, vol. 21, pp. 46-54, 2008.
H.-G. Stratigopoulos and Y. Makris "Error moderation in low-cost machine-learning-based analog/RF testing", IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 27, no. 2, pp.339 -351 2008
F. Ferhani, N. Saxena, E. McCluskey, and P. Nigh, "How Many Test Patterns are Useless?" VLSI Test Symposium, pp. 23-28, 2008.
K.M. Butler, J.M. Carulli, J. Saxena, “Modeling Test Escape Rate as a Function of Multiple Coverages,” International Test Conference Proceedings, p. 21.2, 2008.
F. Liu "A general framework for spatial correlation modeling in VLSI design", Proc. Design Autom. Conf., pp.817 -822 2007
L. Fang, M. Lemnawar, and Y. Xing. Cost Effective Outliers Screening with Moving Limits and Correlation Testing for Analogue ICs. In Proceedings IEEE International Test Conference (ITC), October 2006. Paper 31.2.
T.J. Anderson, J.M. Carulli, “Modeling & Monitoring of Product DPPM with Multiple Fail Modes,” International Reliability Physics Symposium, p. 545, 2006.
K. M. Butler, S. Subramaniam, A. Nahar, J. M. Carulli Jr., T. J. Anderson, W. R. Daasch, "Successful Development and Implementation of Statistical Outlier Techniques on 90nm and 65nm Process Driver Devices," Proc. 2006 Int. Reliability Physics Symp., pp. 552-559, Oct. 2006.
J.M. Carulli, T.J. Anderson, “The impact of multiple failure modes on estimating product field reliability,” Design & Test of Computers, Volume 23, Issue 2, p. 118, 2006.
A. Nahar, R. Daasch, and S. Subramaniam, "Burn-in Reduction Using Principle Component Analysis," Proc. 2005 IEEE Int. Test Conf., Paper 7.2, Nov. 2005.
L. Ning, A. Nahar, R. Daasch, K. M. Butler, J. M. Carulli Jr., S. Subramaniam, "Burn-in Reduction using Robust Canonical Correlation Analysis," Proc. SRC TECHCON 2005, Paper 9.1, Oct. 2005.
Z. Yuan and Y. Yang "Combining linear regression models: When and how?", J. Amer. Stat. Assoc., vol. 100, no. 472, pp.1202 -1214 2005
R. Turakhia, B. Benware, R. Madge, T. Shannon, R. Daasch, "Defect Screening Using Independent Component Analysis on IDDQ," Proc 2005 IEEE VLSI Test Symp., pp. 427-432, May 2005.
W. C. Riordan, R. Miller, E. R. St. Pierre, "Reliability Improvement and Burn In Optimization Through the use of Die Level Predictive Modeling," Proc. 2005 IEEE Int. Rel Physics Symp., pp. 435-445, Apr. 2005.
R. Madge, B. Benware, R. Turakhia, R. Daasch, C. Schuermyer, and J. Ruffler, "In search of the optimum test set - adaptive test methods for maximum defect coverage and lowest test cost," Proceedings International Test Conference, pp. 203-212, 2004.
S.S. Sabade, D. M. H. Walker, "CROWNE: Current Ratio Outliers with Neighbor Estimate", DFT 2003, pp 132-139.
C. Schuermyer, B. Benware, K. Cota, R. Madge, R. Daasch, L. Ning, "Screening VDSM Outliers Using Nominal and Subthreshold Supply Voltage IDDQ," Proceedings IEEE Int. Test Conference, 2003, pp. 565-573, Sep 2003.
Automotive Electronics Council, "Guidelines for Part Average Testing (PAT)," AEC Q001, rev. C, 18 July 2003, http://www.aecauncil. comAECDocuments.html.
P. Buxton, P. Tabor "Outlier Detection for DPPM Reduction," Proceedings IEEE Int. Test Conference, 2003, pp. 818-827, Sep-Oct 2003.
T.S. Barnett and A.D. Singh. Relating Yield Models to Burn-In Fall-Out in Time. In Proceedings IEEE International Test Conference (ITC), pages 77-84, October 2003.
S.S. Sabade, D. M. Walker, "Evaluation of Effectiveness of Median of Absolute Deviations Outlier Rejection-based IDDQ Testing Burn-in Reduction" Proceedings 2002 VLSI Test Symp., pp. 81-86, Apr-May 2002.
D. I. Bergman, H. Engler, "Improved IDDQ Testing with Empirical Linear Prediction", Proc. 2002 IEEE Int. Test Conf, page 954, Nov. 2002.
W.R. Daasch, J. McNames, R. Madge, and K. Cota. Neighborhood Selection for IDDQ Outlier Screening at Wafer Sort. IEEE Design & Test of Computers, 19(5):74-81, September-October 2002.
W. R. Daasch, J. McNames, R. Madge and K. Cota "outlier screening at wafer sort", IEEE Design Test Comput., vol. 19, no. 5, pp.74 -81 2002
P. N. Variyam, S. Cherubal and A. Chatterjee "Prediction of analog performance parameters using fast transient testing", IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 21, no. 3, pp.349 -361 2002

T.S. Barnett, A.D. Singh, M. Grady, and K. Purdy. Redundancy Implications for Early-Life Reliability: Experimental Verification of an Integrated Yield-Reliability Model. In Proceedings IEEE International Test Conference (ITC), pages 693-699, October 2002.
J. Saxena, K. M. Butler, J. Gatt, Raghuraman R., S. P. Kumar, S. Basu, D. J. Campbell, J. Berech, "Scan-Based Transition Fault Testing: Implementation Challenges," Proc. 2002 IEEE Int. Test Conf., pp. 1120-1129, Oct. 2002.
R. Madge et al. Screening MinVDD Outliers Using Feed-Forward Voltage Testing. In Proceedings IEEE International Test Conference (ITC), pages 673-682, October 2002.
R. Madge, M. Rehani, K. Cota, and W.R. Daasch. Statistical Post-Processing at Wafer Sort - An Alternative to Burn-In and a Manufacturable Solution to Test Limit Setting for Sub-Micron Technologies. In Proceedings IEEE VLSI Test Symposium (VTS), pages 69-74, May 2002.
T.S. Barnett, A.D. Singh, M. Grady, and K. Purdy. Yield-Reliability Modeling: Experimental Verification and Application to Burn-In Reduction. In Proceedings IEEE VLSI Test Symposium (VTS), pages 75-80, May 2002.
S.S. Sabade, D.M.H. Walker, "Improved wafer-level spatial analysis for IDDQ limit setting, Proc. 2001 IEEE Int. Test Conf., pp 82-91, Nov. 2001.
R. Daasch, K. Cota, J. McNames, R. Madge, "Neighbor Selection for Variance Reduction in IDDQ and Other Parametric Data" Proceedings IEEE Int. Test Conference, 2001, pp. 92-100, Oct 2001.
S. Benner and O. Boroffice, "Optimal production test times through adaptive test programming", Proceedings International Test Conference, pp. 908-915, 2001.
R. B. Miller, W. C. Riordan, "Unit Level Predicted Yield: A Method of Identifying High Defect Density Die at Wafer Sort," Proc 2001 IEEE Int. Test Conf., pp. 1118-1127, Oct.-Nov. 2001.
K. Butler and J. Saxena, "An empirical study on the effects of test type ordering on overall test efficiency," Proceedings International Test Conference, pp. 408-416, 2000.
E. Riess, "Automatic Monitoring of Electrical Parameters in the Semiconductor Industry Based on ROC," IEEE Trans. On Sys., Man, and Cybernetics-Part A: Sys. And Humans, vol. 30, No. 6, pp. 853-857, Nov. 2000.
C. Thibeault, "Diagnosis Method Using AIDDQ Probabilistic Signatures: Theory and Results", Journal of Electronic Testing: Theory and Applications 2000, Vol 4., pp 339-353.
A. Kinra, H. Balachandran, R. Thomas, J.M. Carulli, “Logic mapping on a microprocessor,” International Test Conference Proceedings, p. 701, 2000.
W. R. Daasch, J. McNames, D. Bockelman, K.Cota, R. Madge, "Variance Reduction Using Wafer Patterns in IDDQ Data" Proceedings IEEE Int. Test Conference, 2000, pp. 189-198, Oct 2000.
J.M. Carulli Jr., D.C. Wrobbel, A. Mehta, K.E. Krause Jr., B.E. Campbell, F.A. Valente, “Frequency Distribution Modeling for High-Speed Microprocessors Using On-chip Ring-oscillators,” SPIE Proceedings, Inline Methods & Monitors for Process & Yield Improvement, p. 146, 1999.
A. E. Gattiker, W. Maly, "Current Signatures: Application," Proc. 1998 IEEE Int. Test Conf, pp. 1168-1177, Oct. 1998.
B. Stine, D. Boning, and J. Chung, "Analysis and decomposition of spatial variation in integrated circuit processes and devices," IEEE Transactions on Semiconductor Manufacturing, vol. 10, pp. 24-41, 1997.
A. Singh, P. Nigh, and C. M. Krishna, "Screening for known good die (KGD) based on defect clustering: An experimental study," in Proceedings International Test Conference, 1997, pp. 362-371.
A.D. Singh, P. Nigh, and C.M. Krishna. Screening for Known Good Die based on Defect Clustering: An Experimental Study. In Proceedings IEEE International Test Conference (ITC), pages 324-331, November 1997.
T. W. Williams, R. H. Dennard, R. Kapur, M. R. Mercer, W. Maly, "IDDQ Test: Sensitivity Analysis of Scaling," Proc. 1996 IEEE Int. Test Conf, pp. 786-792, Oct. 1996.
A. Singh and C. Krishna, "On the effect of defect clustering on test transparency and IC test optimization," IEEE Transactions on Computers, vol. 45, no. 6, pp. 753-757, Jun. 1996.
A.D. Singh and C.M. Krishna. On Optimizing VLSI Testing for Product Quality Using Die Yield Prediction. IEEE Transactions on Computer-Aided Design, 12(5):693-709, May 1993.
J. M. Soden, C. F. Hawkins, R. K. Gulati, and W. Mao, "IDDQ Testing: A Review," J. Electronic Testing:Theory and Applic. (JETTA), vol.3, no.4, pp. 291-303, Dec. 1992.
C. Crapuchettes, "Testing CMOS IDD on Large Devices," Proc. 1987 IEEE Int. Test Conf., pp. 310-315, Sep. 1987.

Industry Links
CAST www.semi.org/en/collaborative-alliance-semiconductor-test
DR Yield dryield.com
Optimal+ www.optimalplus.com
PDF Solutions www.pdf.com
Mentor Graphics (previously Galaxy) www.mentor.com/products/silicon-yield/quantix/
Qualtera www.Qualtera.com

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