HIR Annual Conference Huge Success

The Heterogeneous Integration Roadmap (HIR) 7th Annual Conference

The Heterogeneous Integration Roadmap (HIR) 7th Annual Conference, held at the auditorium of the Samsung Electronics Campus North First Street San Jose California on February 21-23, 2024, was a huge success.

Day 1

The conference started on Wednesday February 21st 1 pm devoting the entire afternoon to describing the US National Advanced Packaging and Manufacturing and Project (NAPMP). The keynote speaker was NAPMP Director Professor Professor Subramanian S. Iyer, Chair Professor at UCLA, on assignment to NIST to lead the US CHIP Act program.

Along with Prof. Iyer, we had invited three distinguished panelists to join in a roundtable fireside chat following the keynote presentation. They were: Ajit Manocha, President and CEO of SEMI and formerly CEO of Global Foundry, Nicky Lu, CEO and founder of Etron, long time industry veteran and member of the Taiwan SIA, and Tim Lee president-elect of IEEE USA, Boeing Fellow and chairs of two HIR Technical Working Groups (TWG). Ajit and Nicky both serve on HIR Global Advisory Council. William (Bill) Chen and Ravi Mahajan served as moderators for this afternoon program.

The conference room was filled with every seat taken (see attached photo) and standing room at the entrance corridor for the entire program. In 60 minutes and 27 slides Professor Iyer covered his vision for Advanced Packaging and Manufacturing in establishing electronics ecosystem from co-design to finished goods in United States.

In the fireside chat, Ajit Manocha reiterated SEMI's strong support for the HIR effort and his commitment to help drive the evolution of the roadmap. Prof. Iyer highlighted the need to create a quantified roadmap analogous to the earlier ITRS effort. Nicky Lu pointed out the value of

innovation and how innovation in HI could drive the roadmap forward. Tim Lee highlighted IEEE support of the roadmap.

Day 2 and Day 3 Programs

The conference on Thursday and Friday took place at the large auditorium. On Thursday the HIR conference started with welcome, agenda review, followed by an acknowledgement of the conference HIR Techncial Program committee working in collaboration with the EPS Santa Clara Valley Chapter who worked behind the scene in making sure that all logistics including from internet connectivity, registration to coffee breaks, box lunches, wine tasting and other logistics items were taken care of and worked smoothly without a hitch.

The agenda for Thursday and Friday are organized each day with four (4) keynote presentations in the morning and technical working group (TWG) presentations in the afternoon.

Day 2 and Day 3 Keynote Presentations

For the two days the eight keynotes speakers and their presentation titles are:

- Woopoung Kim/ Moonsoo Kang (Samsung) “Advanced Packaging in the Era of HPC and AI” described their plans for scaling memory performance for HPC/AI & Mobile AI and how interconnects in these memories scale.
- Alan Smith (AMD) “AMD Instinct^{TM} MI300 Series Modular Chiplet Package – HPC and AI Accelerator for Exa-Class Systems” spoke about how chipletization and interconnect scaled HI is driving performance.
- Carl McCants (DARPA) “Challenges and Opportunities in Manufacturing 3-Dimensional Heterogeneously Integrated (3DHI) Microsystems” described how DARPA is pushing the frontiers of 3D HI.
- SV Sreenivasan / John Schreck (Texas Institute of Electronics (TIE), UT Austin)“Creating a Wafer-level 3DHI R&D and Prototyping Facility” introduced the TIE effort to the HIR community and described how they are scaling HI with a broad scope effort on physical scaling enabled by equipment, materials and process scaling.
- Wei-Chung Lo / Shih-Chieh Chang (ERSO-ITRI, Taiwan) “Collaboration in Advancing Advanced Packaging Manufacturing in Heterogeneous Integration in ITRI” described research vectors and industry academia collaboration pursued at ITRI.
- Robert Wisniewski (Samsung) “The Importance of Tight Coupling for Performance and Productivity” spoke about memory and communication walls and how HI in all three dimensions could help bridge performance gaps.
- Josh Fryman (Intel), “Future architecture demands for more aggressive packaging” built on the ideas Prof Iyer had discussed and challenged the community to think deeper to evolve significantly more innovative architectures to improve computing.

- Erik Jung / Albert Heuberger (Fraunhofer Institutes Germany) “Advance Heterogenous Integration as a core activity in the European ChipsJU Initiative" described EU funded “Chip” initiatives to evolve HI.

Note 1: when there are two names listed the first name delivered the presentation.

Day 2 and Day 3 HIR TWG Presetnations

The afternoon sessions on Day 2 & Day 3, we invited each of the HIR Technical Working Groups to make a 10 minutes presentation of their Technical Focus, followed by 30 – 40 minutes interactive dialogue on collaboration across the TWGs with the goal to multiply mutually the value of their Roadmap Chapters output.

While we invited each TWG to deliver their talk in-person, there were a few TWG chairs who had to cancel their talk at the last minute due to schedule conflicts. In two cases the talks were delivered on-line.

Team 1 Thursday February 22, 2024. 1:00pm – 2:30 pm

- Aerospace & Defense: Tim Lee , Dan Blass
- 5G Communications & Beyond: Tim Lee , Herbert Bennett
- Thermal Management: Weihua Tang, Madhu Iyengar , Azmat Malik, Yin Hang
- Co-Design: Jose E. Schutt-Aine
- Test: Jeorge Hurtarte, Ken Butler
- Integrated Power Electronics: Francesco Carobolante, Patrick McCluskey, Douglas Hopkins

Team 2 Thursday February 22, 2024. 2:40 pm to 4:10 pm

- High Performance Computing & Data Centers:John Shalf, Kanad Ghose
- 2D-3D Interconnect: Ravi Mahajan ,
- Modelling & Simulation: Chris Bailey , Xuejun Fan
- Automotive: Vikas Gupta, Veer Dhandapani
- Additive Electronics Manufacturing: Kris Erickson

Team 3 Friday February 23, 2024

- SiP & Module: Erik Jung, Rolf Aschenbrenner , Klaus Pressel
- MEMS & Sensors Integration: Benson Chan, Mary-Ann Maher, Shafi Saiyed ,
- Advanced Manufacturing & Multi Chip Integration Annette Teng & William Chen
- Supply Chain: Kitty Pearsel, Melissa Grupen Shemansky Paul Trio , Siva Sivasankar

- Integrated Photonics, Amr Helmy, Bill Bottoms
- Cyber Security: Sohrab Aftabjahani

Team 4 Friday February 23, 2024

- Medical, Health & Wearables: Benson Chan, Mark Poliks , Nancy Stoffel , Jan Vardaman
- IoT: Rockwell Hsu, Robert Lo
- Mobile: Benson Chan , William Chen
- Reliability Richard Rao, Abhijit Dasgupta, & Shubha Sahasrabudhe
- Emerging Research Devices: Meyya Meyyapan

Note 2: when there are more than one name listed the first name delivered the presentation.

HIR Annual Conference planning and organization

We had two teams working in close collaboration.

Technical Program Team (HIR TWGs): Ravi Mahajan, John Shalf, Tim Lee, Amr Helmy, Melissa Groupen Shemansky, Bill Chen and Denise Manning

Arrangement Team: (EPS SCA Chapter) Chandan Bhat, Jin Yang, Azmat Malik, Annette Tang, Luu Nguyen, Venkatesh Avula, Denise Manning, Sangnam Jeong

Registration for this in-person event was 187.

We wish to acknowledge our sincere debt of gratitude to both teams for the huge success of the 7th Annual HIR Conference. In particular we wish to thank Denise Manning for managing the presentations, Azmat Malik for registration management and to Jin Yang for arranging the Samsung conference facilities. We wish to express our appreciation to Samsung for the use of their conference venue and to ASE for sponsorhsip.