2024 ECTC HIR Workshop

Challenges and innovations in Thermal Engineering from form Fan-Out to 2.5D and 3D stacking

*Thermal challenges for stacked die systems:*
*Need for multi-scale thermal analysis*

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Advanced 3D integration trends

Both technology directions rely on Si substrate thinning / removal
The 3D interconnect technology landscape

3D-SIP
- Package stacking
  - Multi-die Packaging
  - Interposer “2.5D”
  - Embedded Die

3D-SIC
- Die Stacking µbump
- Die Stacking Hybrid bonding

3D-SOC
- Wafer-to-Wafer Hybrid bonding
- Dielectric bonding µTSV
- Wafer-to-Wafer Sequential
- BSPDN

3D-IC
- Transistor Stacking

3D Interconnect Pitch scaling

1mm 400µm 100µm 40µm 20µm 10µm 4µm 2µm 1µm 500nm 100nm

3D Interconnect Density (#/mm²)

1 10 10² 10³ 10⁴ 10⁵ 10⁶ 10⁷ 10⁸

Source: Eric Beyne (imec)

Scaling towards higher interconnect density / smaller pitch
The backside PDN concept enables:

- Use of fine line BEOL for signal interconnect (reduces routing congestion)
- Increases the effective chip-area utilization
- Strongly (10x) reduces the PDN resistance from package-to-transistor

Results in strongly enhanced system performance
3D Technology:

Through-Silicon-Via Connections

a.k.a. TSV’s
TSV Scaling TREND: Si thickness scaling to reduce AR

Source: Eric Beyne (imec)
Future vision: CMOS 2.0

Self-heating concerns $\Rightarrow$ accurate thermal models needed for the assessment of thermal mitigation solutions

https://www.nature.com/articles/s44287-023-00016-3

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Thermal impact of Si thinning

- Thermal spreading problem
- Spreading resistance depends on heat source size and boundary conditions
Thermal impact of Si thinning

- Reduced lateral thermal spreading due to Si substrate thinning / removal
- Spreading resistance depends on heat source size and boundary conditions

Small local heat source: 3X self-heating increase

Large heat source: small impact of Si thinning

Detailed power distribution map needed for relevant analysis
Powermap granularity requirements

80 core SOC test case

- Higher powermap resolution required for very thin / no Si configurations
- Brute force simulation of complete SOC at fine resolution not realistic
- Need for multi-scale simulation methodology
Need for multi-scale thermal analysis

WHOLE THERMAL PATH FROM HEAT SOURCES TO THE COOLING SOLUTION TO BE CONSIDERED:

- Thermal transport at different time and length scales
- Different tools used at different scales
- No single tool available across all scales
Device level thermal simulations (Monte Carlo BTE)

IN-HOUSE SIMULATOR SUITE

ATOMISTIC THEORY (DFT)
crystal unit cell
interatomic forces

HEAT CARRIER PROPERTIES
dispersions
group velocities
lifetimes

MONTE CARLO SIMULATION
numerical solution of thermal BTE

IN-PROFILE REFERENCE

HEAT SOURCE
particle emission
intrinsic scattering

interface transm/refl
specular reflection

STOCHASTIC TRAJECTORY
intrinsic scattering
diffuse re-emission
particle absorption

ISOTHERMAL HEAT SINK

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Device level thermal simulations (Monte Carlo BTE)

Device level validation

Extraction of effective thermal properties

Heat source

Heat sink

Measurements
- Group mean
- Single device observation

Interval $1\sigma$ $2\sigma$

Monte Carlo simulation

Nanoscale transport effects

Diffusive simulation

Self-heating in gate line ($^\circ$C) @ 1mW total power

Effective conductivity (W/m-K)

Number of fins

Thickness (nm)

Si
Cu
Ru

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Multi-scale analysis attempts: example 1

Commercial tool: sub-modeling technique (global – local)

- Global package level model with effective properties for BEOL, BSPDN, FEOL
- Local model with detailed BSPDN and power distribution map

- Validation of global – local model with huge package level reference model with all detail shows reasonable agreement

- For the required level of geometrical detail, methodology hits the limits to capture local gradients
Multi-scale analysis attempts: example 2

Cell-level hot spots vs SOC-level temperature distribution

SOC background temperature

- Functional regions ~1mm²
- Power densities ~100 W/cm²
- Simulation resolution ~10μm

Cell-level hotspots

- Footprints < 1μm²
- Channels ~ 5nm x 10nm
- Power densities ~50,000 W/cm²
- Simulation resolution ~1nm

Clock buffer cell
Multi-scale analysis attempts: example 2

Refined layers with effective conductivity for hotspot assessment

3D Monte Carlo simulation with uniform planar heat dissipation → Extraction of effective (cross-plane) conductivity

Heat source
Si substrate

Refined layer sequences for hotspot assessments

Lumped Si
Lumped BEOL

+ 11°C
100 nm
100 nm

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Summary

- 3D interconnect density scaling and BSPDN introduce significant Si substrate thinning or even removal

- Thermal analysis consequences:
  - Thermal impact of Si thinning, or heat spreading improvement solutions depends on the power distribution and cooling scenario assumptions
  - Thin Si / no Si configurations are more sensitive to the power map sampling resolution → detailed, high-resolution power map needed
  - Partial multi-scale thermal models show significant impact of local features on package level thermal models

- Clear need for:
  - Efficient multi-scale thermal analysis methodologies and experimental validation
  - Availability of relevant power maps
  - Experimental validation of device self-heating in thinned Si
Questions?

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