HETEROGENEOUS INTEGRATION ROADMAP

Co-Design for Heterogeneous Integration

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Brain-Inspired AI Chiplets

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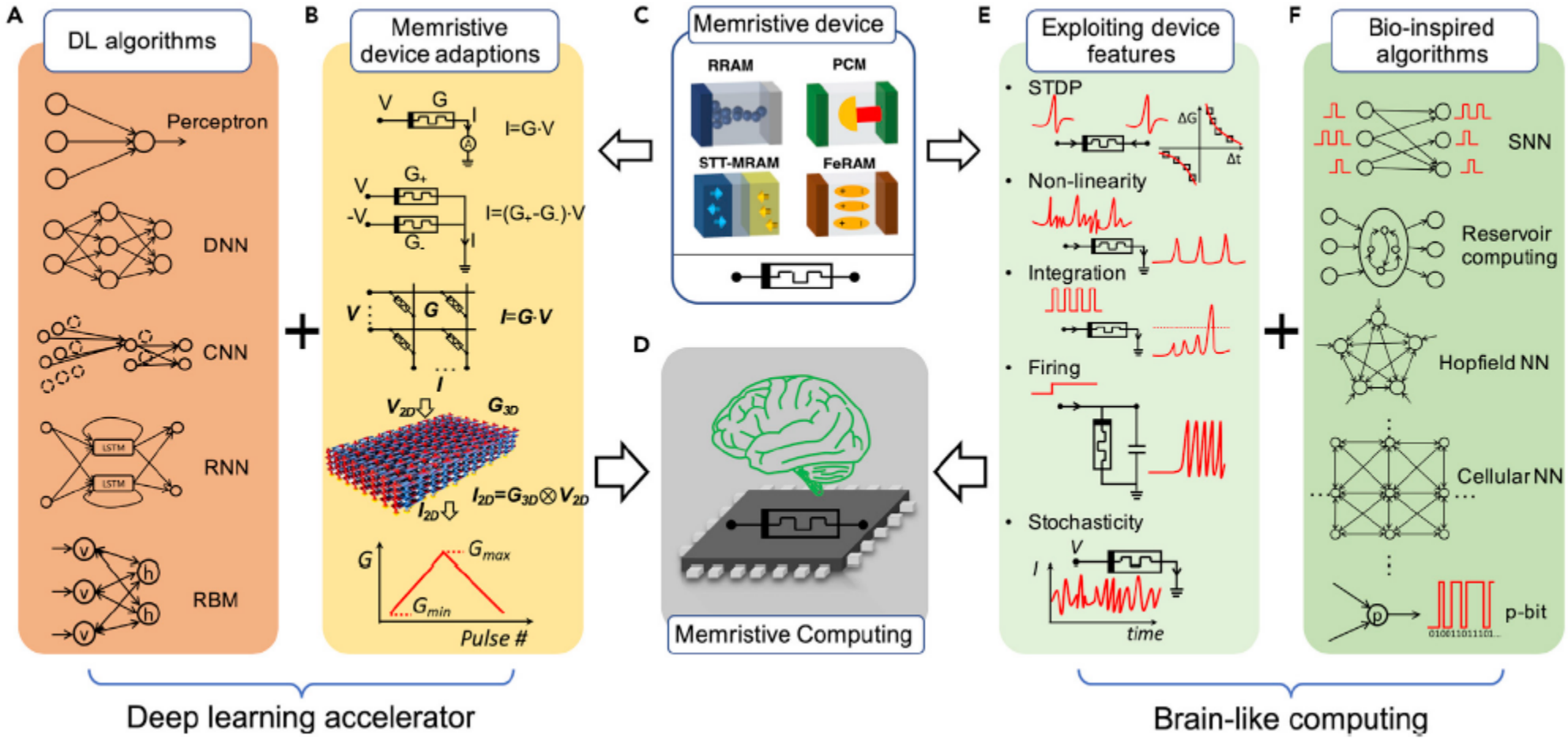

SOURCE: Wei Wang, Wenhao Song, Peng Yao, Yang Li, Joseph Van Nostrand, Qinru Qiu, Daniele Ielmini and J. Joshua Yang, "Integration and Co-design of Memristive Devices and Algorithms for Artificial Intelligence", *iScience 23, 101809*, December 18, 2020

The Problem of Disagreggation

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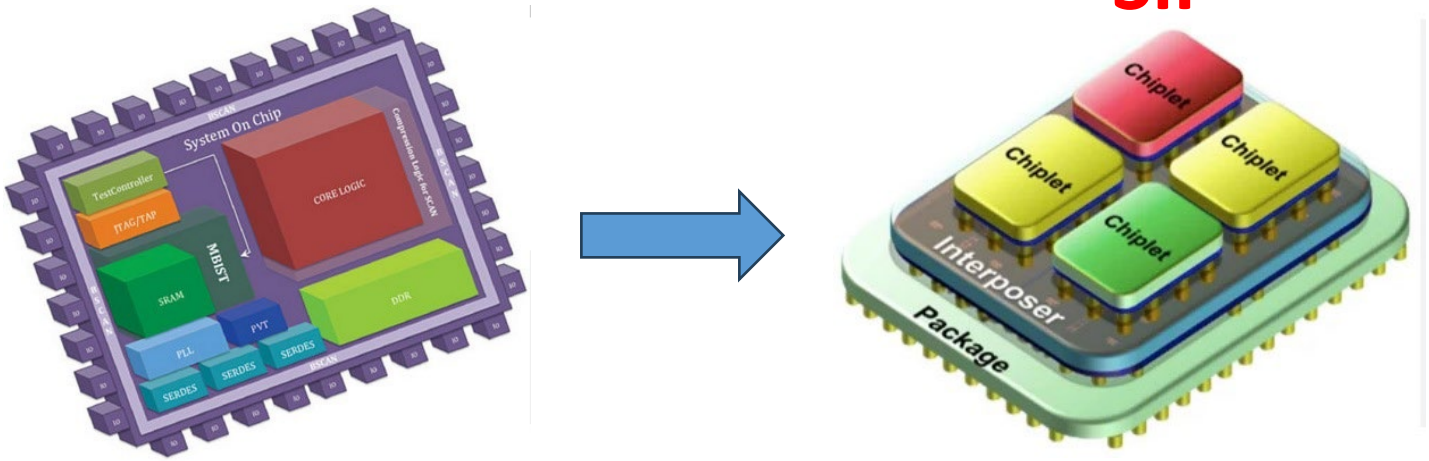
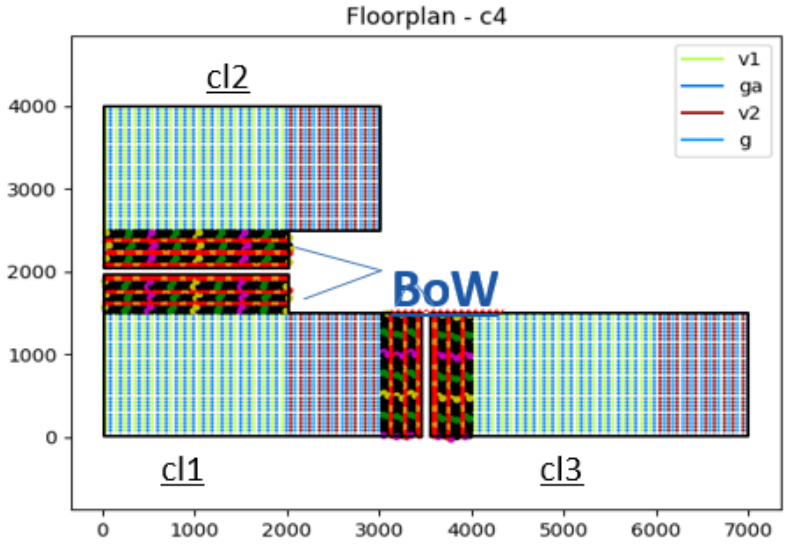
Architecting an IC as a chiplet-based SiP rather than a SoC is referred to as disaggregation of function. Today, it is performed *ad hoc*; there is no established methodology to optimize the disaggregation, i.e., to determine how many separate chiplets should be used in order to meet specifications. Once chiplet design is democratized, there will be more choices from different vendors which could make the process more chaotic.

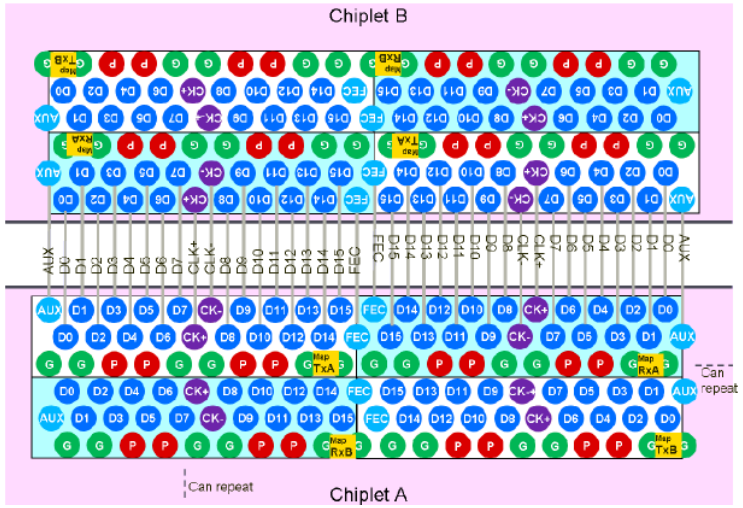
SOC **SiP**



Automating Disagreggation

- Implement co-design into EDA tools
- Assist with AI/ML
- Integrate interconnection standards (e.g. UciE, BoW)





[1] Shahab Ardalan, Ramin Farjadrad,Mark Kuemerle,Ken Poulton,Suresh Subramaniam, Bapiraju Vinnakota, "Chiplet Communication Link: Bunch of Wires (BoW)", IEEE Micro, Jan/Feb 2021

The Co-Design Challenge

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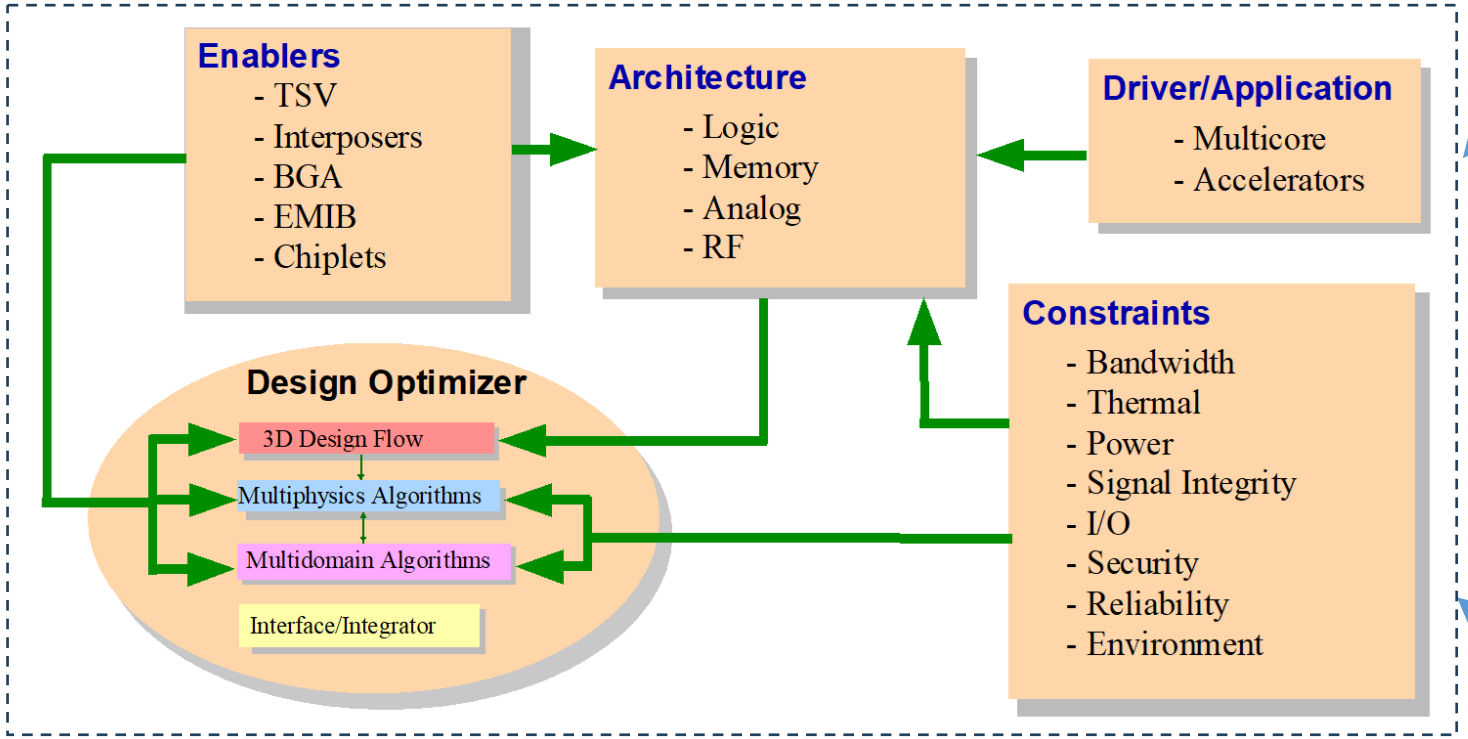
TESTING

Reliability



Security

Interoperability

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Co-Design Challenges

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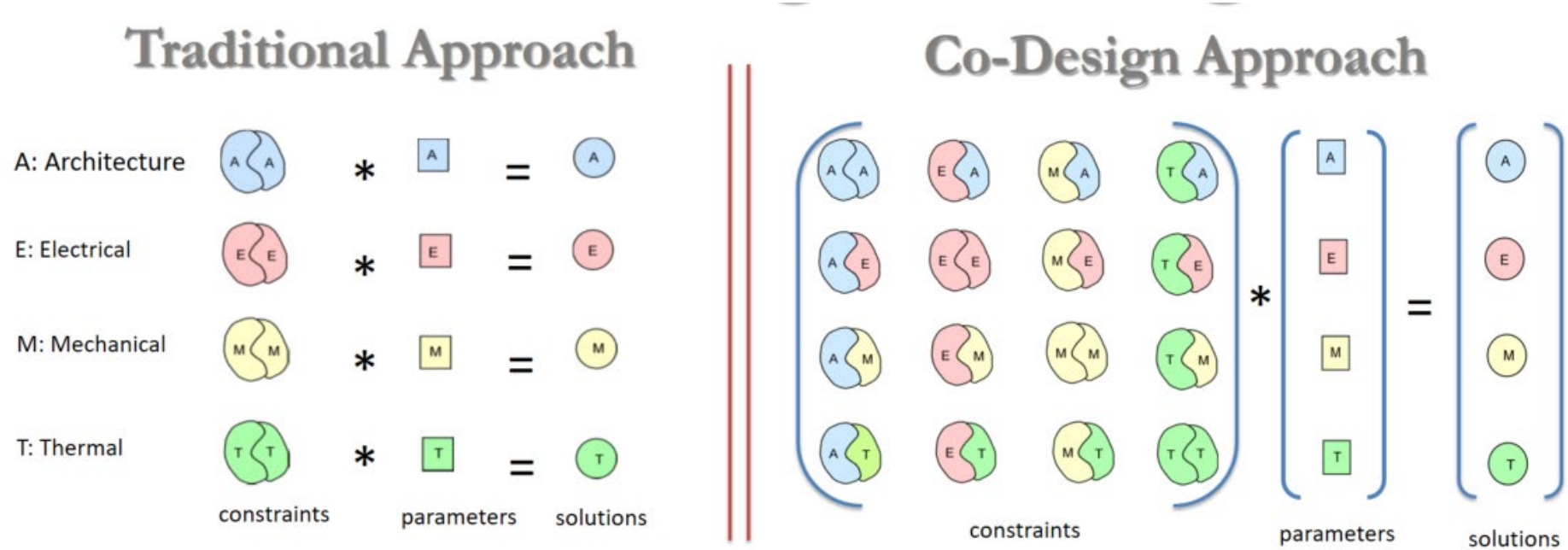
Current co-design methods are simply a cascade or combination of independent solutions. Real co-design requires concurrent solution from a formulation that accounts for all multi-physics interactions while embodying conflicting requirements



Constraints

- Bandwidth
- Thermal
- Power
- Signal Integrity
- I/O
- Security
- Reliability
- Environment
- Size
- Cost

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Power Delivery for Chiplet-Based SiP

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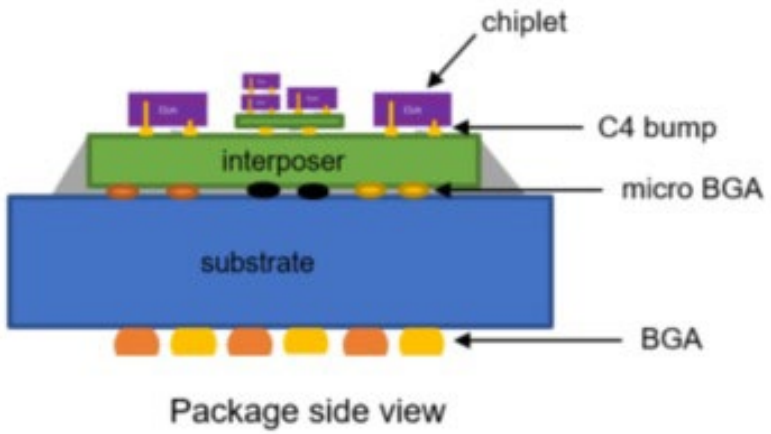
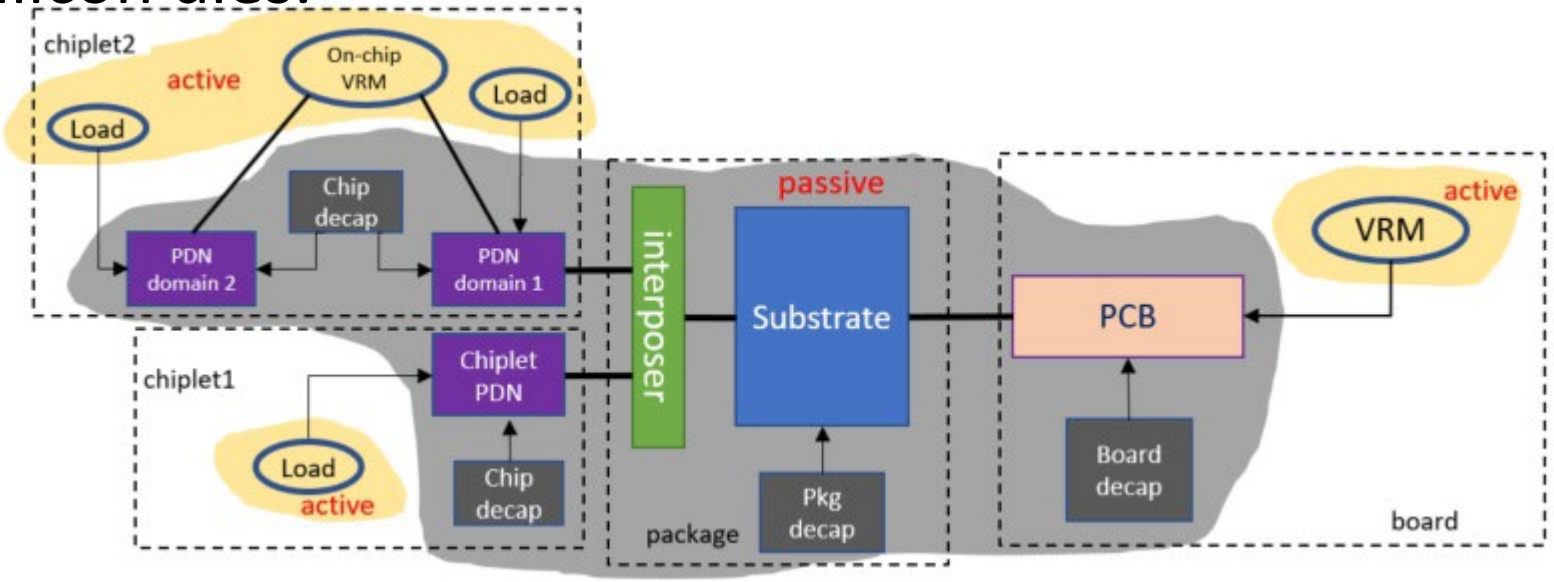
Chiplets must be positioned in their respective locations and provided with paths through the power distribution network. There can be multiple power domains. Package builder tools are used to automate the placement of vias, ball grid arrays and traces to the PDN. To mitigate supply voltage fluctuations decoupling capacitors (“decaps”) are placed on the PCB, package substrate, package interposer, and the silicon dies.



Package side view



Computational Bottleneck

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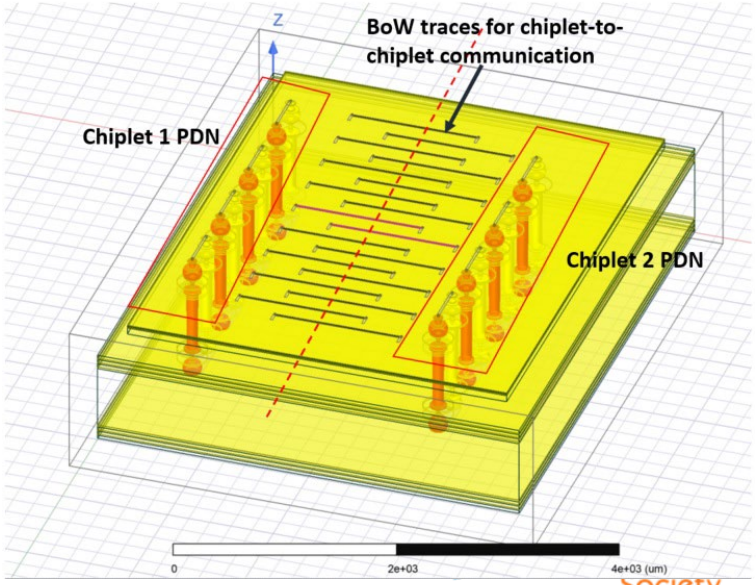
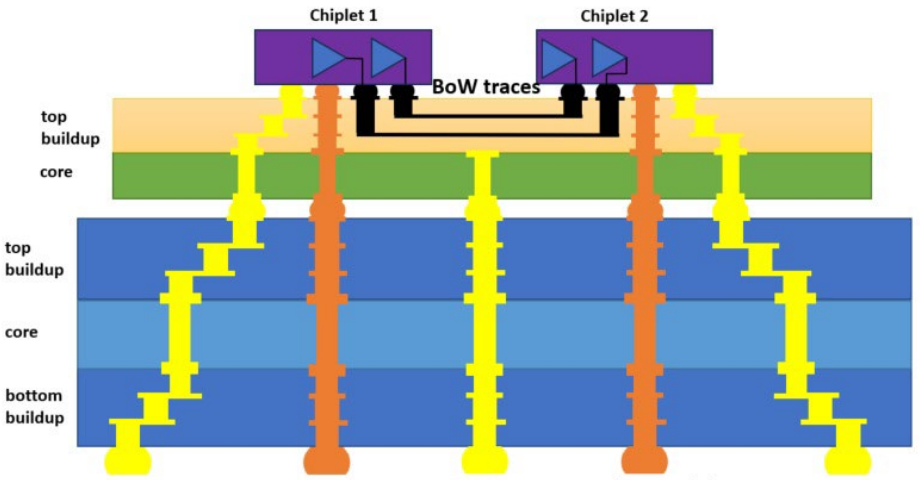
Many problems take too long to simulate and thus make it to difficult to predict the “what if” scenarios. This slows down the design process. This gets exacerbated when handling multiphysics situations (e.g. electrical + thermal) One approach is to first start with simplest possible models that will capture some physics and produce meaningful outputs

Top View



Cross-Section



Chiplet-based design with PDN and D2D network

For 50 X 50 µBGA structure, extraction of network parameters takes more than a week!

Computational Bottleneck -- Research Needs

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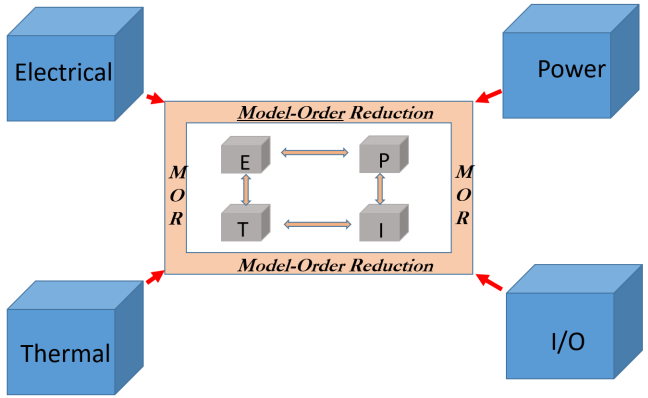
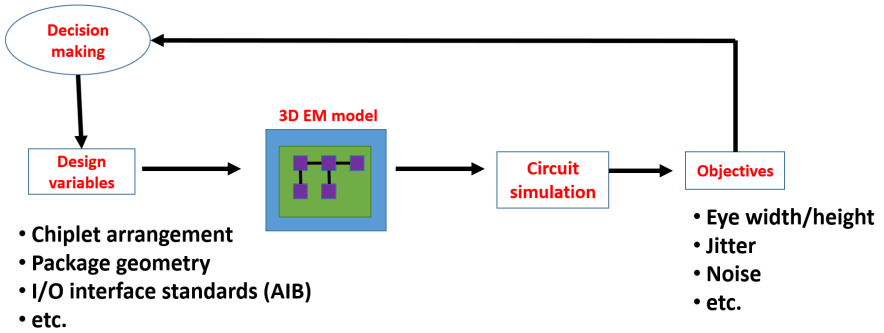
- **Methodical abstractization**
  - Compact models
  - Reduced-order models
  - Behavioral models
- **Faster verification platforms (>10X)**
  - Multi-physics solvers (EM , thermal management, materials)
  - Transistor-level circuit simulation
- **AI/ML assisted solutions**
  - Optimization, mitigation of uncertainty





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Conclusion

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- Brain-inspired computing will be major driver for HI
- Chiplet Disagreggation + PDN - Higher level of complexity
- Can only be resolved by Co-design
- Real Co-Design is far more complex
- Abstractize multi-physics models
- Make use of AI and ML techniques