HETEROGENEOUS INTEGRATION ROADMAP

Photonics TWG update

Chair Bill Bottoms MTS

Co-Chair Amr S Helmy University of Toronto

2024

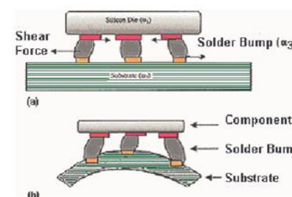
Select Outcomes - Photonics TWG Chapter

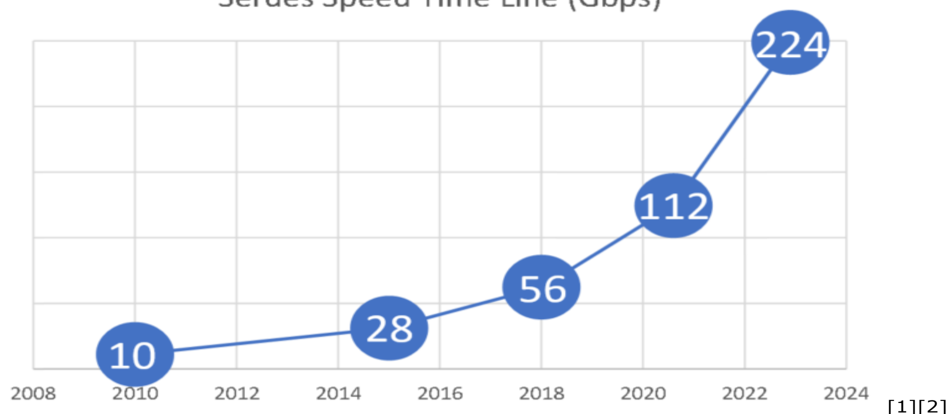
- Bandwidth density in interconnects
- Fiber Attach
- New TWG Members

Speed and Distance

HIR HETEROGENEOUS INTEGRATION ROADMAP

- Feature and BW driven package dimension increase
  - 1Logic + 2HBM -> exceeds 1 reticle with 400mm^2 logic die
  - Signal Fanout – pin larger package
  - Power density – layers for power distribution
  - Die partition / HBM – Heterogeneous integration
- Assemble reliability challenges with larger pkg
  - Warpage, COP/Coplanarity, Si crack, UF crack
- PDN competition from adjacent high-density logi
- Thermal preheat





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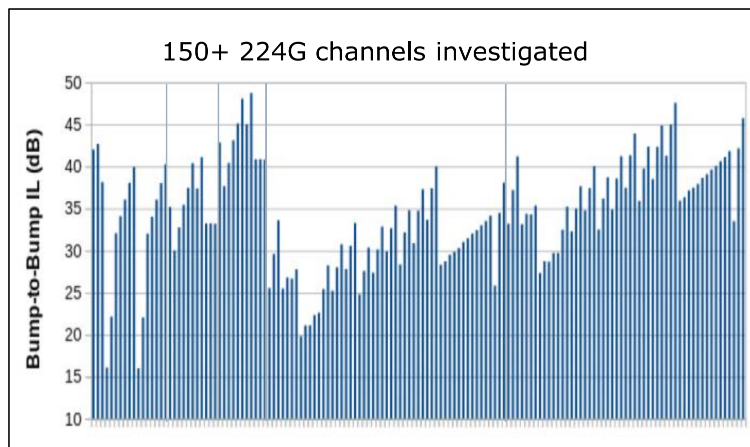
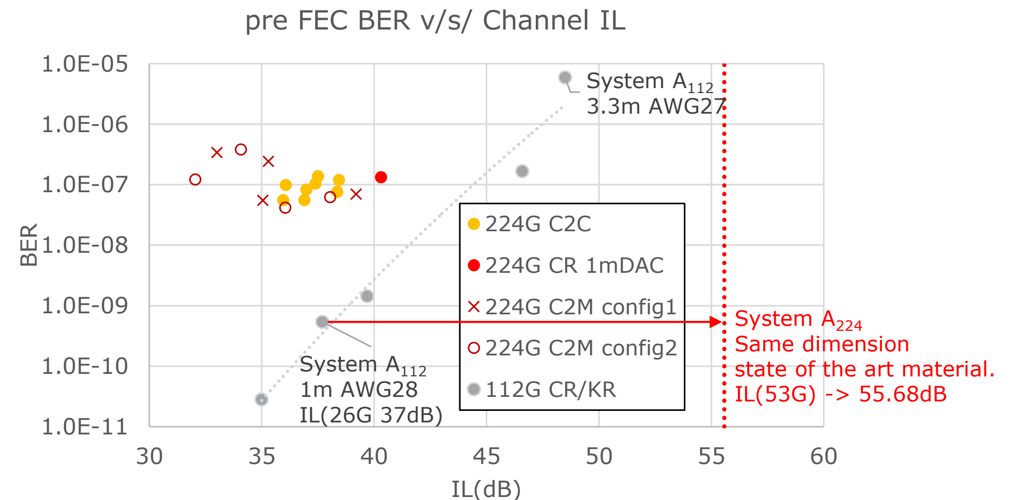
Speed and Distance

- 112G Serdes provides robust support for High loss passive Cu links
- Will it still work in legacy system architecture?





ISSCC 2024 Forum 6.1 Highlights and Challenges in deploying 100 G+ SERDES

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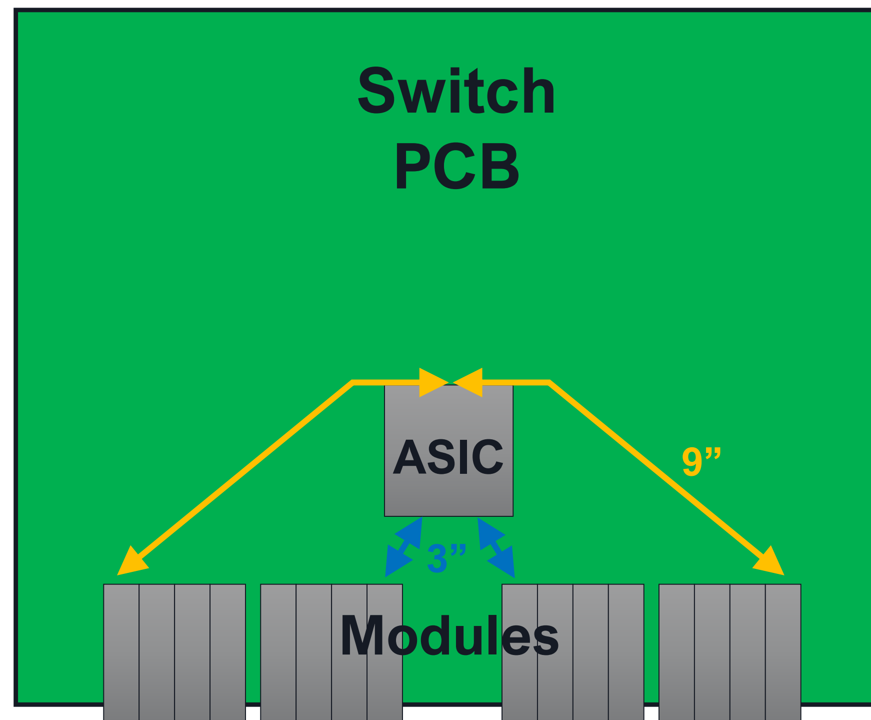
HIR Heterogeneous Integration Roadmap

Speed and Distance

HETEROGENEOUS INTEGRATION ROADMAP

- Difficult routing for some channels
- Significant additional loss introduced by large packages
- ➢ Total chip-to-module channel loss may exceed 35dB at 200G
- Potential measures:
  - Extensive equalization
  - Repeaters
  - Flyover cables



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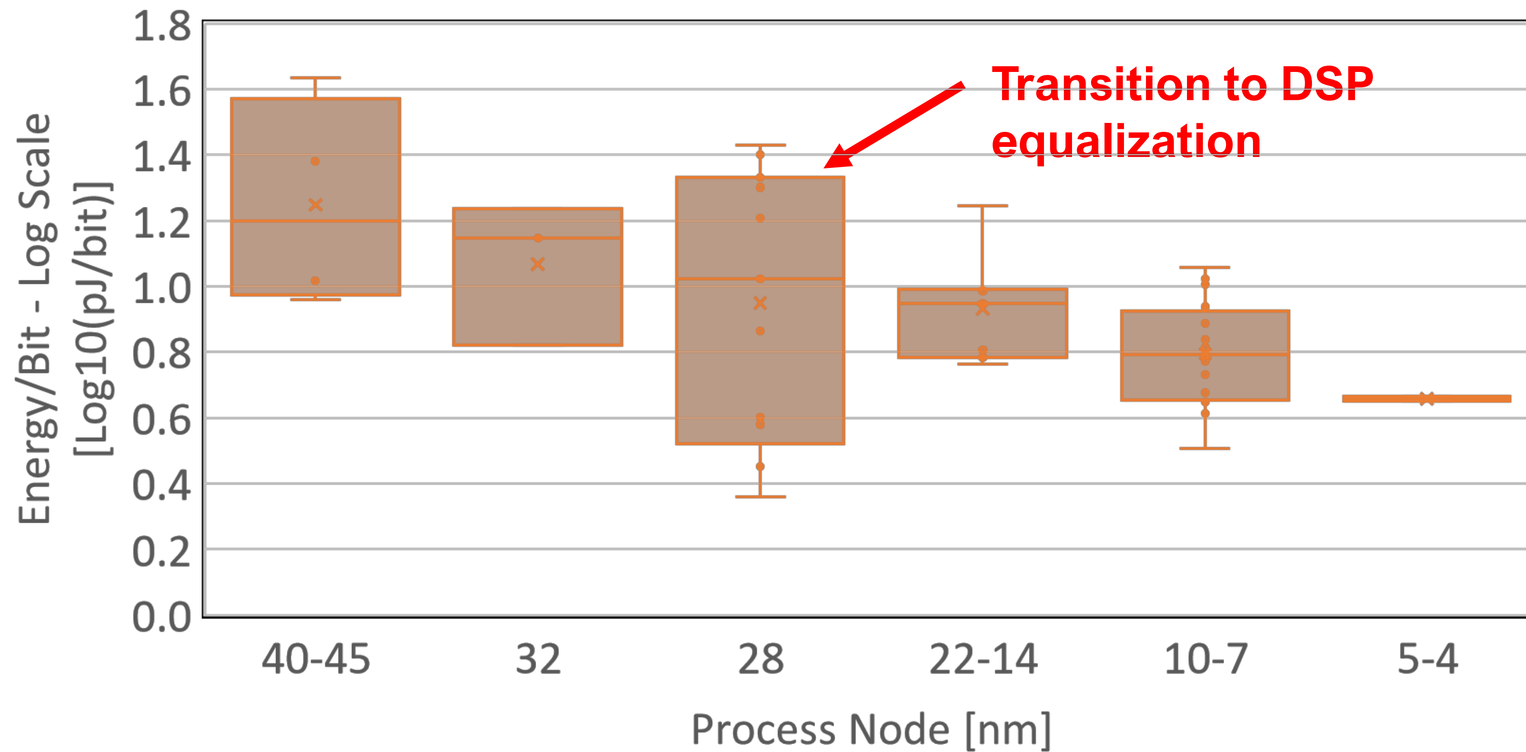
Speed and Distance

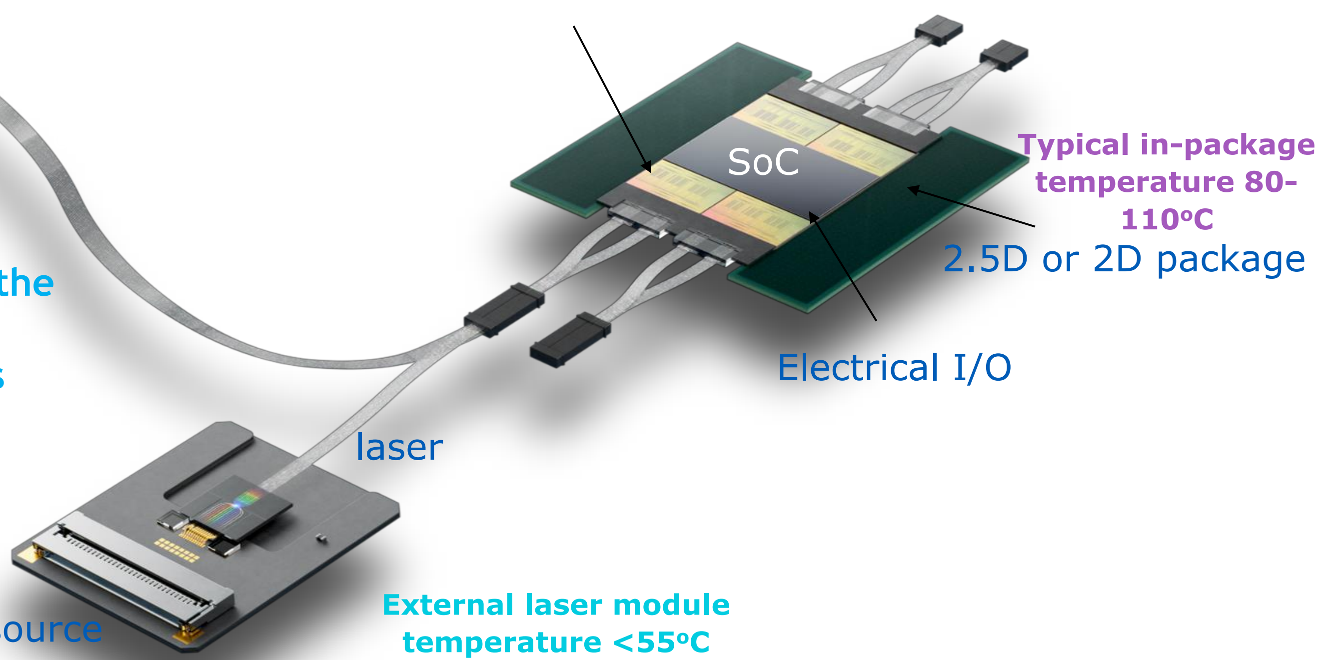
HETEROGENEOUS INTEGRATION ROADMAP



Fiber Connect

Socket – Socket
Board – Board
Rack - Rack

A new universal I/O - communicate anywhere at the cost and performance of in-package interconnects



SuperNova™ multi-port, multi-wavelength laser source

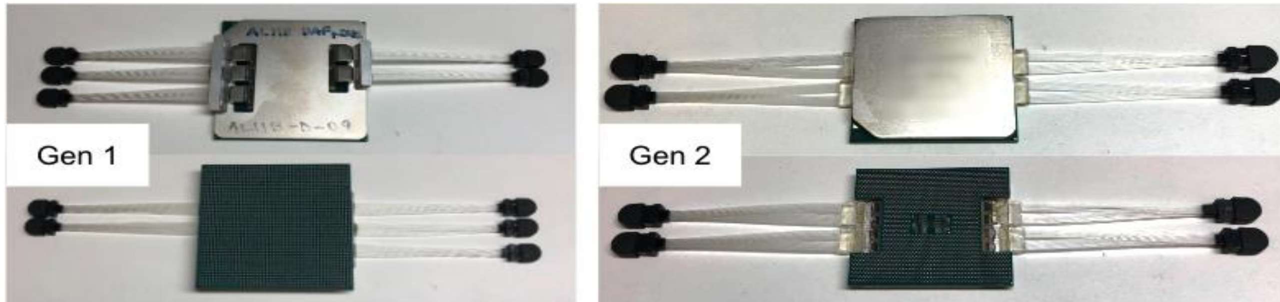
HIR HETEROGENEOUS INTEGRATION ROADMAP

Vladimir Stojanović Ayar Labs + Intel

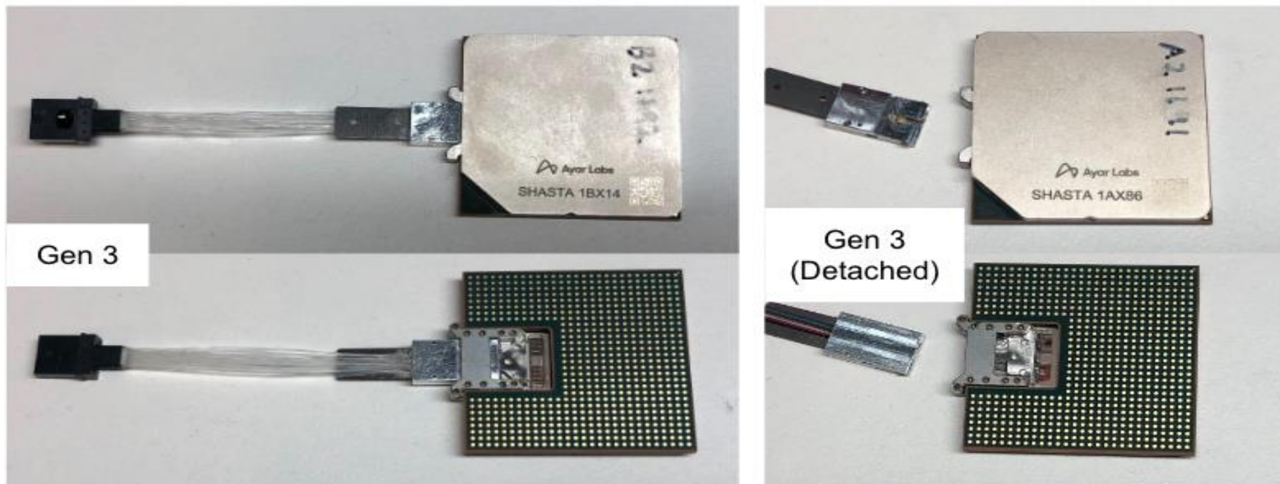
Packaging and Fiber Attach

HIR
HETEROGENEOUS INTEGRATION ROADMAP

Gen 1:
Actively aligned vertical attach of fiber pigtails



Gen 3:
Detachable edge attach optical connector



(Source: Wade *et al* HotChips 2023)

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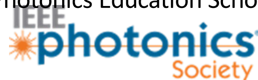
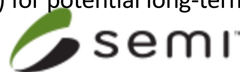
Farnood Rezaie, Ph.D.

HETEROGENEOUS INTEGRATION ROADMAP

- 8+ years of experience in high-volume manufacturing and development of optical transceivers for applications in A.I. and D.C.
- 15+ years of experience in opto-electronics in industrial and academic institutions
- Cisco Systems (2022-now)
  - Technical leader in hardware engineering
  - Ownership of Cisco's SiPh common platfrom, supporting all types of transceiver products from IMDD to coherent
  - Chair of IEEE-EPS Photonics TC, member of Test TC and co-lead of JEDEC's SiPh qualification task group within JC14.3
- TowerJazz/Tower Semiconductor (2017-2022)
  - Developed, qualified and scaled up PH18* and PN18* (both leading SiPh PIC platforms in the world) from conception to high-volume production (+100M business by 2022)
  - Developed one of industry's 1st SiPh PDKs (PH18MA) in close collaboration with Lumerical, Synopsys and Cadence
  - Multiple granted patents, publications and contributions in area of SiPh process, PDK, testing and reliability
  - Winner of Tower Semi's CEO award of excellence (2021)
- Skorpios Technologies Inc. (2016-2017)
  - Developed 100G transceivers based on heterogenous integration of III-V into SiPh platfrom
- Education
  - PhD from University of Central Florida (2015)
  - MSc from University of Central Florida (2011)
  - BSc from University of Tehran (2009)
  - Northrop Grumman Fellowship (2015) awarded to outstanding individuals in optical physics
  - SPIE Optics & Photonics Education Scholarship (2014) for potential long-term contributions to optics and photonics





Bassem Tossoun bio

- Bassem Tossoun is a Senior Research Scientist in the Large Scale Integrated Photonics (LSIP) Lab at Hewlett Packard Labs
- He graduated with a Ph.D. degree from the University of Virginia in 2019, advised by Prof. Andreas Beling and co-advised by Prof. Joe Campbell
- His research interests lie in integrated photonics, optoelectronic devices, heterogeneous integration of III-V on silicon photonics, and emerging memory technologies for next-generation computing accelerators in high-performance computing systems and for artificial intelligence (AI) on the edge
- He is currently the principal investigator at Hewlett Packard Labs on a project funded by DARPA to develop a scalable and energy-efficient neuromorphic computing accelerator on a heterogeneous III-V on silicon photonic platform
- He is a Los Angeles-native currently living in Santa Barbara, CA
- Enjoys hiking, camping, playing his guitar, playing and watching sports

Thank You

- Please get involved
- Emails us or leave comments
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