Future of AI Hardware Enabled by Advanced Packaging

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Sam Naffziger, SVP and Corporate Fellow, AMD
RELENTLESS DEMAND
AI Driving Hyper-Exponential Demand for High-Performance Compute

Parameters (Log Scale)

Image and speech recognition models
- ResNet50: 26 million
- BERT-large: 330 million
- AmoebaNetB: 557 million

Language + recommender models
- GPT-3: 175 billion
- GPT-4: 1.7 trillion

2x per year
- 2x per year
- 20x per year

2020 2018 2016 2014
Exponential growth in model sizes driving massive increase in energy required for training

Upper bound on training requirements is yet to be determined
Absolute power sets limits on AI

- The quest for greater AI and AGI drives massive compute demand
- Power for training in reasonable time requires massive datacenters
- Power generation and grid limits will set a ceiling on training capability

Datacenter power

<table>
<thead>
<tr>
<th>T Parameters</th>
<th>MW to Train in 30 Days</th>
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<tbody>
<tr>
<td>1000 GPUs</td>
<td>1</td>
</tr>
<tr>
<td>10,000 GPUs</td>
<td>10</td>
</tr>
<tr>
<td>100,000 GPUs</td>
<td>100</td>
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Based on AMD internal calculations of modern GPU power and compute capability plus typical training requirements per parameter
Datacenter-level optimization

- Maximize accelerator compute capability
  - Advanced technology, 3.5D chiplet integration

- System-level optimizations
  - Tight hierarchical network
  - Shorter reach high speed interconnects

- Software co-optimization up/down the stack
  - Maximize locality
  - Exploit new math formats
  - Hardware / Software co-design
  - Advanced technology, 3.5D chiplet integration
Reducing Data Movement Energy

Communication energy grows exponentially with distance. Maximizing locality key to efficiency.
3.5D PACKAGING MOTIVATION

- The key to power-efficient performance is **tight integration**

- 3D Hybrid bonding provides by orders of magnitude the **densest**, most **power-efficient** chiplet interconnect

- Advanced 2.5D enables **more compute** and **HBM** in a package

- Increased **system-level** efficiency
AMD INSTINCT™ MI300 SERIES

Key Innovations

I/O Die (IOD)
256MB AMD Infinity Cache™
Infinity Fabric Network-on-Chip

Accelerator Complex Die (XCD)
6X38 AMD CDNA™3 Compute die

CPU Complex Die (CCD)
3 x 8 “Zen 4” Cores

3.5D Package
3D hybrid bonding
2.5D silicon interposer

AMD Infinity Fabric™
AP Interconnect

8 stacks of HBM3
MI300A: 128 GB (8H)
MI300X: 192 GB (12H)
AMD INSTINCT™ MI300 FAMILY
3.5D Advanced Packaging Elements

Unique Thermal architecture
→ ~750W TDP

Advanced 3D Hybrid Bonding→ Compute density and perf/W

Advanced 2.5D Arch→ Ultra high BW IOD-IOD and HBM3 integration

Large module Attach on Advanced 2D Substrate

Illustration purposes only
Future AI hardware requires investments in all key areas of advanced packaging to build best-in-class devices.
3D HYBRID BONDING EVOLVED

AMD 3D V-CACHE™ TECHNOLOGY
Gen 1 and Gen 2

- Hybrid Bonding size: ~7 x 10 mm
- Logic die as base for voltage delivery
- N7 (X3D) on N5 base (CCD) die
- Up to 2.5TB/s vertical bandwidth

AMD INSTINCT™ MI300 ACCELERATOR
Gen 3

- Hybrid Bonding size: ~13 x 29 mm (0.45x reticle)
- Logic die on top enables improved thermals
- N5 XCD/CCD stacked on N6 base die (IOD)
- Up to 17TB/s vertical bandwidth

Extended hybrid bonding technology envelopes to enable MI300
2.5D ARCHITECTURE EVOLVED

MI100→MI200

• 2.5D Module Size < 2-2.5x Reticle
• <3x Reticle Stitching
• D2D Micro-bump pitch 45-55u
• Monolithic SOC attach

MI300

• 2.5D Module Size ~ 4x Reticle for UMA
• 4x Reticle Stitching
• D2D Micro-bump pitch ~35u
• Hybrid Bonded Stack attach

Significant capability expansion in 2.5D architectures to enable MI300
Future Opportunities
Revolutions in 3D Hybrid Bonding (Process, materials) can enable Groundbreaking Architectures not Possible with Monolithic Designs.
EVEN Tighter INTEGRATION OF COMPUTE AND MEMORY

Higher Levels of Integration Enables Higher Bandwidth at Lower Power

<table>
<thead>
<tr>
<th></th>
<th>On Board Memory</th>
<th>2.5D Micro-bumps (HBM)</th>
<th>3D Hybrid Bond</th>
</tr>
</thead>
<tbody>
<tr>
<td>pj/bit</td>
<td>~12</td>
<td>~3.5</td>
<td>~0.2</td>
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Invest in Scaling New Logic-Memory Architectures

Image source: https://commons.wikimedia.org/wiki/File:SDRAM-Modul.jpg, Creative Commons 4.0.
Co-packaged optics provide a path forward
Energy efficiency at < 1pJ/bit

Single mode, enabling 10m up to 2km reach

Standardization of coupling schemes and manufacturing flows

Fully automated solutions for enabling FAU assembly in high volume

Investments in Key Optics Technologies Critical for Scaling
FUTURE SYSTEM-IN-PACKAGE ARCHITECTURE

Modularity, Compute Density and Heterogeneous Integration
Driving performance gains over the next decade requires relentless focus on chiplet integration for efficiency

- Insatiable demand for more compute
- Energy efficiency is the primary limiter
- We must innovate in new dimensions:
  - System level optimizations
  - Domain specific architectures
  - Tight integration of compute and memory with chiplet architectures, advanced packaging, new interconnects
  - Leveraging AI holistically
- Deep collaboration required across materials, process, circuits, system design, architecture, software, and applications
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