HETEROGENEOUS INTEGRATION ROADMAP

# Heterogeneous Integration: 2D - 3D Interconnects 2023 Chapter


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### 2023 Chapter Contributors

| | | | |
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# Chapter Objectives

- Define and proliferate a standardized nomenclature for package architectures covering and clearly identifying, 2D and 3D and hybrid packaging constructs
  - Comprehend all HI announcements including Wafer-scale constructions.
- Define and disseminate key metrics driving the evolution of the physical interconnects in these architectures
  - The chapter lists their current values and projections for the next generations
- Chapter is organized into 4 primary areas:
  - Converged Nomenclature Framework for 2D , 3D and hybrid Architectures
  - Key Metrics:
    - Design Attributes
    - Electrical Attributes including Signaling and Power Delivery
  - Challenges
  - Discussion

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# 2023 Chapter Key Summary

- Nomenclature from a few years ago holds for the most part but will need an update (Thanks to Prof Fukushima & Venky for highlighting this). Mid-Year refresh proposed
- WB section is weak and needs help from experts like Jan Vardaman, Ivy Qin and Adeel Bajwa
- AI/ML driven increases in compute demand are forcing some non-linearity in our estimates and to respond, the BW roadmap has been expanded
- Lots of publications on standardized D2D links have appeared and references are updated to be fair to all and historically consistent
- Tom Gregorich made an excellent suggestion to define an interconnect landscape. It is a good idea but will need careful thought and argues for a mid-year update
- Table 5 on architecture-process elicited some good feedback. Have requested Dishit Parekh, Vidya Jayaram, Krutikesh Sahoo, Jan Vardaman and Adeel Bajwa to help get this table updated and correct.

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# Interconnects

- **Die-Die Interconnects:** Interconnects between stacked die that enable vertical interconnects between multiple die in a 3-D stack *Covered in this chapter*
- **On-package Die-Die Interconnects** i.e., 2D and Enhanced 2D Interconnects: Interconnects between die within the package that enable lateral connections *Covered in this chapter*
- **Die-to-Package (*or to substrate*) Interconnects:** Interconnects between the die and the package typically known as the first level interconnect (FLI) *Covered in this chapter*
- **Within Package Interconnects:** Interconnects within the package that enable lateral connections *Covered in the Substrate Section of the Single Chip and Multi-Chip Chapter*
- **Package to Board Interconnects:** Interconnects between the package and the next level, which is typically the motherboard, referred to as the second level interconnect (SLI) *Covered in this chapter*
- **Package on Package Interconnects** *Covered in this chapter*

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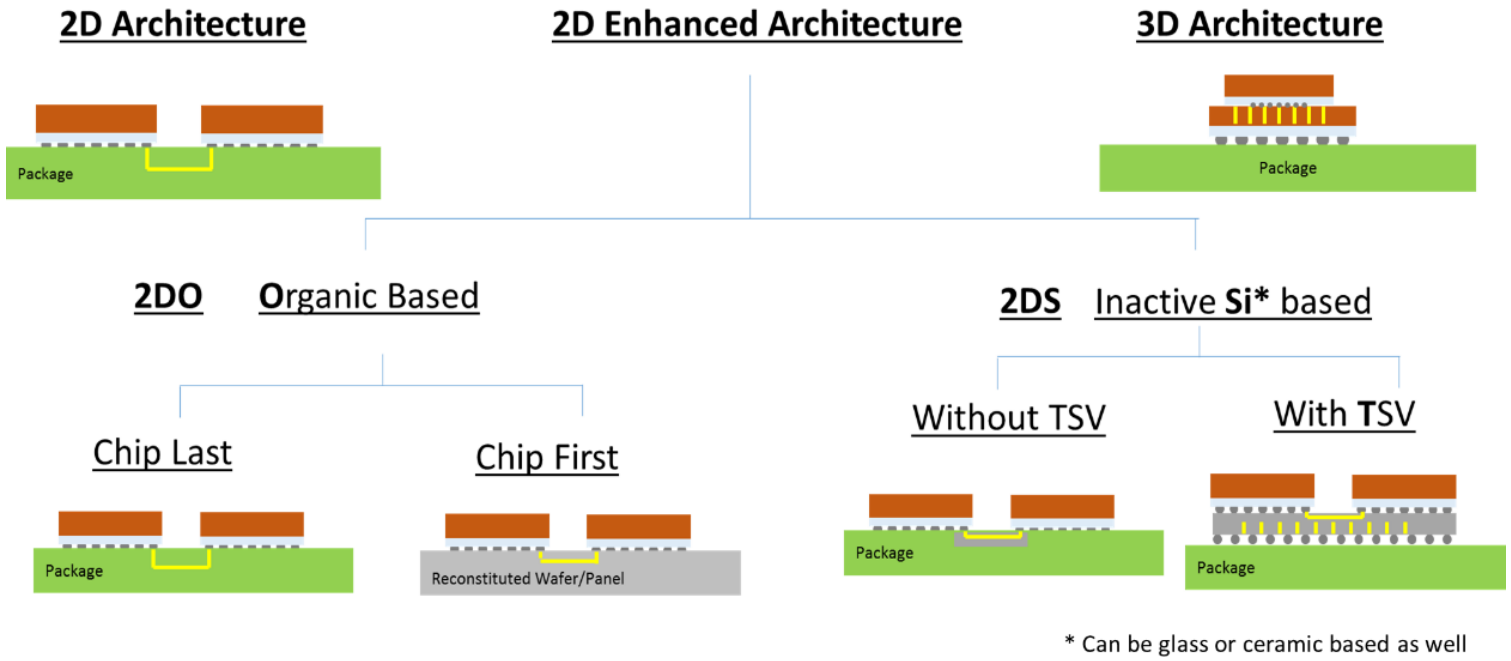
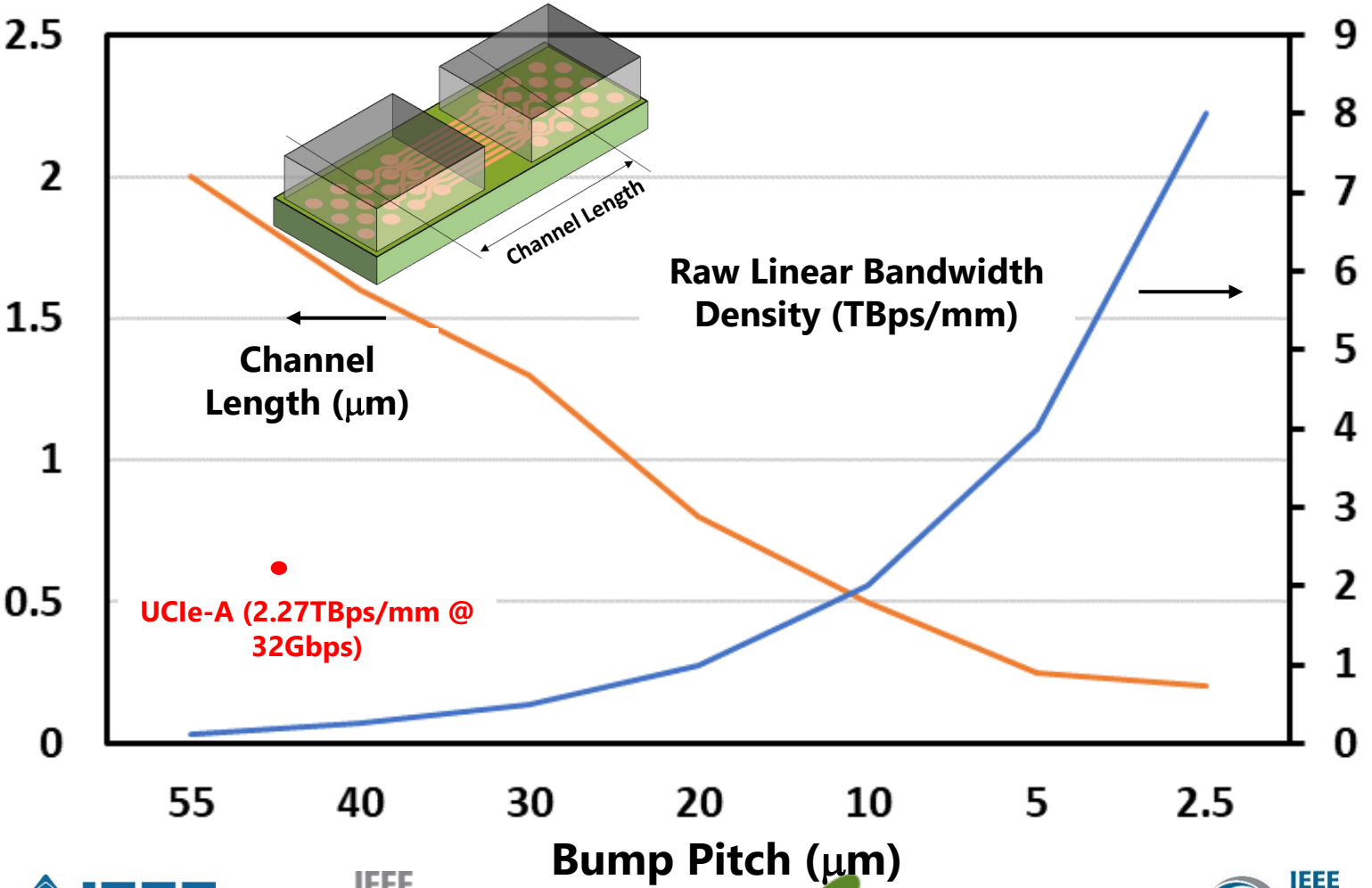
# Nomenclature




- Add Chip-Mid & Improve Picture (Ref: D. C. Hu et al., "2.2D Die last Integrated Substrate for High Performance Applications," 2021 IEEE 71st Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2021, pp. 157-163)
- Clarify 2DO includes organic interposers
- Add a broader interconnect hierarchy picture

# Non-Unique On-Package Planar Interconnect Scaling Roadmap




- @ 32Gbps UCIe-A theoretical BW@ 45μm pitch is 2.2716 TBps & this roadmap states @ 3Gbps & @ 40μm pitch a theoretical BW of 0.25TBps is possible. There is no discrepancy in the numbers and modulating speed (hence power efficiency) is a knob for scaling BW → lots of room to grow
- Extended to 7 generations

# On-Package 3D Interconnect Scaling Roadmap

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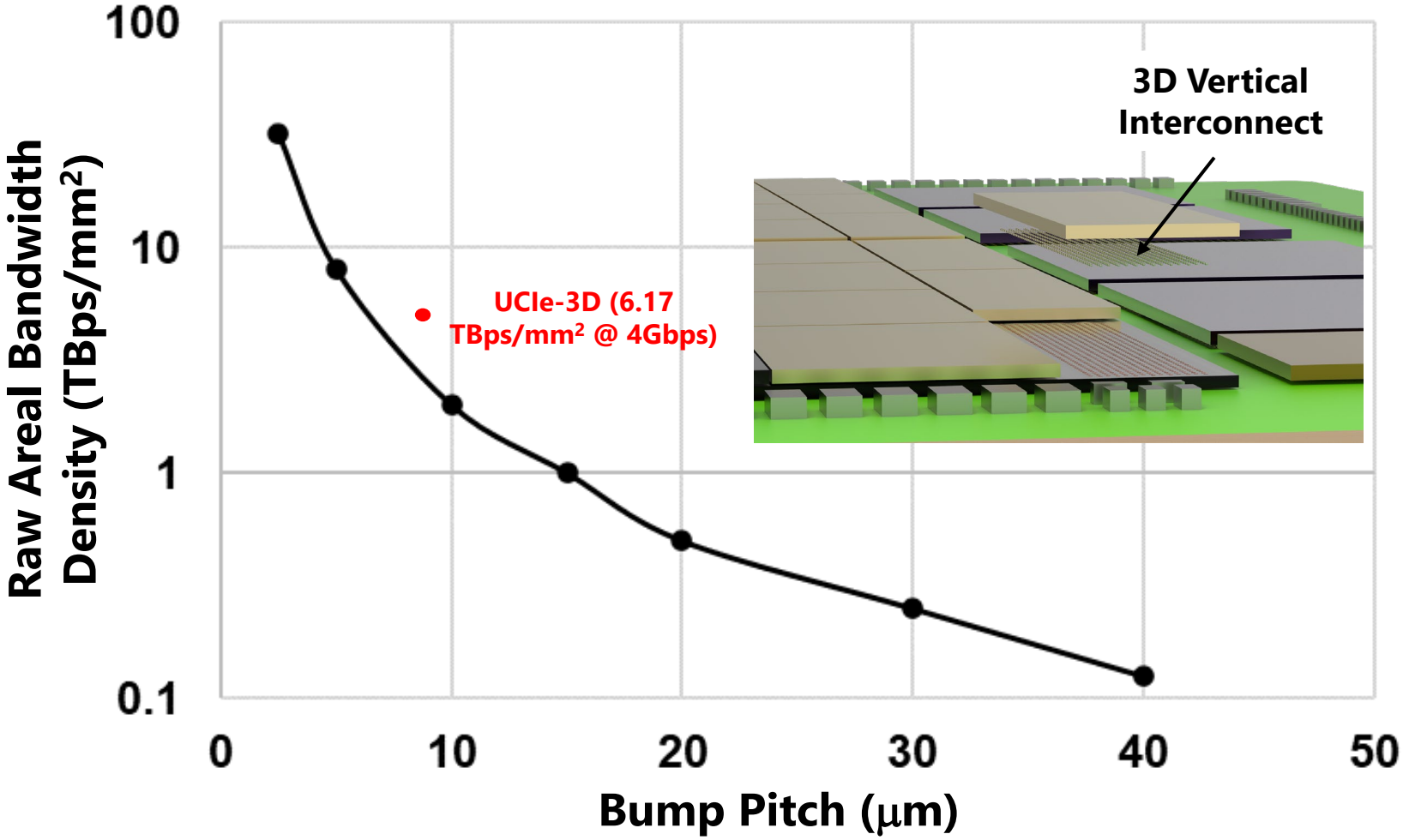


- Extended to 8 generations
- Signaling speed ≤ 1.8Gbps (speed is a knob → room to grow

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# Signal Integrity Attributes

| Generation Number → | | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| Linear Bandwidth Density (GBps/mm) | | 125 | 250 | 500 | 1000 | 2000 | 4000 | 8000 |
| Channel Performance | Channel Length (mm) | <2.0 | <1.7 | <1.4 | <0.8 | <0.50 | <0.25 | <0.15 |
| | Bump-to-Bump Channel RC (ps) | <10 | <10 | <10 | <10 | <10 | <10 | <10 |

Channel Signaling Characteristics for 2D and Enhanced-2D Architectures (RC Dominated)

| Generation Number → | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| Areal Bandwidth Density (GBps/mm$^2$) | 125 | 250 | 500 | 1000 | 2000 | 8000 | 32000 | 200000 |
| Bump Capacitance (fF) | <30 | <22 | <15 | <10 | <7 | <5 | <3 | <1 |

Channel Signaling Characteristics for 3D Architectures (Capacitance Dominated)

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# Power Delivery Attributes: Area Interconnects for 2D and 3D Architectures

| Year | 2024 | 2026 | 2028 | 2030 | 2032 |
|---|---|---|---|---|---|
| Maximum Core Power Density ($W/mm^2$) | 5 | 7 | 10 | 14 | 20 |
| Sustained Core Power Density (W/mm2) | 1 | 1.4 | 2 | 2.8 | 4 |
| On-die MIM Capacitance Density ($nF/mm^2$) | 140 | 210 | 320 | 520 | 800 |
| VR Power Density ($W/mm^2$) | 1 | 1.4 | 2 | 2.8 | 4 |
| Ceramic Cap Density ($\mu F/mm^2$) | 10 | 14 | 20 | 28 | 40 |
| Sustained Bump Current Carrying Capability ($A/mm^2$) | 1.4 | 2.1 | 3.2 | 5.2 | 8 |

Power delivery Attributes for 2D, Enhanced-2D and 3D Architectures. It should be noted that power delivery attributes are agnostic to the architecture

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# Cross-TWG Collaboration Opportunities

- Substrates and Power Delivery are key areas of Interaction
- This chapter (with appropriate calibration) should be the basis of driving on-package signaling definition

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# Back-up

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# Metrology Focus Areas*

- Characterization Metrologies for Model development and Validation
  - Warpage as a function of temperature
  - Properties (Mechanical, Thermal, Electrical, Interface)

- In-Situ (Fast & Accurate) Process Metrologies
  - Defects (Voids, Cracks, Delamination, Residue)
  - Dimensional metrologies

- Reliability
  - Defects (Voids, Cracks, Delamination, Residue)
  - FA/FI Techniques/Enablers

* Partial List. See refs (e.g., SRC Needs (https://www.src.org/program/grc/research-needs/) for a more detailed discussion