Future Architecture Demands for More Aggressive Packaging

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Moore's "Page 3" refocused upon by DARPA's ERI programs:

"The total cost of making a particular system function must be minimized. To do so, we could amortize the engineering over several identical items, or evolve flexible techniques for the engineering of large functions so that no disproportionate expense need be borne by a particular array.

[..]

It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically."

– Gordon Moore, Electronics, No. 38, Vol. 8, April 19, 1965

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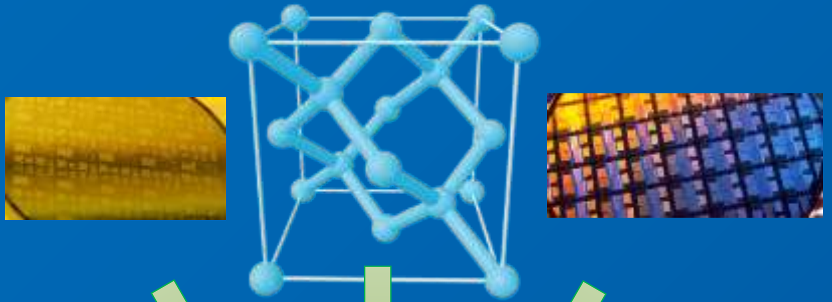

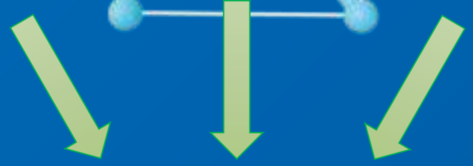

HETEROGENEOUS INTEGRATION ROADMAP

"... there is no spoon."

(There is no box... package... limit...)

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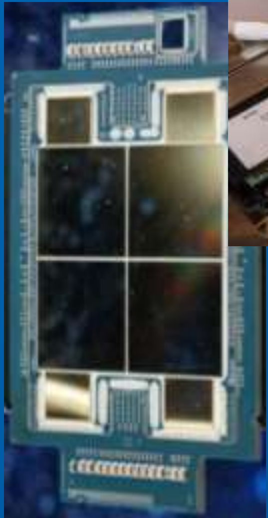
Image from "The Matrix" from Warner Bros.

It's about *systems*, not just ingredients



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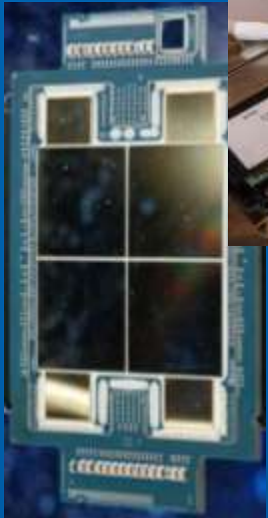
It's about *systems*, not just ingredients



Total Cost of Ownership →
System Technology Co-Optimization

AI, HPC, Mobile, Medical, AR/VR, Contact Lens, . . .

By 2030 scaling up to 50 TB/s DRAM BW,
20 TB/s IO BW, and 100 AI PFLOPS as a single module!

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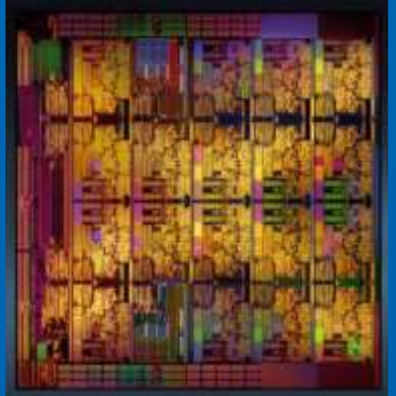
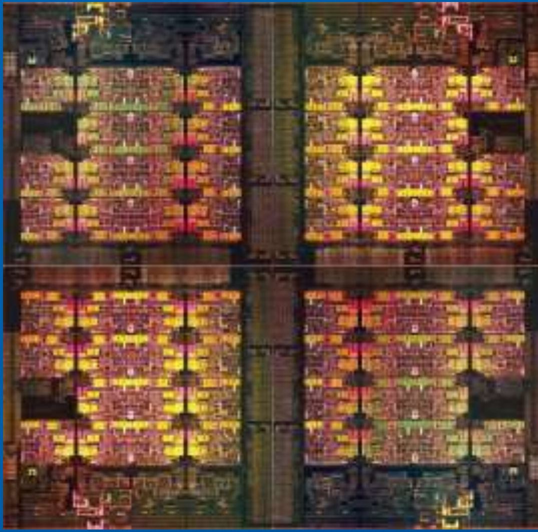
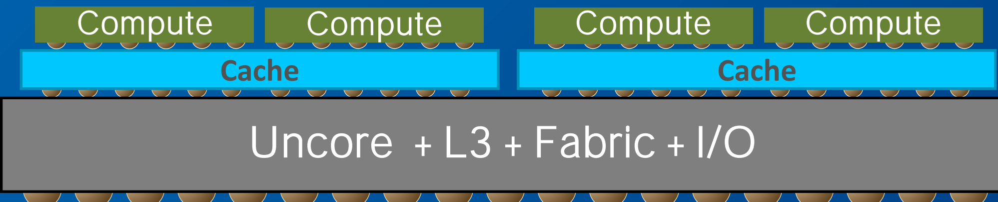
Are we really going all-in?

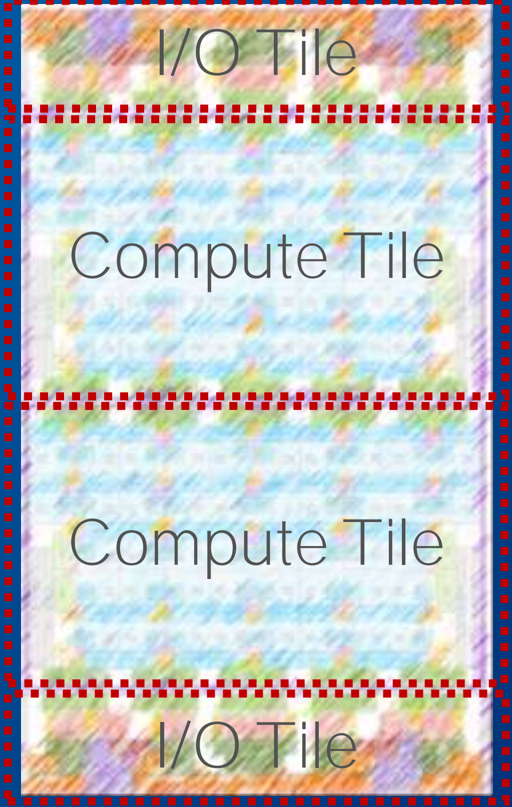


Monolithic

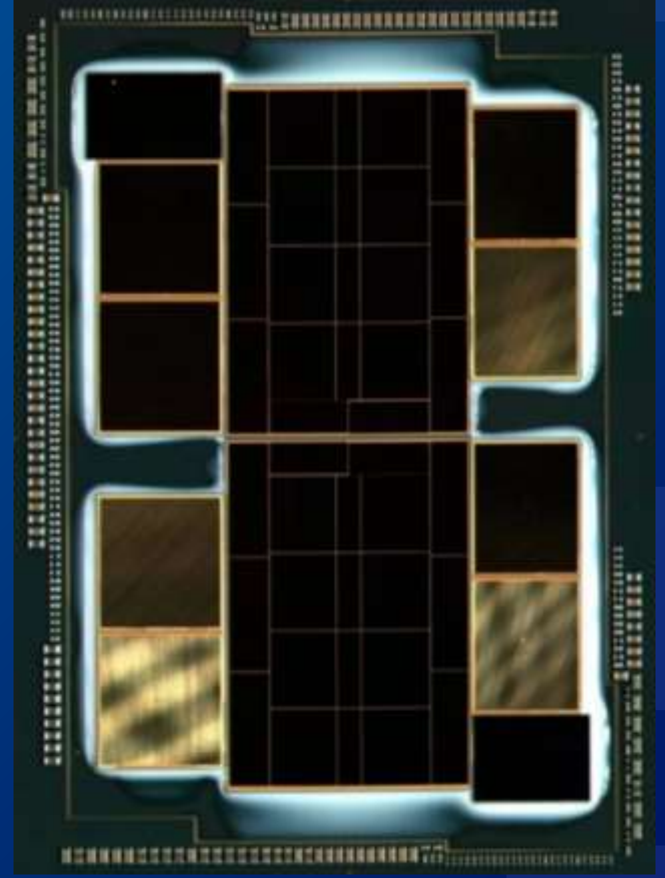


Polylithic
multi-chip





Polylithic tiled



Heterogenous
polylithic tiled

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Are we really going all-in?

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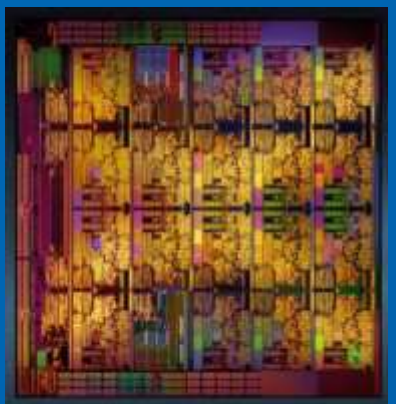
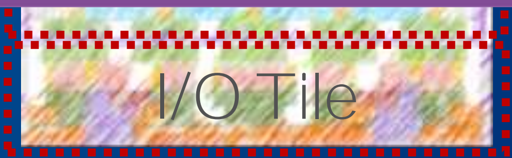
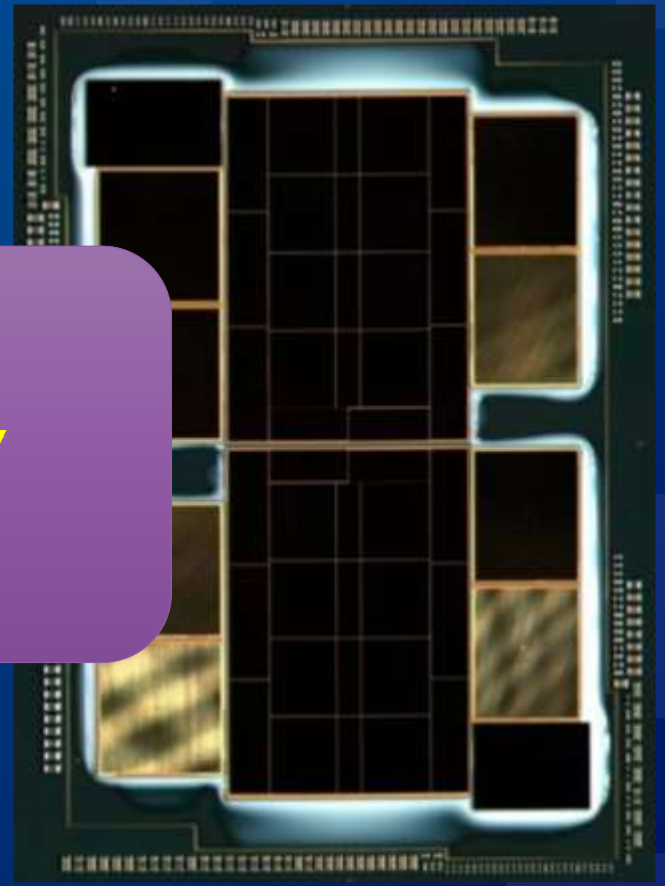


Monolithic

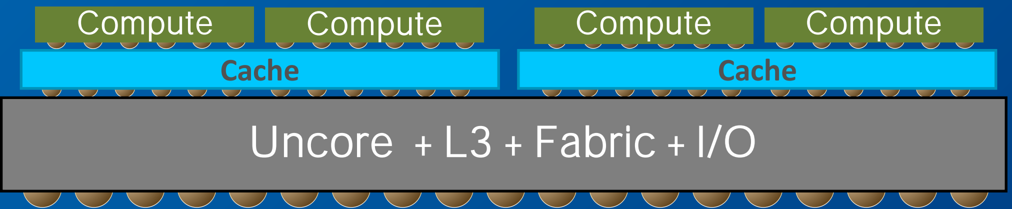
Multi-chip



Polylithic tiled



Heterogenous polylithic tiled



Whether it's 2.5D or 3D in name . . .

it's all the same old "planar thinking"

Is that bad?

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What about big-opportunity thinking?

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"We need to think about packaging 60,000 mm^2 for processing all those LLMs . . ."

– UCLA Prof. Subramanian Iyer, Director of NAPMP

Assume the equivalent of ~80 SotA GPUs at ~800 mm^2 each

sq mm	X,Y dims	pJ/b wires	pJ/b stops	pJ/b d2d	W intern	W extern	Notes
64,000	253	1,265	316	5	46	-	3 GHz, 12 TB/s mesh, 10% activity, no external switches, only counting fabrics
800	28	141	35	1	5	36	

If that 80-GPU part prices at $2M, is that okay?

# units	W fabrics total	OpEx $M annually	OpEx 5 yr life $M
1	46	0.16	0.82
80	3,287	11.83	59.17

Image credit https://samueli.ucla.edu/chips-for-america-taps-ucla-engineering-professor-to-lead-rd-program/

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What about big-opp... ...king?

"W... ...for
pr...

~800 mm^2 each

sq m...		...es
64,000		...GHz, 12 TB/s ... % activity, no
800		...ernal switches, only counting fabrics

...M, is that okay?

# uni...	...abrics	OpEx $M annually	OpEx 5 yr life $M
	46	0.16	0.82
8...	3,287	11.83	59.17

Grossly simplistic model . . .
but $58M is a critical
opportunity for optimization!

Or is it?

(Coherency, Substrates,
Memory, . . .)

Image credit https://samueli.ucla.edu/chips-for-america-taps-ucla-engineering-professor-to-lead-rd-program/
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Real 3D

layers	sq mm	X,Y dims	pJ/b walk	pJ/b stops	pJ/b d2d	W intern	W extern
1	64,000	253	1,265	316	5	46	-
1	800	28	141	35	0	5	36
10	64,000	80	400	100	1	14	-
100	64,000	25	126	32	2	5	-
800	64,000	9	45	11	3	2	-

# units	W fabrics	$M annually	5 yr life $M
1	46	0.16	0.82
80	3,287	11.83	59.17
1	14	0.05	0.26
1	5	0.02	0.08
1	2	0.01	0.03

Each layer thinned to ~10um

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Real 3D

Now a $60M opportunity **that doesn't risk fundamental** economic hurdles . . . only technical hurdles.

How far can we go?

(Still grossly simplistic)

ms		stops	pJ/b d2d	W intern	W extern
					-
				5	36
			1	14	-
			2	5	-
			3	2	-

	ics		5 yr life $M
	46	0.16	0.82
80	87	11.83	59.17
1	14	0.05	0.26
1	5	0.02	0.08
1	2	0.01	0.03

Each layer thinned to ~10um

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Package sprawl vs. package scrapers

- Assume ~8mm x ~8mm die size
  - 800 layers makes it ~8mm tall
- HBI-TSV density drives bandwidth by pitch
  - 9um → 12k/mm^2 → 800K total
  - 3um → 111k/mm^2 → 7.2M total
- Assume ~67% for power/gnd,~33% for IO
  - ~0.27-2.4M IO signals per 1 GHz
  - ~0.260 – 2.4 Pbps total bidir BW per GHz
- 16 TB/s/dir – 150 TB/s/dir IO capable per GHz
  - Lots of floorplanning, thermal concerns
  - Future delivery of **≤1 um** HBI-TSV resolves wiring challenges
  - Bottom die PHY area limits IO sustainable
- Some open hurdles
  - Time on tools
  - EDA, DFX, DFT, FA, etc.
  - Lack of lateral connectivity between high-rises

Each layer thinned to ~10um

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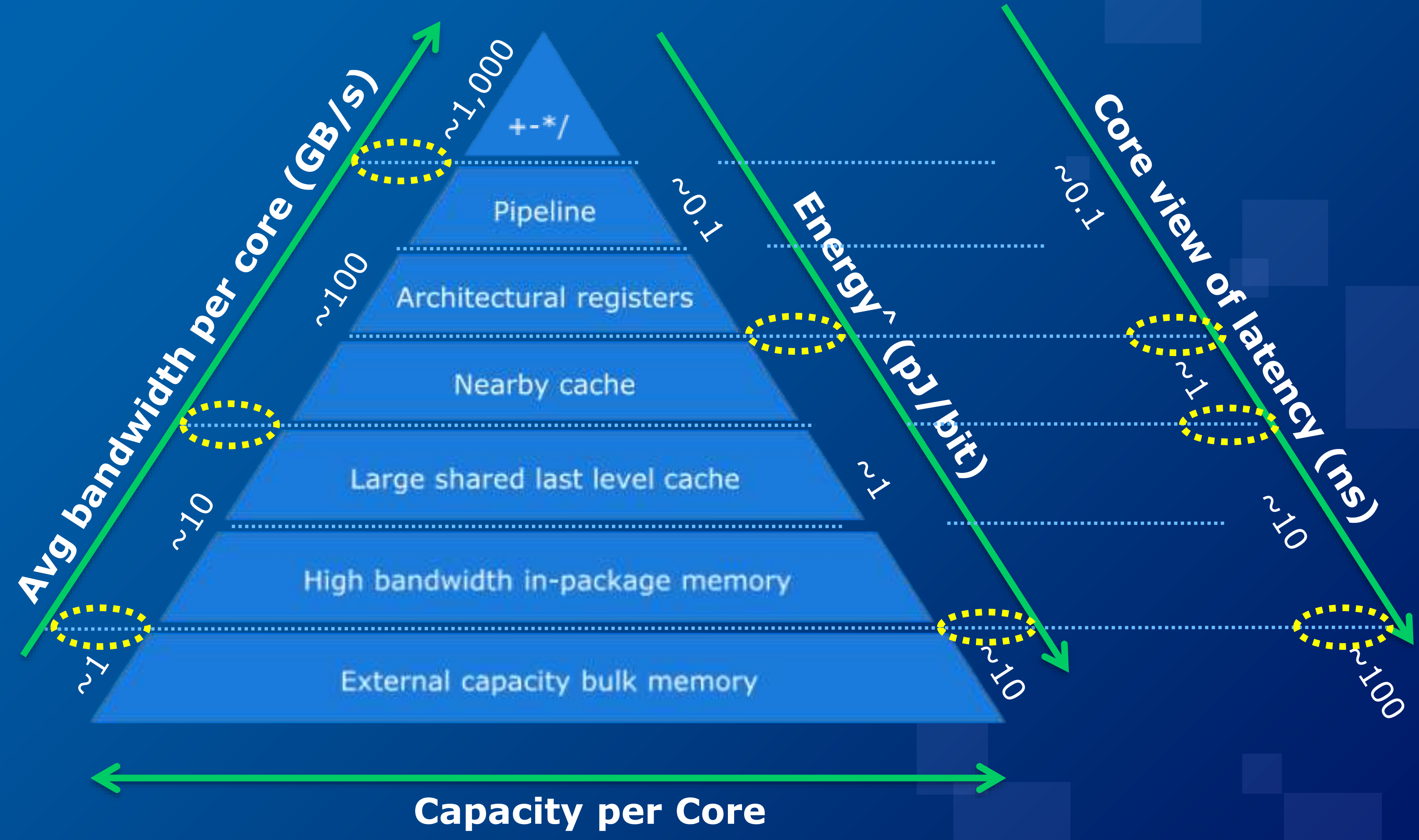
But are we exploiting the right things?

Tapering divisions in bandwidth, energy, and latency are opportunities to optimize



^Not counting overheads for access

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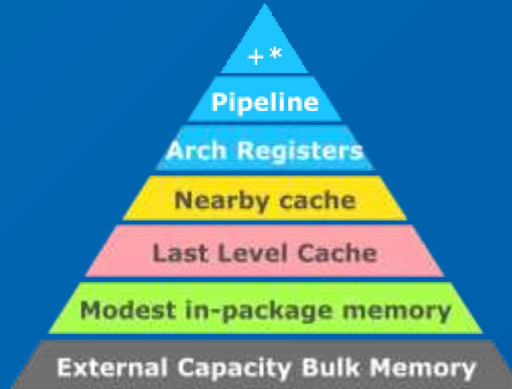
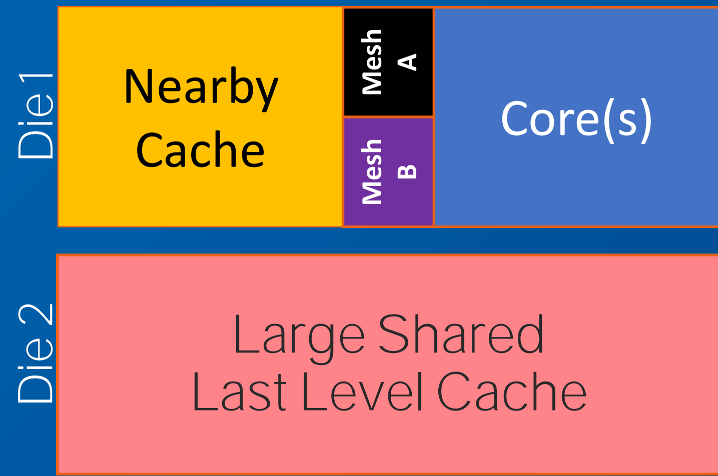
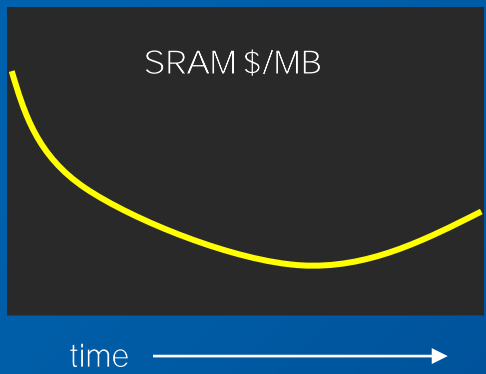
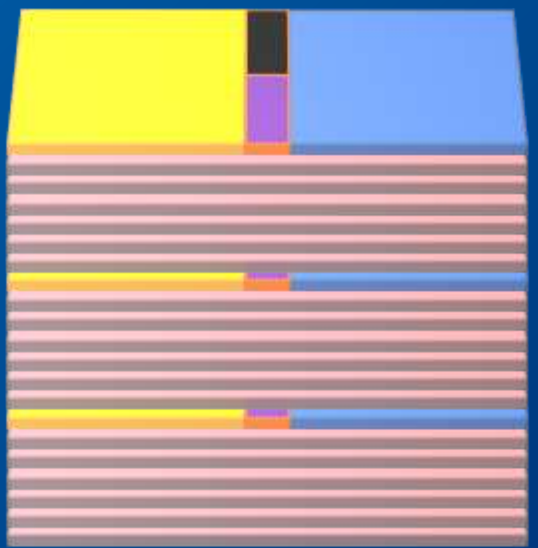
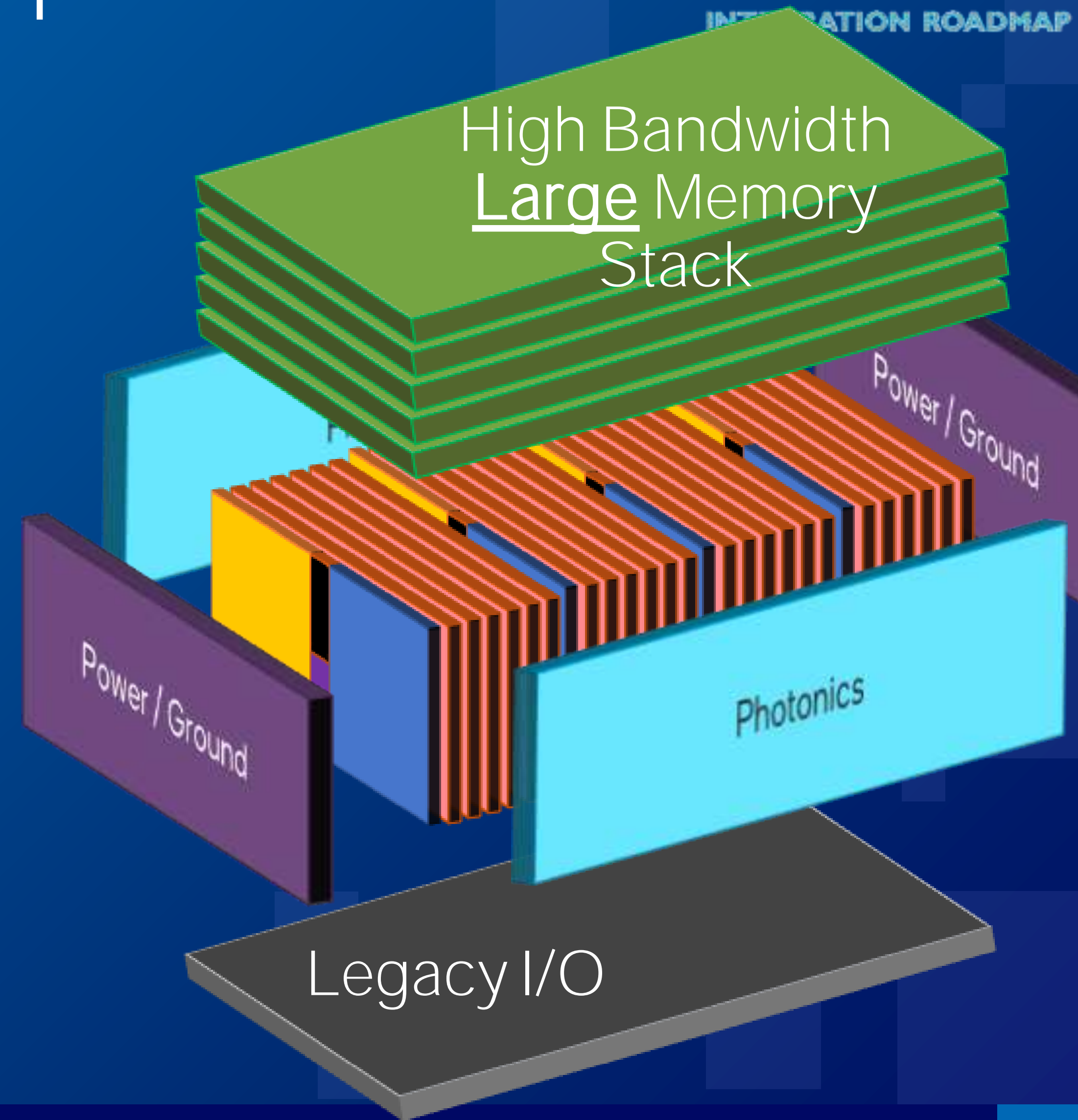
3D as a spatial concept, not planar











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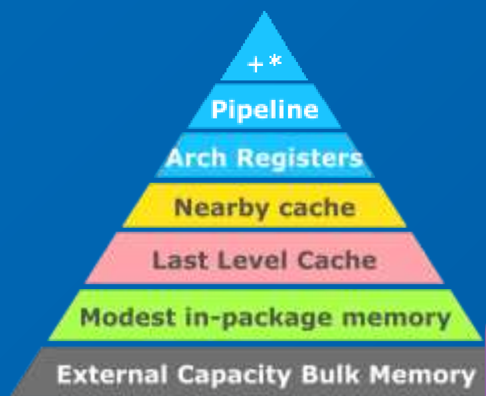
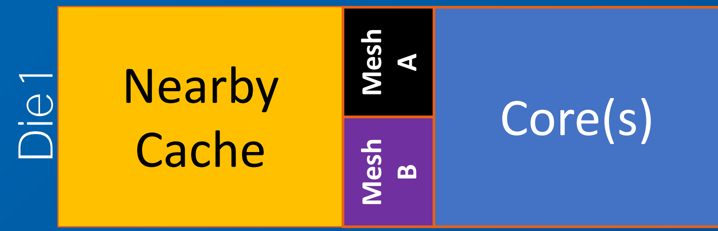
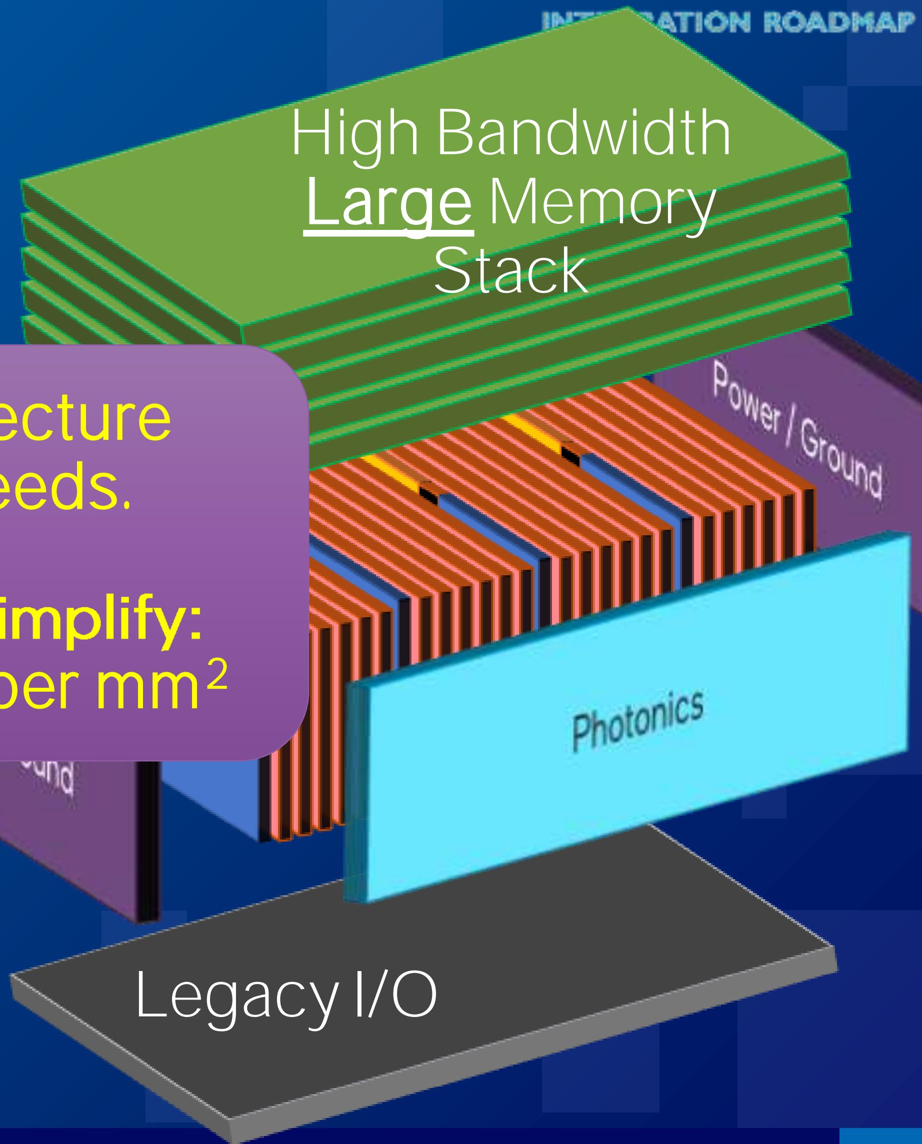
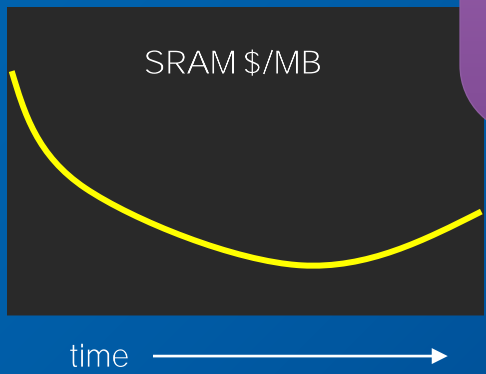
3D as a spatial concept, not planar









Match trade-offs to natural architecture inflection points – speeds and feeds.

Use all 6 faces of "cubic 3D" and simplify:
O(1k) hybrid bonding connections per mm^2

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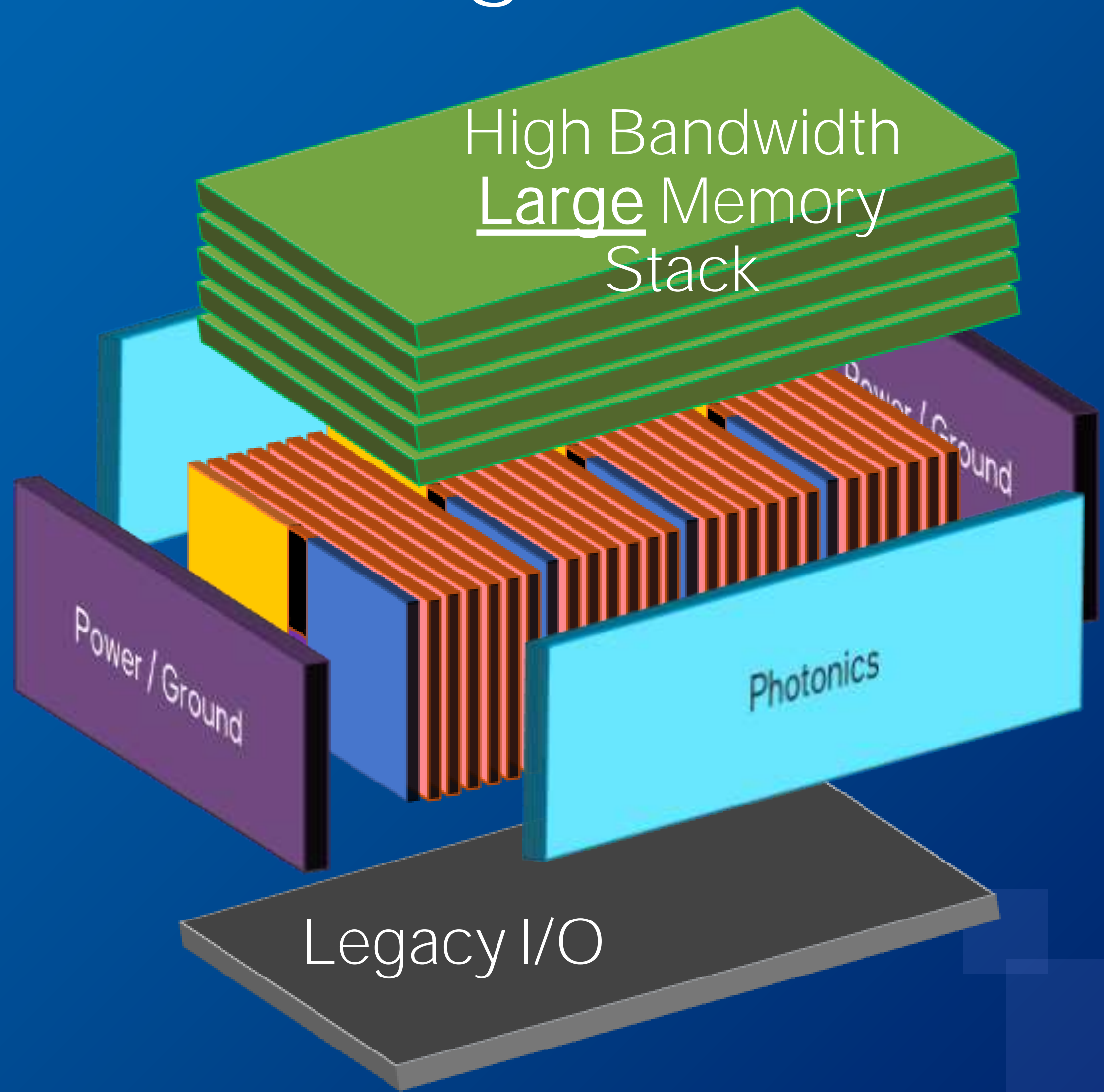
Challenges to achieving dense 3D

Manufacturing:

- edge polish
- right-angle attach
- via density
- bonding speed
- rework support
- redundancy
- tooling Z-height
- wafer thinning

Power and Thermals:

- thermal density
- power delivery
- cooling layers
- heterogeneous material



EDA:

- rotated die
- taper point isolation
- non-planar libraries
- formal verification
- DF<all> 1,000 layers
- scan chain time
- tests and coverage

Design:

- graceful degradation
- extreme interop
- built-in redundancy
- pluggable modules
- abstractions for all

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Challenges to achieving dense 3D

Manufacturing:

- edge polish
- right-angle attach
- via density
- bonding speed
- rework support
- redundancy
- tooling Z-height
- wafer thinning

Power and Thermals:

- thermal density
- power delivery
- cooling layers
- heterogeneous material

High Bandwidth
Large Memory
Stack

Power / Ground

Photonics

Legacy I/O

Modularity in design, reworkable components, interop standards, and time to develop these tools and flows are critical to enabling this 3D "solution in a cube" future

EDA:

- rotated die
- taper point isolation
- non-planar libraries
- formal verification
- DF<all> 1,000 layers
- scan chain time
- tests and coverage

Design:

- graceful degradation
- extreme interop
- built-in redundancy
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- abstractions for all

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About roadmaps . . . hope is **not** a strategy

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OPEN Compute Project®

- AI will save us! Pixie dust on all!
  - AI will reduce design time
  - It will not innovate – yet
- Some packaging directions to 2035
  - Every 2 yr scaling factor targets
    - 10 yrs to "catch up" and then reassess
  - BW/mm (2x), /mm^2 (4x), /mm^3 (8x)
  - IO escape BW/mm (4x), /mm^2 (8x)
  - X, Y dimension (1.5x, 1.5x)
  - Z dimension (4x)
  - pJ/b/d2d xing (0.7x)
  - Cooling W/mm^2 (4x), /mm^3 (8x)

Building An Open Chiplet Economy

Monday, September 11, 2023 | Posted by Bapi Vinnakota, Engineer, Lawrence Berkeley Laboratory

Introduction

Chiplet-based products have recently emerged
vendors and cloud providers, including AMD, Ir
technology to extend Moore's law. Their remar
motivations: (1) to avoid very large die sizes fo
diversification through mix-and-match strategie
heterogeneous integration - integrating chiplet
and/or performance optimization. One expects
companies developing semiconductor product
domain-specific accelerators is actually domai

High-performance, power-efficient three-dimensional system-in-package designs with universal chiplet interconnect express

Debendra Das Sharma, Gerald Pasdast, Sathya Tiagaraj & Kemal Aygün

Nature Electronics (2024) | Cite this article

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Abstract

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