Rapidus Corporation

Managing shareholders
Terry Higashi  Atsuyoshi Koike

Founding individual shareholders (12 people)

Group of semiconductor experts established company (8/10/2022)

Investing 8 Japanese companies (10/31/2022)

- KIOXIA
- SONY
- SoftBank
- DENSO
- NEC
- NTT
- MUFG
- TOYOTA
Rapidus differentiates in speed.

World’s Shortest Total Cycle-Time
Rapidus secures $3.9 billion for FY 2024 budget from Japan Gov.

Japan approves $3.9 billion in subsidies for chipmaker Rapidus

Story by Reuters • 2d • 1 min read

Including Back-end

Tokyo (Reuters) - Japan’s industry ministry said on Tuesday it has approved subsidies worth up to 590 billion yen ($3.9 billion) for chip foundry venture Rapidus as Tokyo pushes forward with plans to rebuild the country’s chip manufacturing base.

Japan previously agreed to provide subsidies worth some 330 billion yen to Rapidus. The newly approved aid includes 53.5 billion yen for advanced packaging, which is becoming increasingly important for driving chip performance improvement.

Financial Support from Gov.

<table>
<thead>
<tr>
<th>Year</th>
<th>Amount (yen)</th>
<th>Amount (US$)</th>
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<tbody>
<tr>
<td>FY 2022</td>
<td>¥70 billion</td>
<td>$0.5 billion</td>
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<tr>
<td>FY 2023</td>
<td>¥260 billion</td>
<td>$1.7 billion</td>
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<tr>
<td>FY 2024</td>
<td>¥590 billion</td>
<td>$3.9 billion</td>
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<tr>
<td>Total</td>
<td>¥920 billion</td>
<td>$6.1 billion</td>
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To establish design and manufacturing technology for advanced chiplet package using 2nm generation semiconductors (2.xD, 3D), a pilot line will be established in Japan and the following development items will be implemented aiming for volume production and implementation.

- **Item 1**: Development of 3D (2.xD, 3D) package manufacturing technology including 2nm generation semiconductors
  Features: Development of organic insulation RDL interposer by 600mm square working panel, verification of 3D package technology and mass production technology.

- **Item 2**: Design and testing technology development for high-efficiency/high-performance chiplet packages optimized for each application
  Features: Development of design kits (Assembly Design Kit) for customers and KGD sorting test technology (wafer level/die level).

**International Collaboration**: IBM, USA, Fraunhofer, Germany, STAR IME, Singapore

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**Design and Manufacturing Technology Development of Chiplet Package for 2nm Semiconductor**
Innovative Integration for Manufacturing
Back-end Pilot Line Location

- **EPSON Chitose Plant**
- **Rapidus Pilot line setup (Partial floors)**
- **NEW CHITOSE AIRPORT**
- **Semiconductor Fab (IIM-1 & 2)**