HETEROGENEOUS INTEGRATION ROADMAP

Advanced Manufacturing & Multichip Integration TWG

Technical Working Group

February 22,2024

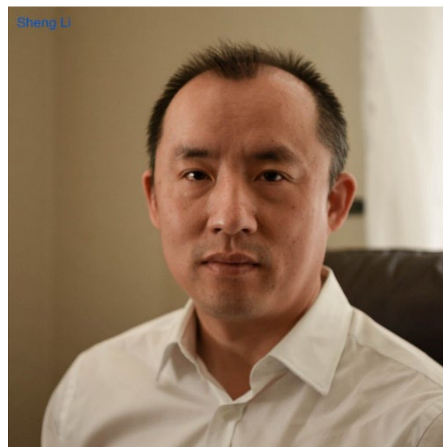
IEEE
IEEE photonics Society
semi
IEEE ELECTRONICS PACKAGING SOCIETY
ASME
ELECTRON DEVICES SOCIETY

Today's Speakers

HIR

Bill Chen
ASE Group

Kris Erickson
META



Sheng Li
Intel

Abhijit Dasgupta
UMD

Lei Shan
Ampere

Benson Chan
Binghamton Univ.

Annette Teng
SUNY Polytechnic

Ivy Qin
Kulicke and Soffa Industries

Mark Gerber
ASE Group

Srikanth Rangarajan
Binghamton Univ.

HETEROGENEOUS INTEGRATION ROADMAP

Advanced Manufacturing & Multichip Integration

	Topic	Lead
1.	Electrical Performance	Lei Shan
2.	Thermal Management	Srikanth Rangarajan
3.	Mechanical Engineering	Benson Chan
4.	Adv Manufacturing & Package Assembly	Annette Teng
5.	Wire bond Innovations	Ivy Qin
6.	Flip Chip & Hybrid Bonding	Mark Gerber
7.	Advanced Substrate	Sheng C Li
8.	Additive Manufacturing	Kris Erickson
9.	Reliability (Spun-Off: full TWG 2021)	Abhijit Dasgupta
10.	Solder & Electromigration	Eric Cotts

William (Bill) Chen & Annette Teng TWG Chair & Co-Chair

IEEE · IEEE photonics Society · semi · IEEE Electronics Packaging Society · ASME · Electron Devices Society

SINGLE & MULTICHIP ROADMAP METRICS

HETEROGENEOUS INTEGRATION ROADMAP

Year of Production	*2022*	*2023*	*2024*	*2025*	*2026*	*2027*	*2028*
On-chip feature size (nm)							
Memory (DDR/HBM)	7	5	5	5	3	3	3
Smart Phone / Laptop	5	3	3	3	2	2	2
High-performance (note1), chiplet/monolithic	5	3	3	3	2	2	2
Core Voltage (Minimum Volts)							
Memory (DDR/HBM)	1.1	1	1	1	0.9	0.9	0.9
Smart Phone / Laptop	0.8	0.75	0.75	0.75	0.7	0.7	0.7
High-performance	0.8	0.75	0.75	0.75	0.7	0.7	0.7
Package Pin count Maximum							
Memory (DDR/HBM)	288/3200	288/3200	288/3200	288/3200	350/4700	350/4700	350/4700
Smart Phone / Laptop	1212/7000	1275/7600	1275/7600	1275/7600	1396/8400	1396/8400	1396/8400
High performance (note3)	7800	7800	9600	9600	9600	11200	11200
Minimum Package Dimension (mm)							
Memory (DDR/HBM)	133/10	133/10	133/10	133/10	133/12	133/12	133/12
Smart Phone / Laptop	50	55	55	55	60	60	60
High-performance	87	87	95	95	95	110	110
Performance: On-Chip							
Memory (DDR/HBM), MHz	800	1000	1000	1200	1200	1600	1600
Smart Phone / Laptop, GHz	3.2	4	4	4.8	4.8	5.2	5.2
High-performance, GHz	8	8	9.6	9.6	11.2	11.2	11.2
Interconnect: Chip-to-Chip *(note4)*							
Memory (DDR/HBM), Gb/s	4.8/3.6	4.8/5.2	5.6/6.4	6.4/7.2	7.2/8.0	8.0/9.6	9.6/9.6
Smart Phone / Laptop, Gb/s	100	100	100	200	200	200	200
High-performance, Gb/s	32	32	32	64	64	64	112
Interconnect: Pkg-to-Board							
Memory (DDR/HBM), Gb/s	8/6.4	8/6.4	9.6	12.8	16	25	25
Smart Phone / Laptop, Gb/s	100	100	100	200	200	200	200
High-performance, Gb/s	56	56	64	64	112	112	224

IEEE · IEEE photonics Society · semi · IEEE ELECTRONICS PACKAGING SOCIETY · ASME SETTING THE STANDARD · ELECTRON DEVICES SOCIETY

UCIe to Enable Low-Power & High-Bandwidth Chiplet Integration

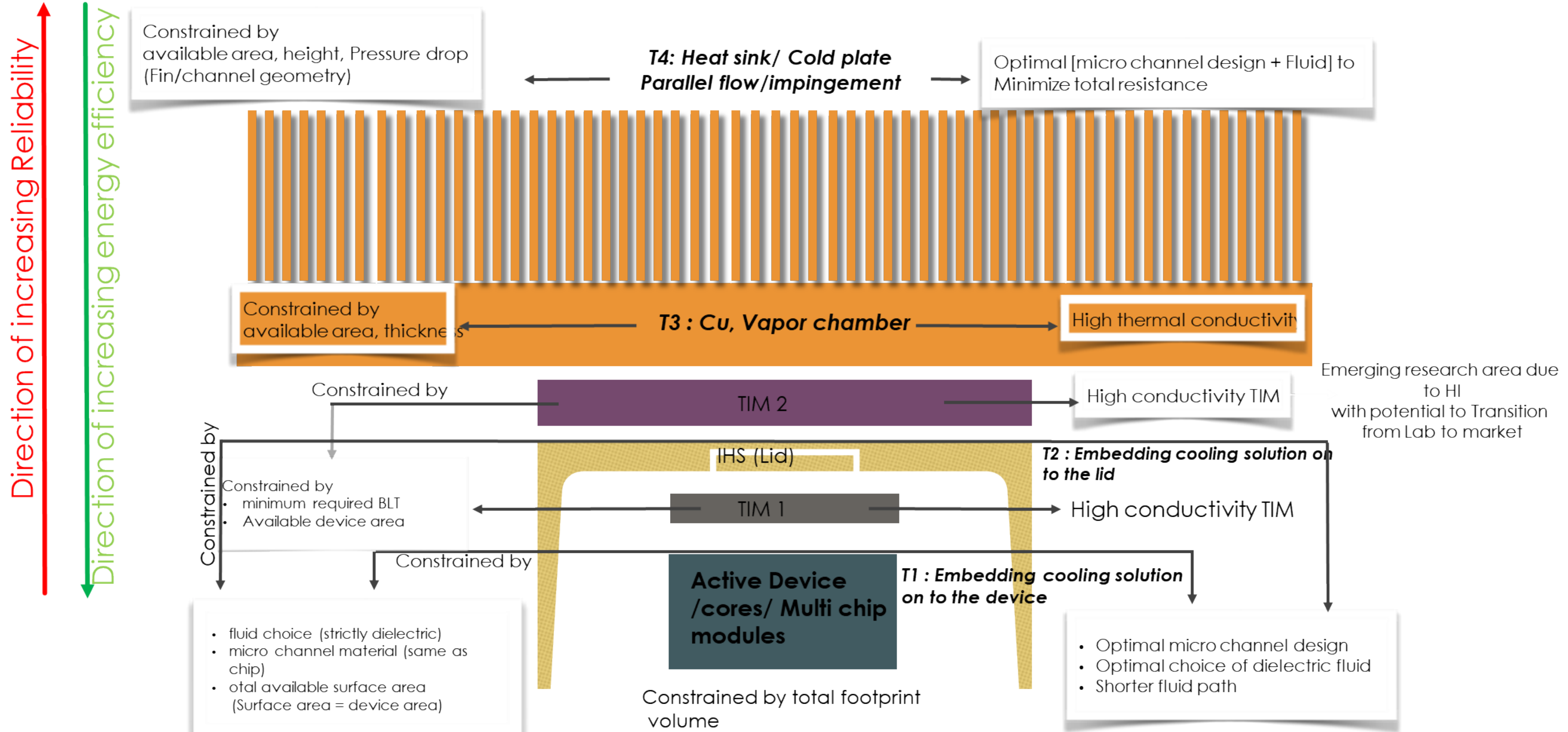
HETEROGENEOUS INTEGRATION ROADMAP

Characteristics / KPIs	Standard Package	Advanced Package	Comments
Characteristics			
Data Rate (GT/s)	4, 8, 12, 16, 24, 32		Lower speeds must be supported -interop (e.g., 4, 8, 12 for 12G device)
Width (each cluster)	16	64	Width degradation in Standard, spare lanes in Advanced
Bump Pitch (um)	100 – 130	25 - 55	Interoperate across bump pitches in each package type across nodes
Channel Reach (mm)	<= 25	<=2	
Target for Key Metrics			
B/W Shoreline (GB/s/mm)	28 – 224	165 – 1317	Conservatively estimated: AP: 45u for AP; Standard: 110u; Proportionate to data rate (4G – 32G)
B/W Density (GB/s/mm^2)	22-125	188-1350	
Power Efficiency target (pJ/b)	0.5	0.25	
Low-power entry/exit	0.5ns <=16G, 0.5-1ns >=24G		Power savings estimated at >= 85%
Latency (Tx + Rx)	< 2ns		Includes D2D Adapter and PHY (FDI to bump and back)
Reliability (FIT)	0 < FIT (Failure In Time) << 1		FIT: #failures in a billion hours (expecting ~1E-10) w/ CXi Flit Mode

Optimization Opportunities for heterogeneous integrated packages

Constrained by overall footprint and height of the package module

HETEROGENEOUS INTEGRATION ROADMAP



IEEE | IEEE photonics Society | semi | IEEE ELECTRONICS PACKAGING SOCIETY | ASME SETTING THE STANDARD | ELECTRON DEVICES SOCIETY

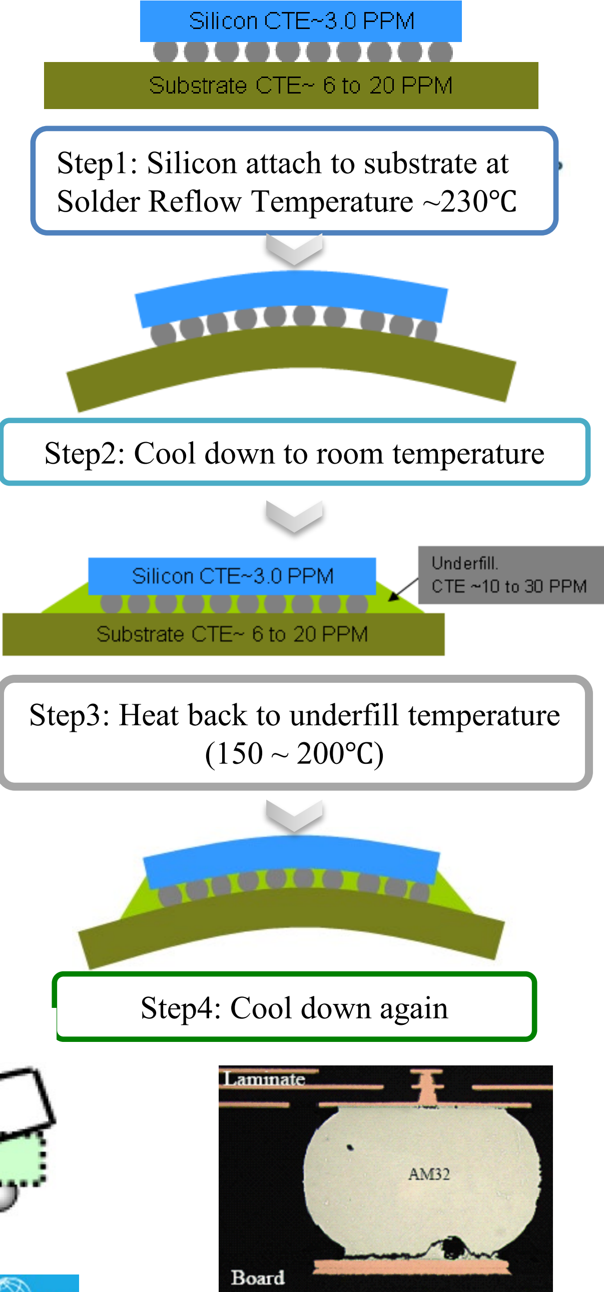
Warpage Engineering, Chip-Package-Interaction (CPI)

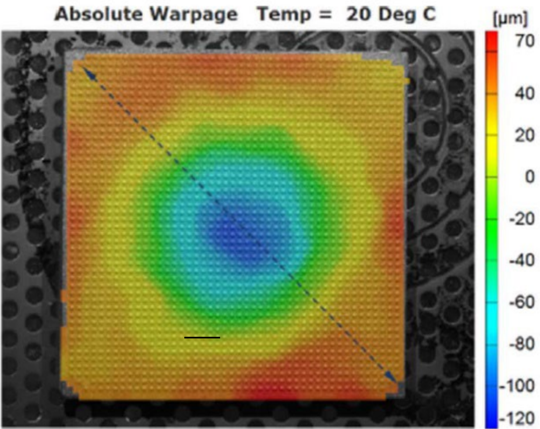
Warpage Engineering

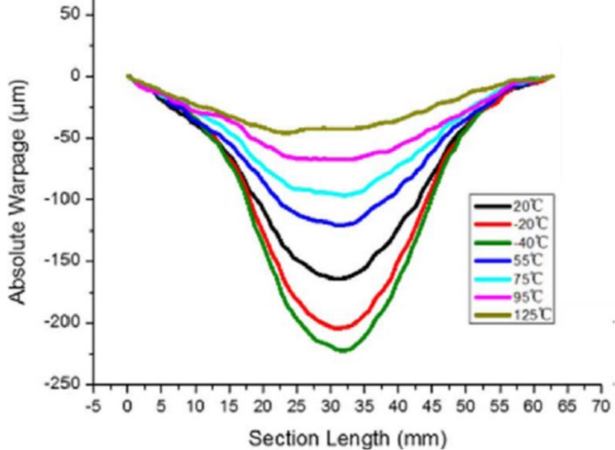
Assembly stress due to warpage is the largest contributor to failures in packaging. Some of the variables leading to the warpage include substrate materials, copper distribution (wiring density), number of layers, underfill material, die thickness, processing temperatures, humidity…

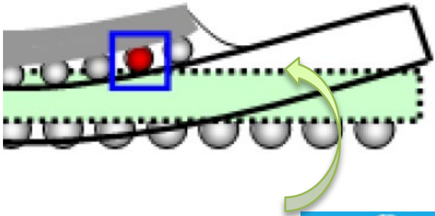
Reducing warpage and stress will contribute to higher yields and better reliabilit

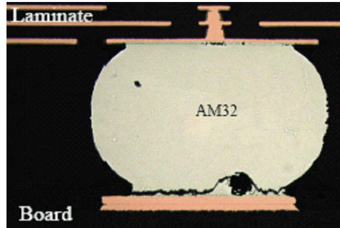
As interconnect pitches go down, the warpage window for packages will be reduced









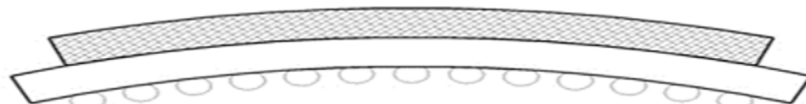


WARPAGE REDUCTION ROADMAP

Table 2: Warpage Allowance across two market segments

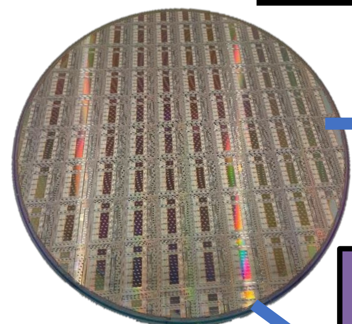
Segment	Year of Production / Pitch (mm)	2018	2019	2020	2023	2026	2029	2030
HPC	1.0	-0.13, +0.21	-0.11, +0.18	-0.11, +0.18	-0.11, +0.18	-0.10, +0.16	-0.08,+0.16	-0.08,+0.17
HPC	1.0	-0.13, +0.20	-0.11, +0.18	-0.11, +0.18	-0.11, +0.18	-0.10, +0.15	-0.08,+0.15	-0.08,+0.16
HPC	0.8	-0.13, +0.21	-0.11, +0.18	-0.11, +0.18	-0.11, +0.18	-0.10, +0.16	-0.08,+0.16	-0.08,+0.17
HPC	0.8	-0.10, +0.10	-0.09, +0.09	-0.09, +0.09	-0.09, +0.09	-0.08, +0.08	-0.07, +0.07	-0.07, +0.07
HPC	0.65	-0.10, +0.10	-0.09, +0.09	-0.09, +0.09	-0.09, +0.09	-0.08, +0.08	-0.07, +0.07	-0.07, +0.07
HPC	0.65	-0.09, +0.09	-0.08, +0.08	-0.08, +0.08	-0.08, +0.08	-0.07, +0.07	-0.065, +0.065	-0.065, +0.065
Mobile	0.5	-0.09, +0.09	-0.08, +0.08	-0.08, +0.08	-0.08, +0.08	-0.07, +0.07	-0.065, +0.065	-0.065, +0.065
Mobile	0.5	-0.08, +0.08	-0.07, +0.07	-0.07, +0.07	-0.07, +0.07	-0.065, +0.065	-0.06, +0.06	-0.06, +0.06
Mobile	0.4	-0.08, +0.08	-0.07, +0.07	-0.07, +0.07	-0.07, +0.07	-0.065, +0.065	-0.06, +0.06	-0.06, +0.06
Mobile	0.4	-0.07, +0.07	-0.065, +0.065	-0.065, +0.065	-0.065, +0.065	-0.06, +0.06	-0.055, +0.055	-0.055, +0.055
Mobile	0.3	-0.07, +0.07	-0.065, +0.065	-0.065, +0.065	-0.065, +0.065	-0.06, +0.06	-0.055, +0.055	-0.055, +0.055
Mobile	0.3	-0.06, +0.06	-0.055, +0.055	-0.055, +0.055	-0.055, +0.055	-0.05, +0.05	-0.045,+0.045	-0.045,+0.045
Mobile	0.25		-0.055, +0.055	-0.055, +0.055	-0.055, +0.055	-0.05, +0.05	-0.045,+0.045	-0.045,+0.045
Mobile	0.25			-0.055, +0.055	-0.055, +0.055	-0.05, +0.05	-0.045,+0.045	-0.045,+0.045
Mobile	0.2			-0.055, +0.055	-0.055, +0.055	-0.05, +0.05	-0.045,+0.045	-0.045,+0.045
Mobile	0.2				-0.045,+0.045	-0.045,+0.045	-0.045,+0.045	-0.045,+0.045
Mobile	0.15				-0.045,+0.045	-0.045,+0.045	-0.045,+0.045	-0.045,+0.045
Mobile	0.15				-0.025,+0.025	-0.025,+0.025	-0.025,+0.025	-0.025,+0.025
Mobile	0.1				-0.025,+0.025	-0.025,+0.025	-0.025,+0.025	-0.025,+0.025
Mobile	0.1					-0.020,+0.020	-0.020,+0.020	-0.020,+0.020

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



HI Single and Multi Chip Manufacturing

HIR
HETEROGENEOUS INTEGRATION ROADMAP



Bumping for interconnect

PVD UBM → PR Coat → Thickness → Stepper → PR Strip → Descum → Cu/Ni/Sn Plating → Strip UBM → Bump reflow → coplanarity → Tape lamination → Wafer Thinning

Wafer Thinning

Wafer Singulation

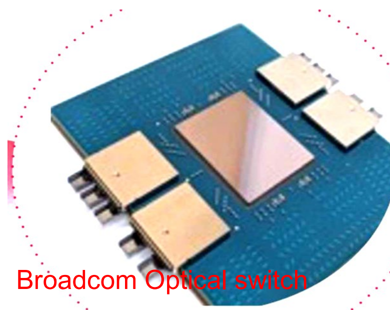
Pick & Place or Stack

Die attach → Die shear → Wirebond → Wire pull → Epoxy mold → Postmold cure → CSAM

Flip Chip/ TCB/ Hybrid Bonding* → X-ray → Underfill → CSAM

Others* (heatsink/ fiber attach; marking, etc.) → TEST

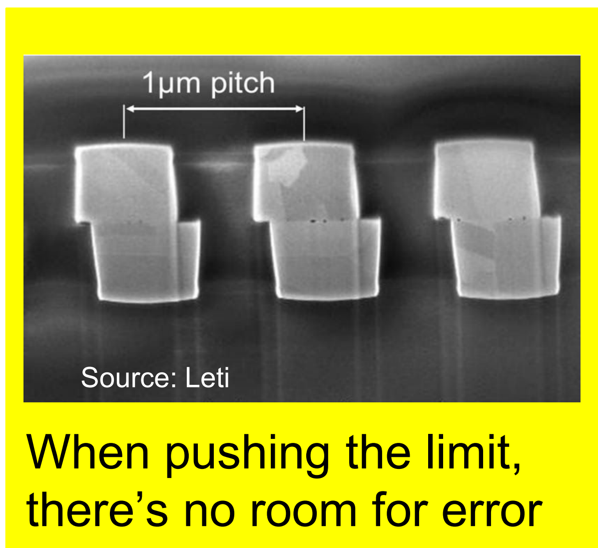
* Represents multiple process steps



Broadcom Optical switch

Annetteteng@promex-ind.com

HI ASSEMBLY KEY CHALLENGES



When pushing the limit, there's no room for error

Annetteteng@promex-ind.com

Chip size, Chip thickness

Bond tool accuracy

Process thermal budget

Surface conditioning

Particle control

Smoothness

Metal density

Dicing quality

Warpage control

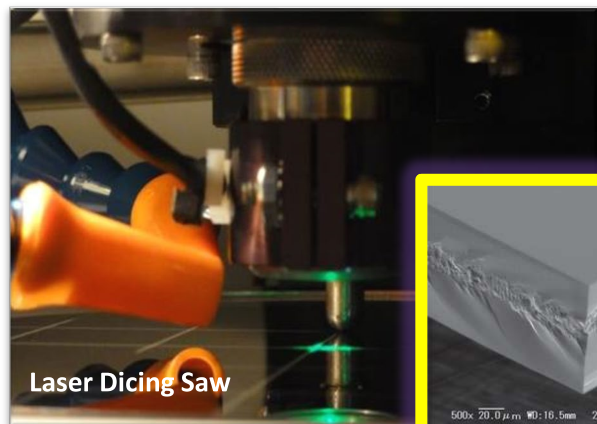
Adapted from
S. W. Liang, Gene C. Y. Wu, K. C. Yee, C. T. Wang, Ji James Cui, and Douglas C. H. Yu "High Performance and Energy Efficient Computing with Advanced SoICTM Scaling" 2022 ECTC, Taiwan Semiconductor Manufacturing Company

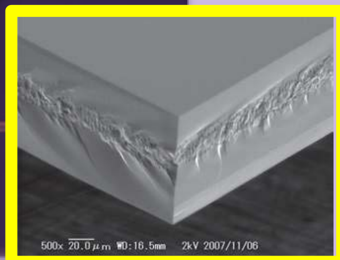
HIR HETEROGENEOUS INTEGRATION ROADMAP

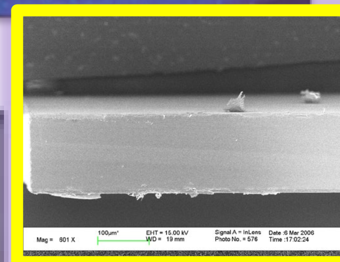
IEEE IEEE photonics Society semi IEEE ELECTRONICS PACKAGING SOCIETY ASME SETTING THE STANDARD ELECTRON DEVICES SOCIETY

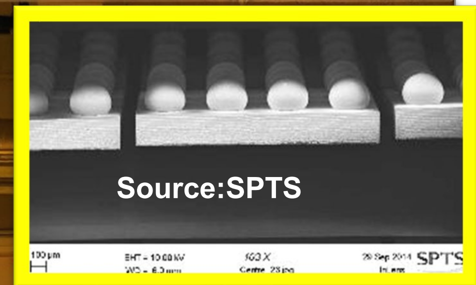
WAFER SINGULATION

HIR
HETEROGENEOUS INTEGRATION ROADMAP









Source:
DISCO

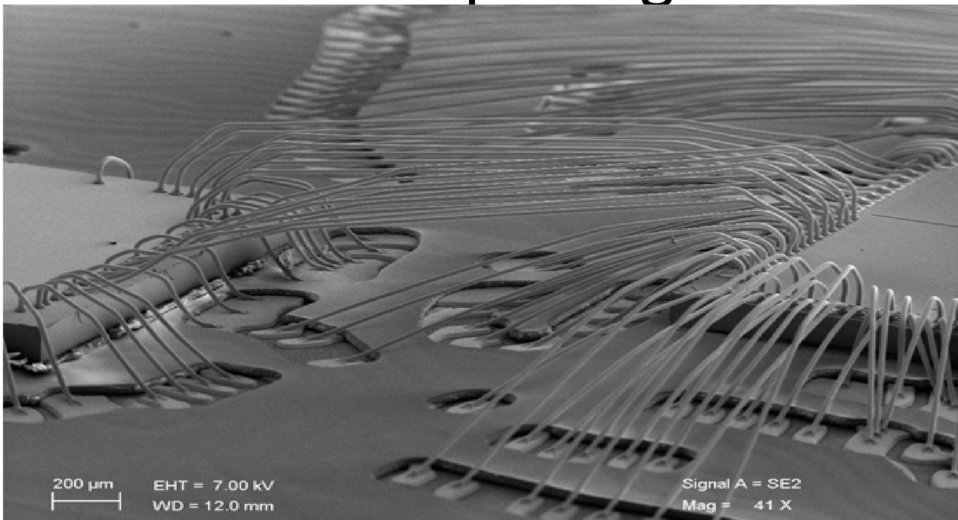
Annetteteng@promex-ind.com

IEEE | IEEE photonics Society | semi | IEEE ELECTRONICS PACKAGING SOCIETY | ASME SETTING THE STANDARD | ELECTRON DEVICES SOCIETY®

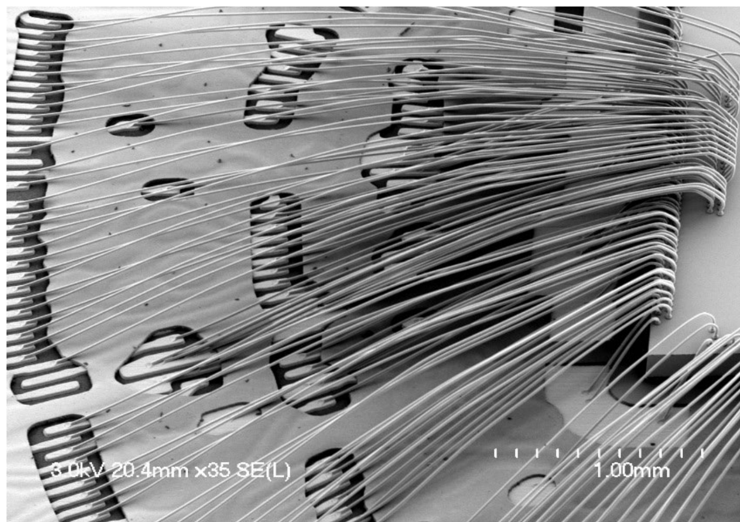
Increased Interconnect Density

HIR
HETEROGENEOUS INTEGRATION ROADMAP

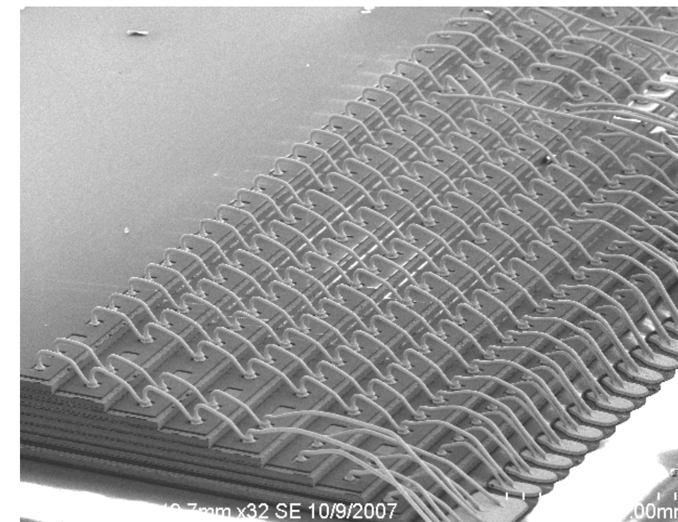
The finest inline pitch of wire bonding has remained around 35um. However, wire bonding interconnect density continuously increases through higher level of system integration such as SiP, stack die and Multi-tier packages.



SiP with Die to Die Wire Bond Interconnect



High Density Multi-tier Package



Stacked Memory Device

IEEE IEEE photonics Society semi IEEE ELECTRONICS PACKAGING SOCIETY ASME ELECTRON DEVICES SOCIETY

Flip Chip Interconnect Pitch Roadmap –HIR 2023

HIR
HETEROGENEOUS INTEGRATION ROADMAP

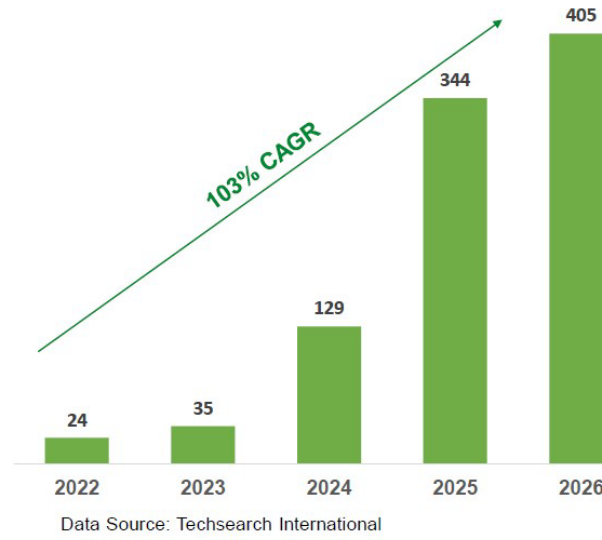
Table HI-4 Chip-to-package Substrate Technology Requirements (Updated Nov 2023)

Year of Production	*2018*	*2019*	*2020*	*2021*	*2022*	*2023*	*2025*	*2028*	*2031*	*2034*
Flip Chip Pitch										
Flip Chip- Large Body Solder >12mm Sq Die	135	130	130	130	130	130	130	130	130	130
Flip Chip- Small Body Solder <12mm Sq Die	135	130	130	130	130	130	130	130	130	130
Flip Chip - Cu Pillar Small Body <12mm Sq Die (Periphery Staggered, Inline Same as large Body Cu	40/80	30/60	30/60	30/60	30/60	20/40	15/30	15/30	15/30	15/30
Flip Chip- Cu Pillar Large Body >12mm Sq Die	120	110	110	110	110	105	100	90	90	80
Flip Chip Solder - COW	50	50	50	50	50	50	50	50	50	50
Flip Chip Cu Pillar -COW (Chiplets on Si)	40	40	40	35	30	30	22	16	13	10
Flip Chip Cu Pillar -COW (Chiplets on RDL)	50	50	45	45	45	45	40	40	30	30
Wafer to Wafer Cu to Cu Interconnect	5	5	5	2	2	2	2	1	1	1
Die to Wafer Cu to Cu Interconnect (Hybrid)	30	20	20	9	9	9	6	6	3	3
Embedded Die In Substrate Interconnect Pitch	120	120	120	120	90	70	60	50	50	50

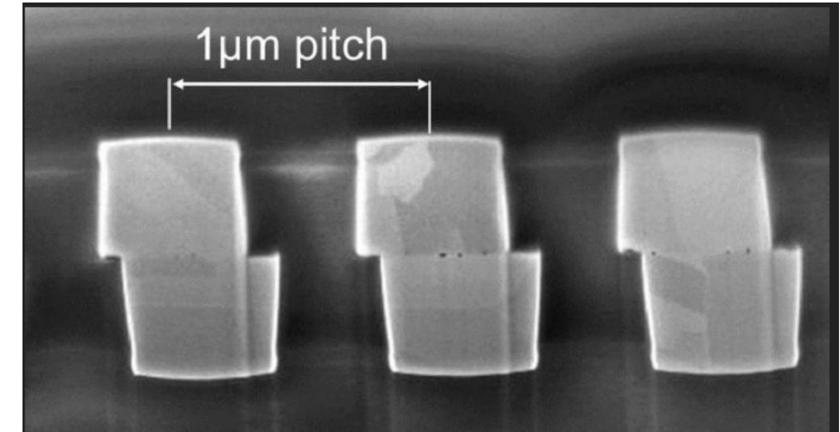
Manufacturable solutions exist, and are being optimized (white)
Manufacturable solutions are known (yellow)
Interim solutions are known (yellow striped)
Manufacturable solutions are NOT known (pink)

IEEE · IEEE photonics Society · semi · IEEE Electronics Packaging Society · ASME · Electron Devices Society

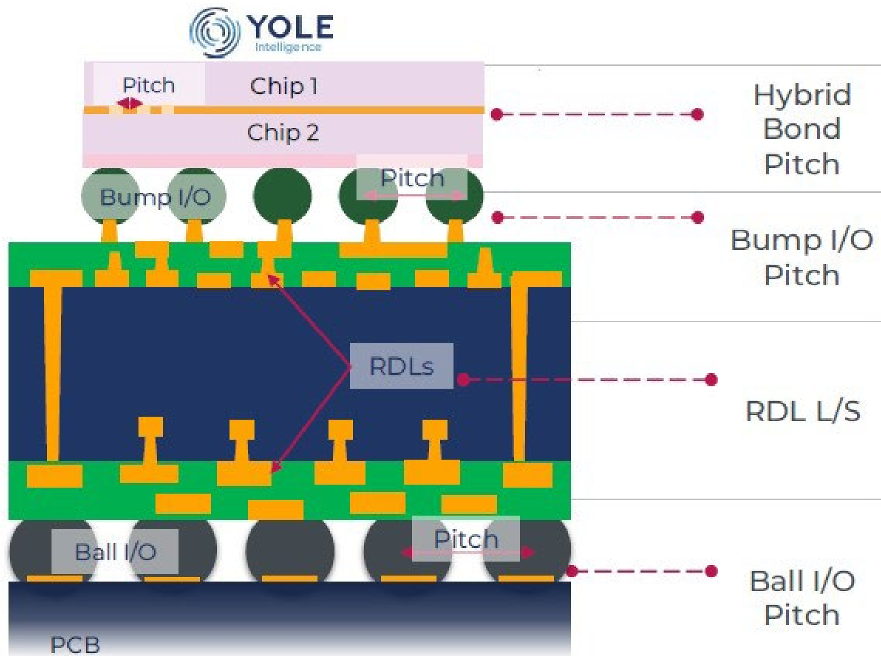
Hybrid Bonding Enabling Next Generation of Chiplets

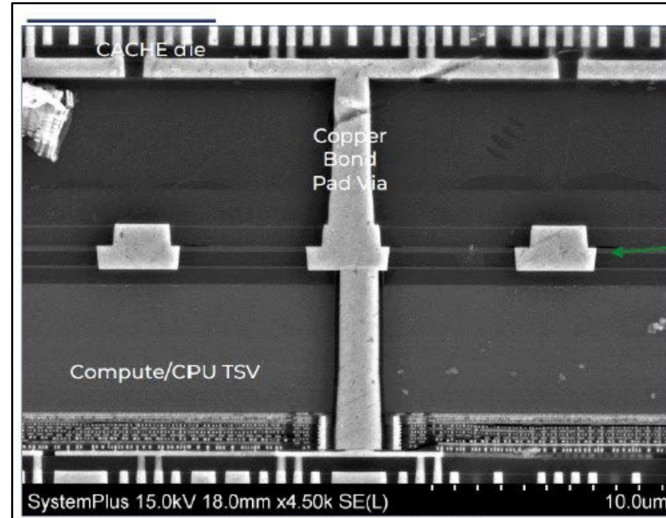


Wafer to Wafer Bonding



Source: Power Pulse



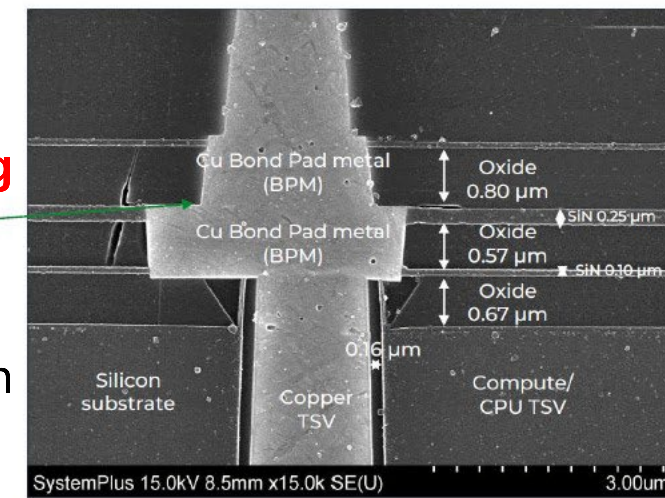


Package Cross-section #2

Die To Wafer Bonding

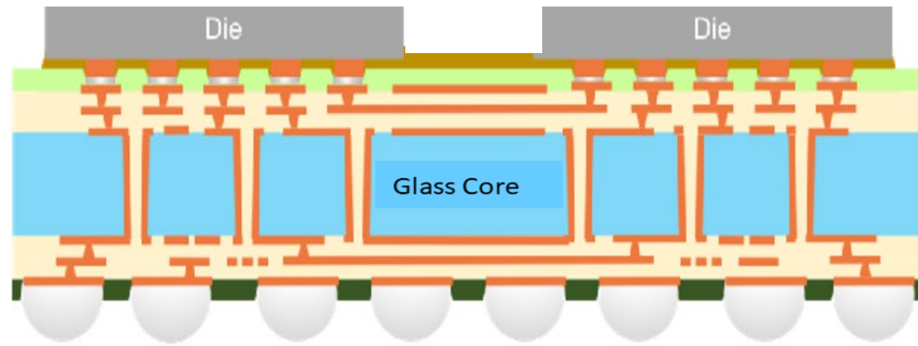
Hybrid Bond Interface

9um Pitch

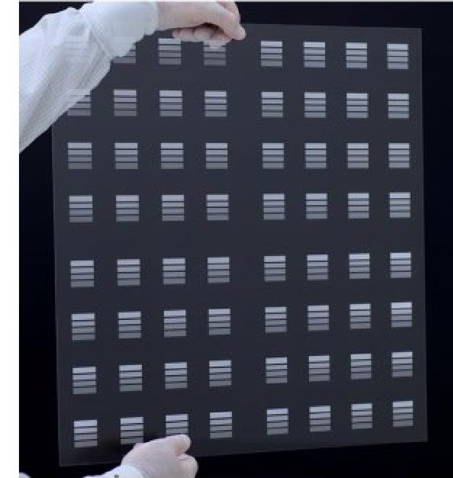


Source: Yole Development

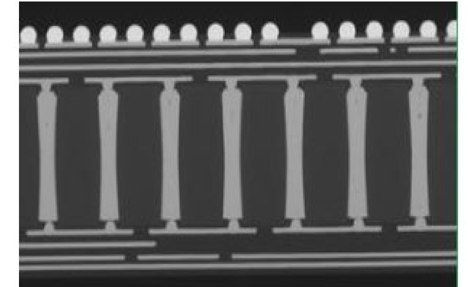
Glass Core Substrate



(Source: Intel)



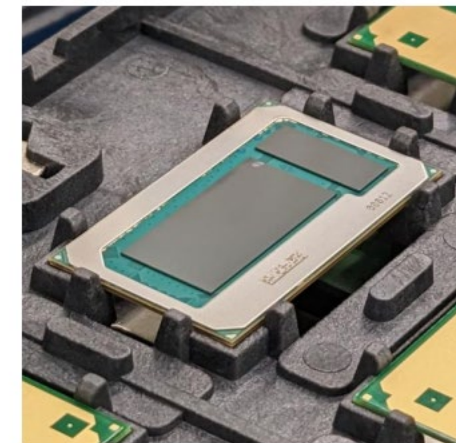
Glass Panel with Through Glass Vias (TGV)



X-section of a substrate test vehicle with 3 RDLs and 75um TGVs for client products

Glass core substrates enable significant improvement to both electrical and mechanical properties

- Tunable Modulus and CTE closer to silicon → Large form factor enabling
- Dimensional stability → Improved feature scaling
- Low Loss → High speed signaling
- High (~10x) through-hole density → Improved routing and signaling
- Higher Temperature Capability → Advanced integrated power delivery



(Source: Intel)

Fully assembled glass substrate

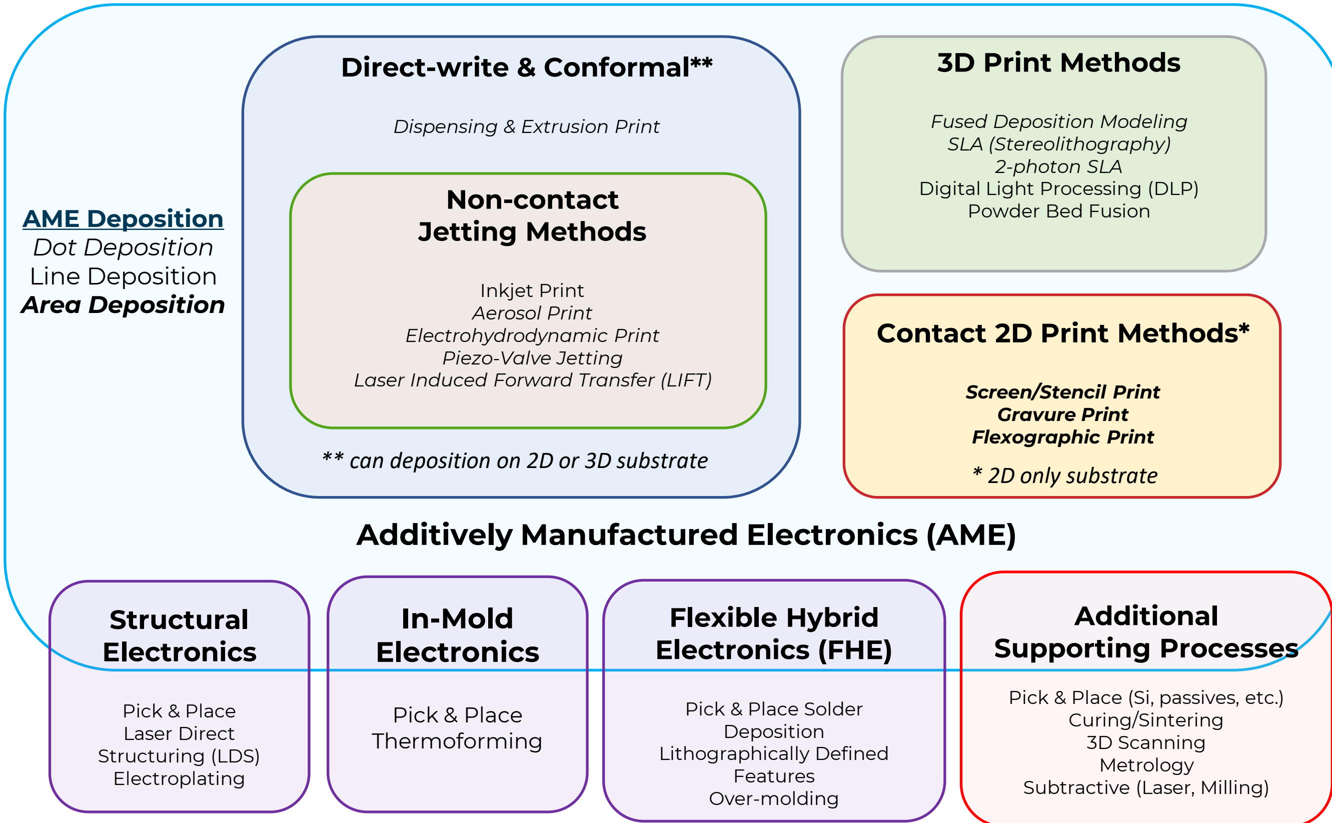
IEEE
IEEE photonics Society
semi
IEEE ELECTRONICS PACKAGING SOCIETY
ELECTRON DEVICES SOCIETY

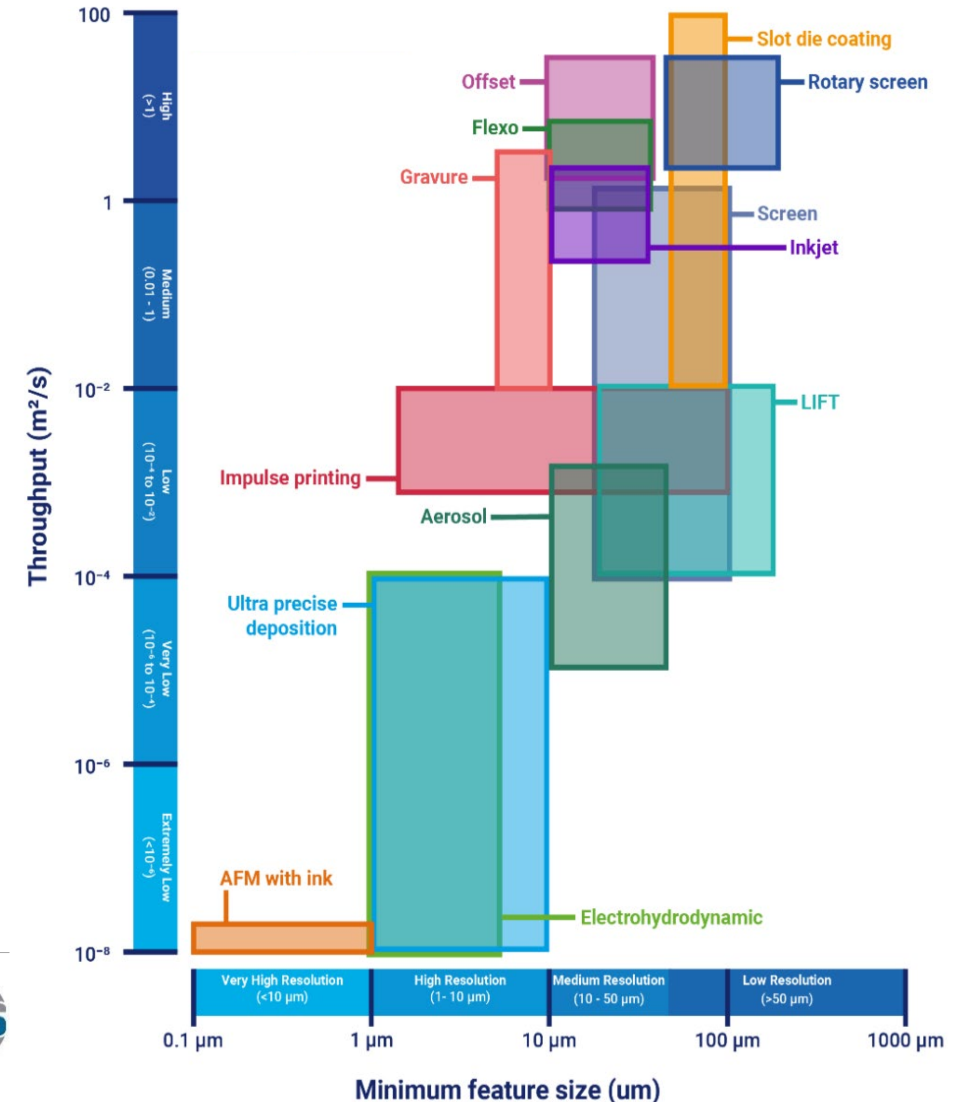
Additively Manufactured Electronics (AME)

HETEROGENEOUS INTEGRATION ROADMAP

AME = Printed Conductor + (Printed/Existing) Dielectric + (optional) Additional Processes

Thanks and with permissions from IDTechEx

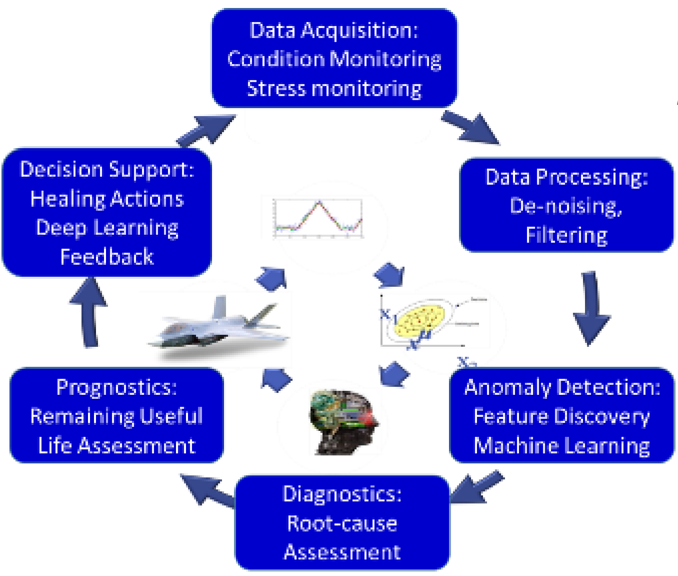




IEEE | IEEE photonics Society | semi | EPS

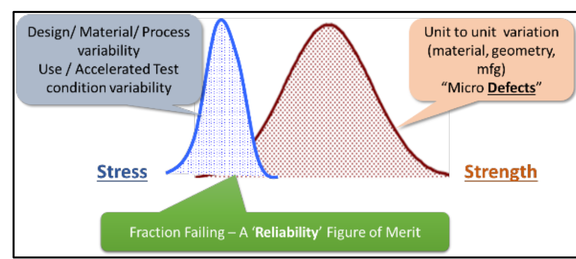
HI System reliability

Prognostics and Health Management

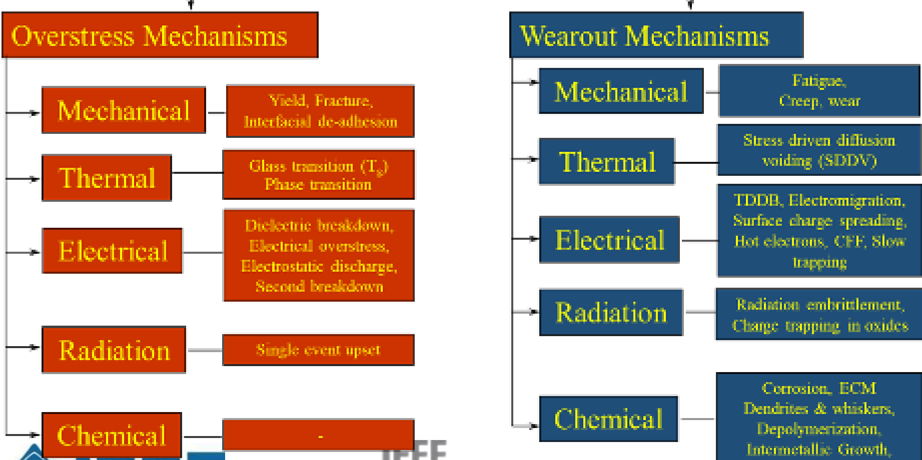


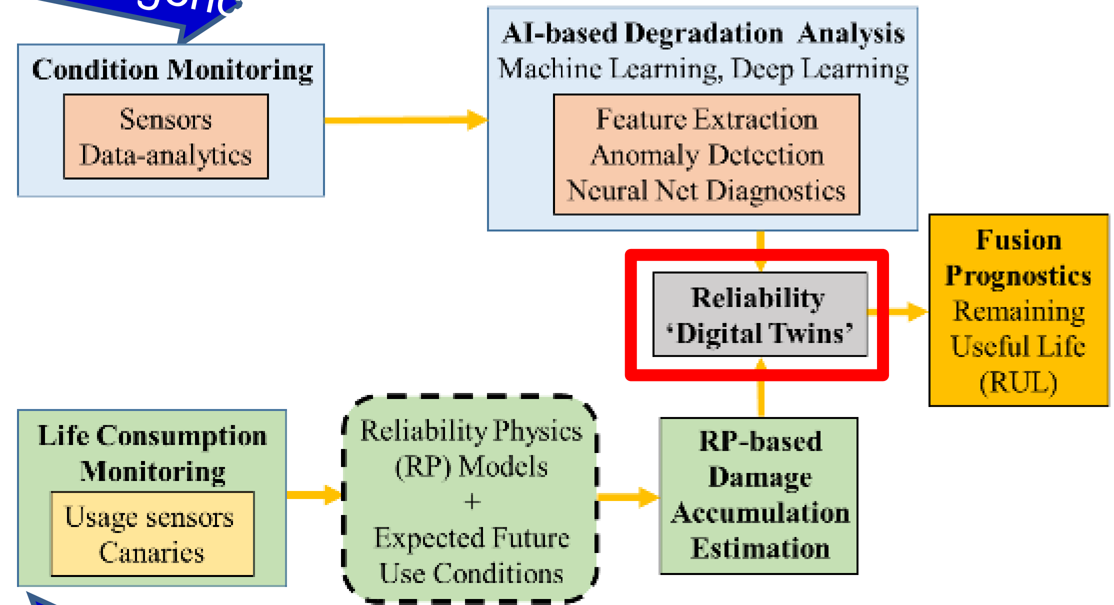
Fusion of bottom-up physics and top-down AI approaches

Machine Learning & Artificial Intelligence



Degradation and Failure Mechanisms





Reliability Physics

HIR HETEROGENEOUS INTEGRATION ROADMAP

IEEE · IEEE photonics Society · semi · IEEE ELECTRONICS PACKAGING SOCIETY · ASME · ELECTRON DEVICES SOCIETY

Modes/Mechanisms/Models for degradation & failure

Electrical Thermal Moisture Thermo-mechanical Mechanical DfR Methods MfR Methods

Multiphysics

Multiscale

Devices

Interconnects

Packaging/ System

Module/System

Multiscale Integration	Multi Physics	Electrical Stress		SI/PI (Electrical Performance)	Thermal Analysis	Moisture		Thermal Mechanical Stress		Mechanical Stress		Thermal Interaction with SI/PI	Stress Interaction with SI/PI	Simulation/Modeling and Co-Design Flows			Manufacturing Variability	Material Property and Variability
		Failure Modes	Failure Mechanism and Reliability Models			Failure Modes	Failure Mechanism and Reliability Models	Failure Modes	Failure Mechanism and Reliability Models	Failure Modes	Failure Mechanism and Reliability Models			Failure Modes	EDA flows	PDK/ADK		
Transistor	FinFET and GAA	Leakage current, ripple currents, unstabel perfofrmance and ESD	N/PBTI models with recovery; HCI model; TDDB Weibull model; Oxide & junction breakdown model	Transistor SPICE	FinFET SHE	No known failures	None	FinFET SHE channel stress; µBump/C4 bump/TSV; system level stresses	FinFET SHE Models; CPI Model; Piezo-electrical models	No known failures	None	SHE effect on SPICE parameters	Influence of Si stress on SPICE paramters	Effects of degradation mechanisms and process variabilities on electrical functionality	Cadence; Relxpert; Mentor Graphics	Integrate of degradation models into Device SPICE Model		
Interconnects	MEOL/BEOL Metal/Via /ELK	Electromigration; Inter Layer Dielectric ELK Breakdown; MEOL Oxide Breakdown; EOS	Electromigration model; Dielectric breakdown model	Extraction of RLC Model	Joule Heating simulation; SHE effects on MEOL/BEOL	Pad and underline metal corrosion; Cu/ELK delamination 3. Cu loss/diffusion	Electrochemical corrosion; Interface degradation due to moisture absorption; Barrier metal oxidation	SHE failure in Cu/ELK, MEOL, BEOL, µBump, TSV; RDL failures from package stress, Cu fatigue; LowK/ELK layer cracking & delamination	Creep induced voiding; CTE mismatch; SHE induced localized thermal cycling	LowK/ELK layer cracking & delamination	Fatige by bending	Joule/SHE temp effects on RLC	Effect of Cu/ELK stress on RLC	CPI induced Cu/ELK cracking; JHE/SHE stresses; stress from bumps/TSV/RDL & Packaging	Ansys Mentor			
	FBEOL RDL/Dielectric	RDL/UBM Electromigration	Electromigration	Extraction of RDL RLC Model	BEOL Joule/SHE effect on RDL temperature	Cu dedrite	Electro-chemical corrosion	RDL cracking	µbump/TSV/ Package/ Board effects on RDL stress			Effect of RDL temp on electrical model	Effect of RDL stress on electrical model	CPI/CBPI induced failures: RDL cracking & delamination	Effect of temp and stress on RDL EM			
	Au/Cu Wirebonding	Electromigration				IMC Corrosion		Bond wire fatigue		Cu/ELK cracking	Bonding force models							
	µBump/C4 Bump/UBM	Electromigration induced voids	Black's model; Mutiphysics EM model including elctron, thermal gradient, stress gradient and atomic diffusion	µbump electrical model	Die Internal Joule/SHE temp effect & external temp effect on bump temperature	UBM delamination	Galvanic effect (electro-chemical reaction)	Bump joint cracking; Under Bump ELK cracking; Under pad cracking in substate	CTE mismatch induced stress; Fatigue	Tensile stress causes bump peel; cracks at µbump; UBM and interface	Fracture/fatigue from shock, drop, impact, Vibr; e.g. in die attach, dielectric layer, inter-poser, UBM, solder joints	Effect of temp on bump electrical model	Effect of bump stress on electrical model	Multi Physics Bump EM - local current, temp, temp gradient and stress effect on µbump EM	Bump fatigue: effect of local temp & stress on fatigue life			
	TSV/Interposer/ EMIB	Electromigration; Barrier Dielectric breakdown	Black's model; Mutiphysics EM model including elctron, thermal gradient, stress gradient and atomic diffusion	TSV electrical model	Internal Joule/SHE temp effect on the TSV temp; External temp effect on TSV temp.			Cu pumping/TSV pop up	Cu extrsion due to CTE mismatch with Si; plastic rachetting at high temp			Effect of TSV temp on electrical model	Effect of TSV stress on electrical model	TSV EM response to local current, temp field and stress; TSV Pop out and effects on TSV/Si delaminaton	Barrier breakdown - How does voltage/current, temp and stress affect TSV barrier BD?	Package material thermal/mechanical properties; Die metal stack and thermal/mech properties; µBump/C4 bump/TSV thermal mechanical properties; Cu/ELK fracture criteria; Void initiation and propagation criteria; Interconnect fatigue/creep model; Package interface fracture criteria; Moisture diffusion and vapor pressure model; IMC thermal/mech/electrical properties; Photonics optical properties		
Packaging /System	Passivation	Passivation cracking	EOS induced cracking			Passivation cracking & delamination; underfill/Mold compound delamination		Passivation cracking	CPI stress in SiN									
	Underfill					Underfill to die/substrate delamination; underfill swelling	Moisture degradation in underfill & at interfaces	Bump joint cracking	Solder joint fracture and fatigue due to underfill expansion									
	High Density Substrate	Metal trace electromigration		Package Substrate RLC model extraction	Co-thermal sim from die to package	Metal trace corrosion		Metal trace/via cracking				Thermal - electrical perfromance interactions	Mechanical-electrical performance interactions	Cu trace EM - effect of local current, temp and stress	Thermal & mechanical effect on Cu trace/via cracking			
	Wafer Level Package							Warpage										
	Fanout Package							Warpage										
	2.x/2.5D Interposer Package (CoWoS and EMIB, etc)							Warpage; Embedded die delamination from substrate & sidewall; µvia & µbump cracking & delamination; Solder/TIM delamination										
	3D Package (Foveros, etc)				Mold compound pop-corn; Anisotropic conductive adhesive cracks		Mold compound pop-corning		FinFET Ion shift (due to TSV/Si CTE mismatch, µBump stress, shrinkage of underfill & EMC); TSV effects on BTI/HCI; BEOL cracking; Cu pillar joint failure; Mold compound pop-corn; conductive adhesive cracking									
	Chiplet/KGD	ESD						Die edge cracking; Under bump ELK cracking										
Module/ System	Printed Circuit Board Assembly	Leakage current and shorts from Conductive filament formation	electro-chemical metal migration	PCB Board electrical model	\Co-thermal sim from die to package to system	leakage current and shorts from loss of surface insulation resistance & conductive filament formation	moisture ingress, leading to fiber-matrix debonding, and electro-chemical metal migration	Solder joint cracking ; Cracking of PTH plating; PCB delamination; trace cracking; Warpage	thermomechanical fatigue of trace and solder, IMC fracture; CTE mismatches between: component / PWB, metallization/ dielectrics	Solder joint cracking; pad cratering	Stress exceeds the material and interface strength	Effects of PCB temp and corrosion on electrical model?	Effects of PCB stress on electrical model?	Board level Solder Joint Reliability	ANSYS Mechanical	PCB thermal/ mechanical properties; Solder joint fatigue/creep model; Solder joint dynamic/ properties		

HETEROGENEOUS INTEGRATION ROADMAP

Thank You

IEEE

IEEE photonics Society

semi

IEEE ELECTRONICS PACKAGING SOCIETY

ASME SETTING THE STANDARD

ELECTRON DEVICES SOCIETY