Heterogeneous Integration Roadmap for Aerospace and Defense (HIR-A/D)

Boeing Technical Fellow, BR&T
2024 IEEE-USA President-Elect
IEEE FNTC Vice-Chair
IEEE HIR TWG Co-Chair
Past President, IEEE MTT-S

Aerospace-Defense TWG Co-Chairs:
Tim Lee (The Boeing Company)
Dan Blass (Lockheed Martin)

February 2024

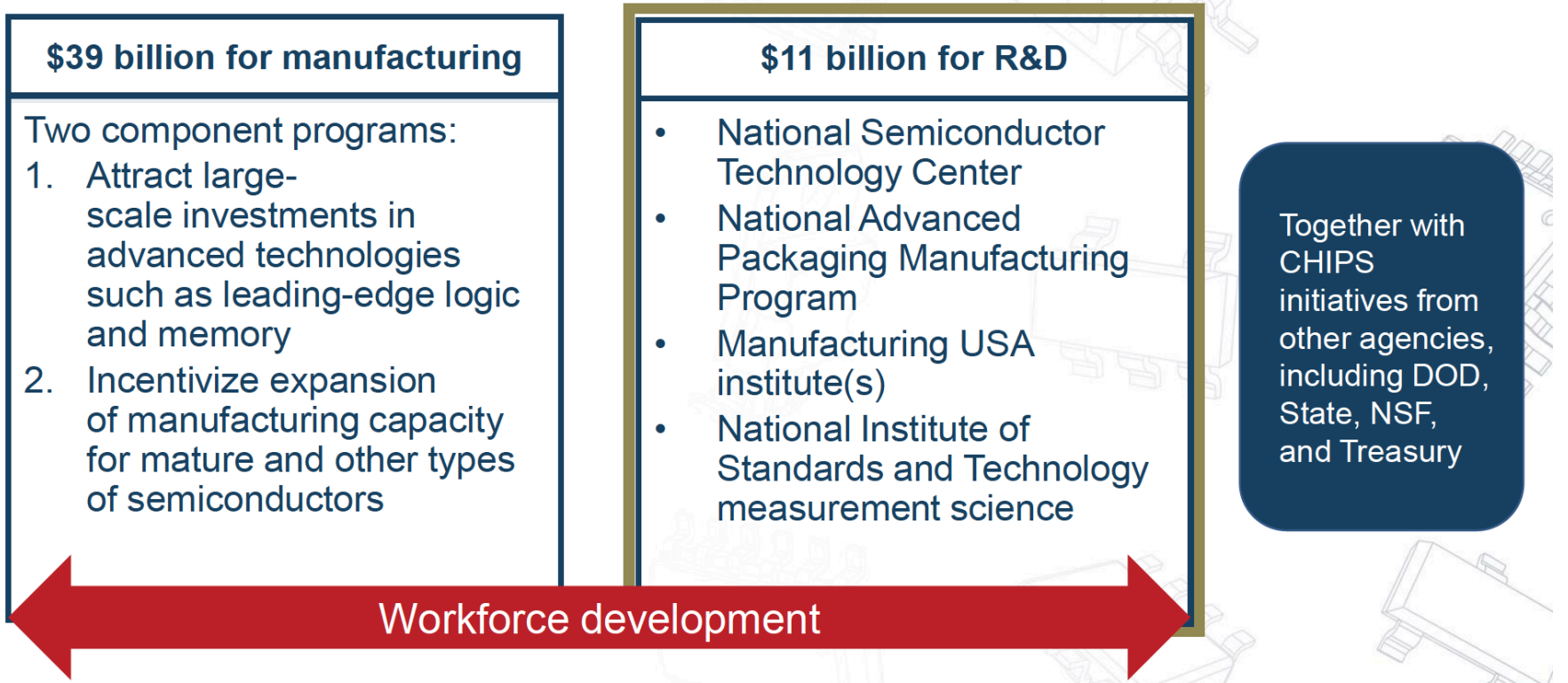
Timothy Lee, currently a Boeing Technical Fellow, is responsible for the development of RF and digital electronics for advanced communications networks and sensor systems. In the IEEE, Tim is promoting the use of technology to benefit humanity.

Summary of Topics Covered

- CHIPS Act – Department of Commerce
- EU CHIPS Act
- DoD Microelectronics Commons
- OSD/Crane SHIP, STEAM PIPE, STAMP
- DARPA ERI 2.0
  - NGMM
- IBAS Cornerstone RESHAPE

CHIPS for America Research and Development Program

CHIPS for America Incentives



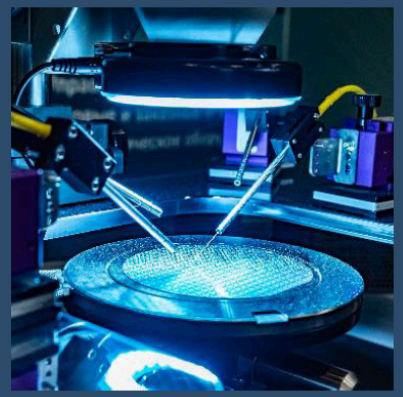
National Institute of Standards and Technology | U.S. Department of Commerce 42

IEEE USA in 2021-2022 let the way to inform Congress on the importance of the CHIPS Act

GlobalFoundries awarded $1.5B in Funding

- Biden-Harris Administration Announces Preliminary Terms with GlobalFoundries to Strengthen Domestic Legacy Chip Supply for U.S. Auto and Defense Industries
- The proposed funding would support a new state-of-the-art facility, significant capacity expansion, and the modernization of GF's U.S. manufacturing sites in New York and Vermont, which produce essential automotive, communications, and defense semiconductor technologies.

https://www.commerce.gov/news/press-releases/2024/02/biden-harris-administration-announces-preliminary-terms-globalfoundries



National Semiconductor Technology Center

Vision: Will serve as the **focal point** for research and engineering throughout the semiconductor ecosystem, advancing and enabling disruptive innovation to provide U.S. leadership in the industries of the future.

Structure: A public-private consortium as an independent entity with a governing board informed and advised by industry, academia, government, and key stakeholders.

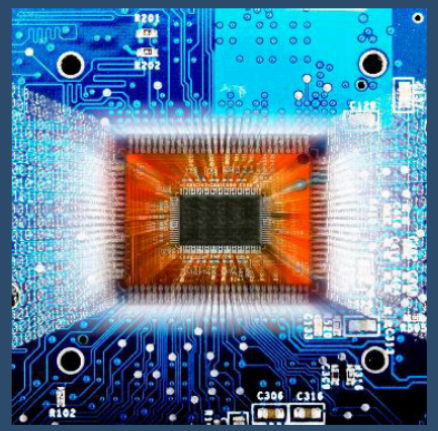
NatCast Formed

- The National Center for the Advancement of Semiconductor Technology, or Natcast, is a new, purpose-built, non-profit entity created to operate the National Semiconductor Technology Center (NSTC) consortium, established by the CHIPS Act of the U.S. government
- Mission
  - Extend America's leadership in semiconductor technology to provide the foundation for future applications and industries and to strengthen the U.S. semiconductor manufacturing ecosystem.
  - Significantly reduce the time and cost of moving from design idea to commercialization through access to shared facilities, digital assets and technical expertise for advancing design, prototyping, manufacturing, packaging, and scaling of semiconductors and semiconductor-related products.
  - Build and sustain a semiconductor workforce development ecosystem. The NSTC will serve as a coordinating body and center of excellence to scale the technical workforce, including scientists, engineers, and technicians. The NSTC workforce programs will include a focus on recruiting, training, and retraining the semiconductor workforce, including groups that are traditionally under-represented in the industry.

NetCast Leadership

DEIRDRE HANFORD – CHIEF EXECUTIVE OFFICER & TRUSTEE

Hanford was appointed Chief Executive Officer and Trustee of Natcast, Inc. in January 2024. Prior to Natcast, Hanford served as an executive at Synopsys, a technology and market leader in electronic design automation and semiconductor design intellectual property. Over the span of thirty-six years, Hanford's roles included being Chief Security Officer, Co-General Manager of the Synopsys Design Group, and leader of a variety of customer engagement, applications engineering, sales and marketing groups.



National Advanced Packaging Manufacturing Program

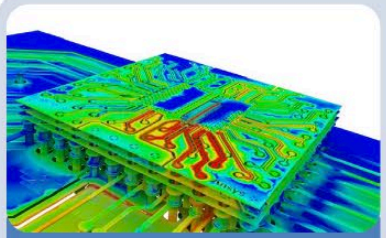
- Strengthen semiconductor advanced test, assembly, and packaging capability in the domestic ecosystem
- Leverage public-private partnerships, that can include support for facilities managed by the NSTC and MUSA
- Broad range of technologies:
  - Heterogeneous integration
  - Wafer and panel-based approaches
  - Tooling and automation
  - Substrate technology

NAPMP Target Areas

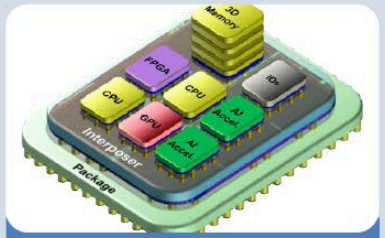
CHIPS for AMERICA

Technology innovation — Create an R&D environment advancing the state-of-the art in advanced packaging.

Ecosystem support — Investments to bolster the growth in domestic capacity and enhance capabilities for competitive edge.

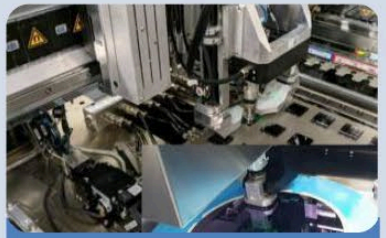


Co-design and simulation

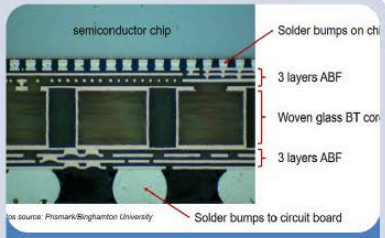


Chiplets

Pilot packaging facilities

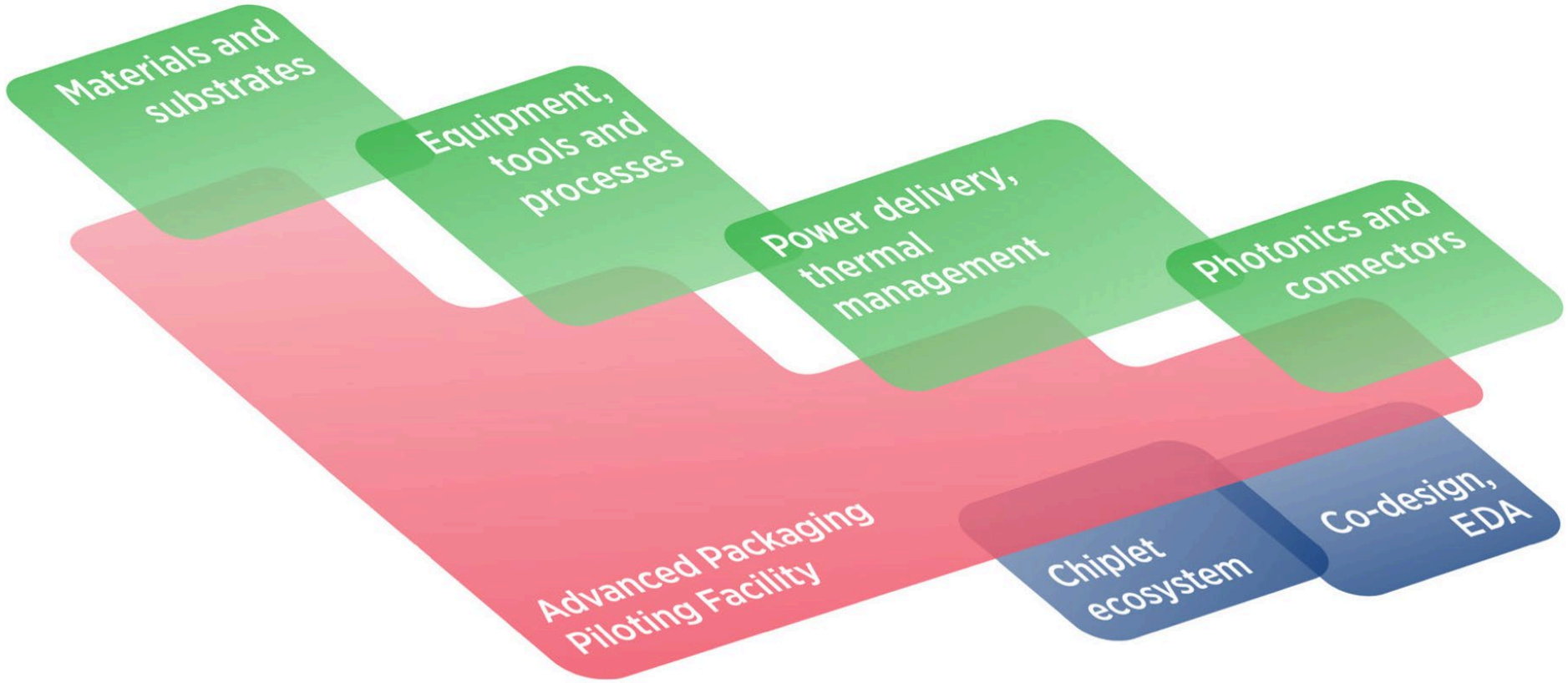


Tooling and automation



Materials and substrates

NAPMP Vision Paper



Technology investments are in green. Ecosystem investments are in blue. The piloting facility, in red, will provide opportunities to validate new technologies for transition to U.S. manufacturing.

https://www.nist.gov/system/files/documents/2023/11/19/NAPMP-Vision-Paper-20231120.pdf

NAPMP News

- On January 31, 2024, the National Advanced Packaging Manufacturing Program (NAPMP) issued a Notice of Intent to announce a competition for new research and development (R&D) activities to establish and accelerate domestic capacity for advanced packaging substrates and substrate materials, a key technology for packaging semiconductors.
- The NAPMP will invest $3 billion in programs that include an advanced packaging piloting facility for validating and transitioning new technologies to U.S. manufacturers, workforce training programs to ensure that new processes and tools are capably staffed, and funding for projects.

https://www.federalregister.gov/documents/2024/02/01/2024-02026/chips-national-advanced-packaging-manufacturing-program-napmp-materials-and-substrates-research-and

RESHAPE

- (Jan-24) The Department of Defense announced today the award of two contracts totaling $49 million to revitalize advanced packaging capabilities and capacity for semiconductors used in defense applications. The awards were made through the Industrial Base Analysis and Sustainment (IBAS) program to Micross Components and the government of Osceola County, Florida.
- (Jan024) SkyWater Florida and Deca Technologies Announce $120M DOD Award to Expand Advanced Packaging Capabilities in Osceola County, Florida

No Substrate Manufacturers Onshore

In Nov 2023, the DoD announced an award of $39.9 million via the DPAI Title III program to **Calumet Electronics Corporation** to "…enhance capabilities to produce High-Density Build-Up (HDBU) substrates, which include High-Density Interconnect Printed Circuit Board (PrCB) cores and HDBU build-up layers."

(Dec-23) The Department of Defense announced an award of $46.2 million to **GreenSource Fabrication**

The award will enhance existing production capabilities at a manufacturing facility of state-of-the-art integrated circuits (IC) substrate, high-density interconnect (HDI) and ultra-high-density interconnect (UHDI), and advanced packaging.

https://www.defense.gov/News/Releases/Release/Article/3624937/dod-awards-462-million-to-revitalize-the-us-defense-industrial-base-on-shoring/

Company	Min. Bump Pitch (µm)	Via/Pad (µm)	Min. Line Width/ Space on Build-up (µm)	Core Via/ Pad (µm)	Max. Build-up Layers (each side)	Max. Core Layers
ACCESS	150	60/95	15/15	-	3	2
AT&S	110	40/-	8/8	-	5	2
Daeduck	110	50/75	8/10	100/200	6	2
Fujitsu Interconnect	112	50/70	12/12	100/200	14	14
Ibiden	90	40/65	7/8	80/180	11	12
Kinsus	130	60/85	9/12	125/225	8	4
Nan Ya PCB	110	55/80	10/10	100/200	10	4
Samsung Electro-Mechanics (SEMCO)	100	49/77	9/12	120/270	7	4
Shinko Electric	90	45/70	8/8	80/180	9	2
Shinko Electric (prototype)	45	38/62	3/3	70/175	10	2
Toppan Printing	130	60/85	9/12	105/200	9	4
Unimicron	90	35/66	8/8	100/190	11	6

https://www.3dincites.com/2024/02/iftle-583-dod-funding-for-u-s-based-substrate-manufacturing/

EU CHIPS Act

https://commission.europa.eu/strategy-and-policy/priorities-2019-2024/europe-fit-digital-age/european-chips-act_en

European Chips Act focuses on five specific areas

- ***Research and Development*:** Calls for further allocations of funds for research and development (R&D) to keep up with global competitors.
  - Further invest €3.3 billion in two current programs: €1.65 billion to the "Horizon Europe" program and €1.65 billion to the "Digital Europe" program.
  - The "Horizon Europe" program focuses on pre-competitive research, development, and innovation in the area of semiconductors
  - "The Digital Europe" program looks to make digital domains and technology widely available for all businesses and the general public to maximize performance in key industries.
- ***"From the lab to the fab":*** Effective translation research into industrial innovation and market-feasible products. Europe must bridge the gap between excellence in laboratory research and onshore manufacturing to sustain leadership in semiconductors and other advanced technologies.
- ***Industry Production*:** Europe is looking to host "first of its kind" facilities through the creation of Integrated Production Facilities, which are factories that design and produce semiconductor components that serve the European market and through Open EU Foundries for chip design, which are facilities that design and produce components for other industrial actors such as medical devices and computer programming.
- ***Local Support*:** Support the workforce development - local skill base and the network of smaller, innovative companies and start-ups as a part of their strategy to grow their semiconductor and high technology ecosystems. The "EU Chips Fund" which will contribute €2 billion to create a more competitive market for semiconductor start-ups to participate in and address skill shortages. Additionally, the Commission wants to help in the retention of employees that have the skills that these start-ups need to be successful and to find industrial partners for these start-ups to collaborate with.
- ***Overhaul the European Supply Chain*:** EU Commission wants to encourage Member States and industry stakeholders to coordinate efforts towards an improved European supply chain for semiconductors.. To enable a rapid response to the current shortages, the Commission has created a list of recommendations to the Member States. Along with streamlining policies of member states, Europe is also looking to build partnerships with the United States and other nations to create a more resilient global semiconductor network.

https://www.csis.org/blogs/perspectives-innovation/european-chips-act-strategy-expand-semiconductor-production

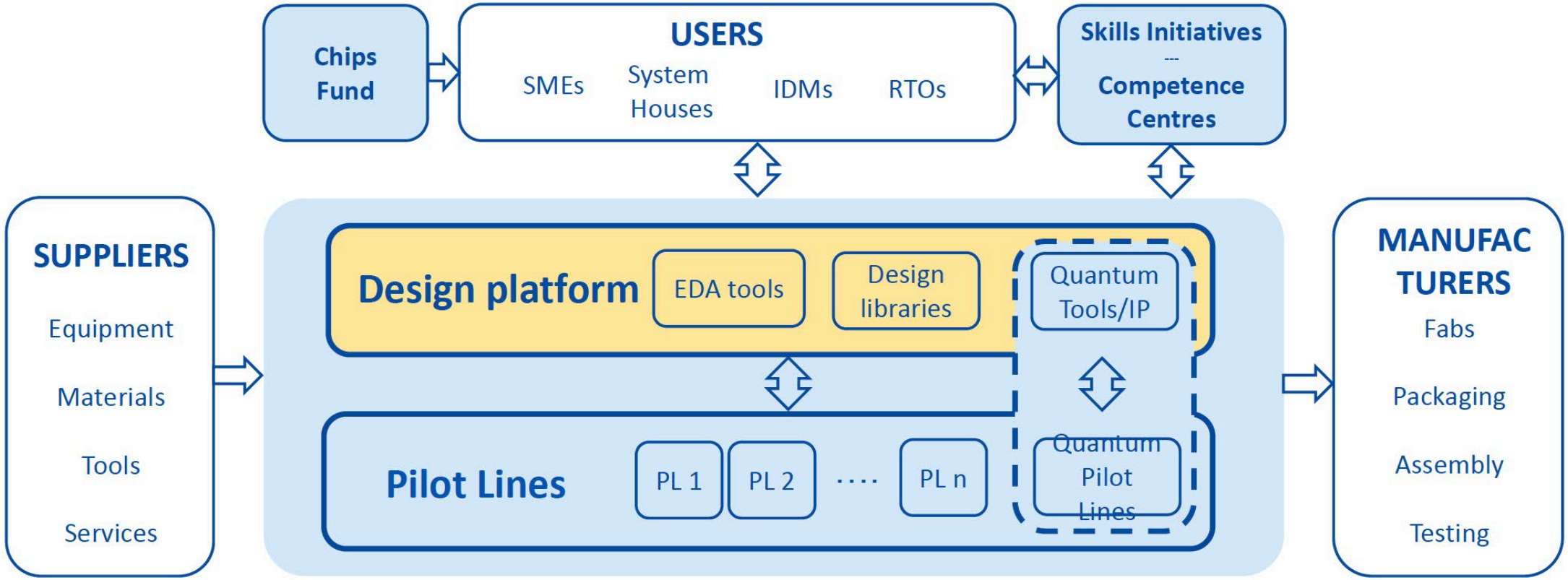
EU CHIPS Act Proposals

- Ministers of European Parament (MEPs) has voted to back the Chips Joint Undertaking proposal, implementing most of the measures put forward under a "Chips for Europe" initiative, as part of the wider Horizon Europe program, the stated aims of which are to support large-scale capacity building through investment in EU-wide research and development infrastructure.
- This will initially pool together about €11 billion ($11.78 billion) drawn from EU central funding, EU countries, and the private sector. The Chips Act aims to eventually unlock €43 billion (£46 billion) in funding for the European semiconductor sector.
- Rapporteur for the Chips Act, MEP Dan Nica said in a statement: "The EU Chips Act should establish Europe as a key player in the global semiconductors arena. Not only does the budget need to be commensurate with the challenges and funded through fresh money, but the EU should lead in research and innovation, have a business-friendly environment, a fast permitting process and invest in a skilled work force for the semiconductor sector."

https://www.theregister.com/2023/02/16/eu_chips_act_bills/

Chips for Europe Initiative

Central role of Design Platform



PILOT LINE 3: PILOT LINE ON ADVANCED PACKAGING AND HETEROGENOUS INTEGRATION

- Offering to Europe a domestic **prototyping option for advanced packaging and heterogenous integration**.
- **Promoting advanced packaging and heterogenous integration technology** and giving to Europe the opportunity to apply it:
  - For advanced communications, enabling a European ecosystem that can support heterogeneous integration to capture higher value in the connectivity market. This is also essential to fulfilling the transition towards the Green Deal objectives through control and forecasting systems.
  - For mobility, enabling autonomous driving, the developed technologies shall provide ways to design and manufacture new environmental sensors, which e.g. simplify and improve object and lane detection, work in difficult weather conditions and situations.
  - For advanced IoT and Edge-AI concepts with minimal form factor, low power consumption and low cost
- Expanding the European technology platform ensuring:
  - **Advanced technology for packaging and heterogenous integration** with the development of relevant demonstrators
  - **Generating intellectual property**.

HETEROGENEOUS INTEGRATION ROADMAP

DoD Microelectronics Commons

https://nstxl.org/opportunity/microelectronics-me-commons/

Lab-to-Fab Transition of Microelectronics Technologies

THE OFFICE OF THE DEPUTY TECHNOLOGY OFFICER FOR CRITICAL TECHNOLOGIES

Research Universities, **Start-ups** have facilities for Lab prototyping but face barriers to demonstrating manufacturability in a Fab.

Core Facilities or Foundries/Fabs provide access to early stage Fab prototyping.

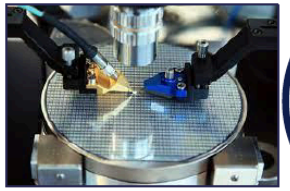
Microelectronics Commons aims to enable lab-to-fab prototyping– evolve microelectronics laboratory prototyping to foundry/fab prototyping – in domestic facilities.

www.slido.com Event Code: #mecdc2022

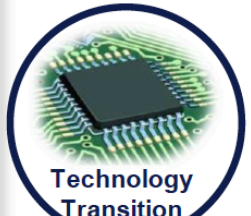
The Microelectronics Commons: Innovation from Lab-to-Fab

Innovation Barriers

- Lack of access to existing fabs for lab-to-fab prototyping
- High capital costs for process and metrology tooling to support manufacturing of microelectronics technologies
- High Intellectual Property (IP) and Electronic Design Automation (EDA) design license costs
- Lack of domestic access to chip carriers, and packaging materials to support integration of electronics
- Lack of workforce talent and expertise to support technology transition



Partnerships



Technology Transition

Workforce Development

End State

- **Sustained partnerships** between emerging technology sources, manufacturing facilities, and interagency partners
- **Rapid transition** of early-stage microelectronics research to proven technology in domestic foundries
- Expand **domestic** microelectronics fabrication capability
- Enhance microelectronics **education** to bolster the microelectronics engineering workforce
- Develop a **pipeline of talent** to bolster local semiconductor economies and grow the domestic semiconductor workforce

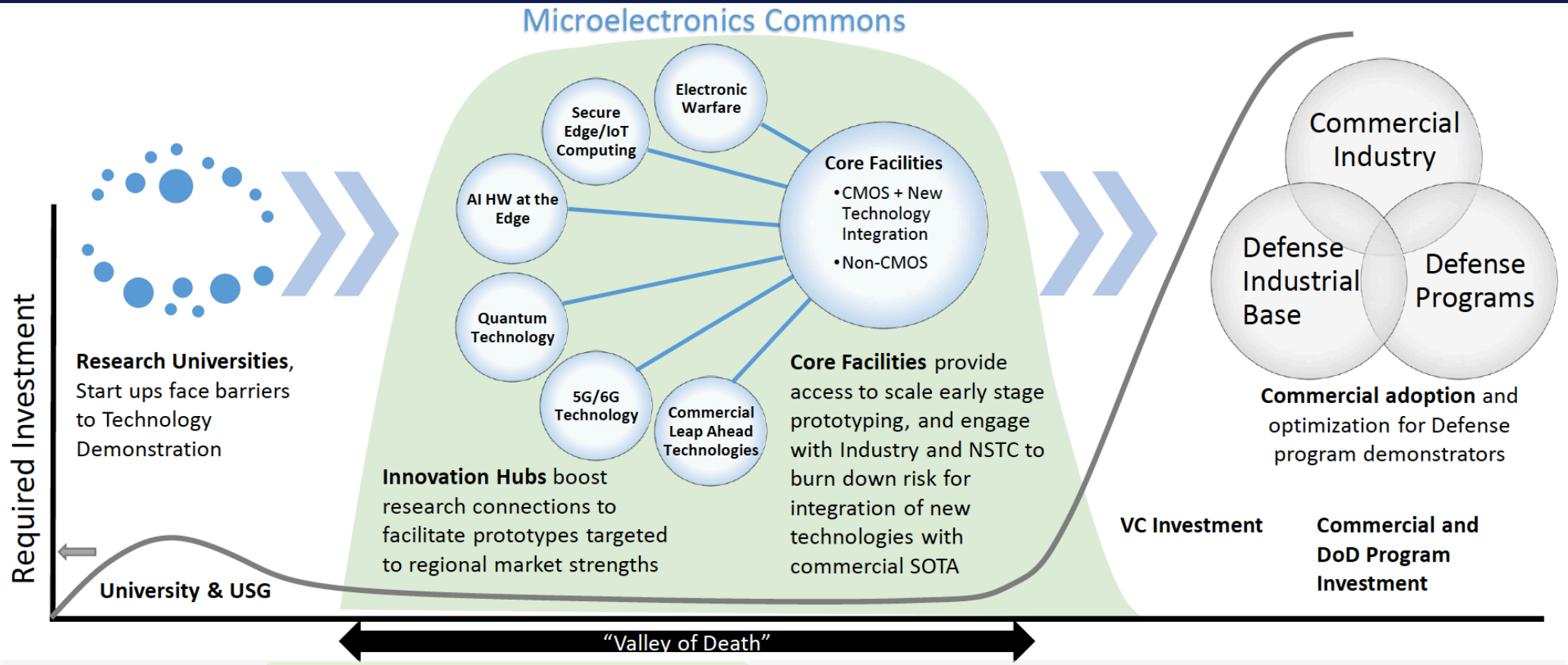
Democratize access to capabilities needed for lab-to-fab prototyping

www.slido.com Event Code: #mecdc2022

DISTRIBUTION STATEMENT A. Approved for Public Release

Microelectronics Commons Addresses the Valley of Death

THE OFFICE OF THE DEPUTY TECHNOLOGY OFFICER FOR CRITICAL TECHNOLOGIES



ME Commons Hubs Awarded

Applied Research Institute Silicon Crossroads Microelectronics Commons (SCMC) Hub	**AZ Board of Regents on behalf of Arizona State University** Southwest Advanced Prototyping (SWAP) Hub	**The Board of Trustees of the Leland Stanford Junior University** California-Pacific-Northwest AI Hardware Hub (Northwest-AI-Hub)	**Massachusetts Technology Collaborative** Northeast Microelectronics Coalition (NEMC) Hub
Midwest Microelectronics Consortium The Midwest Microelectronics Consortium (MMEC)	**North Carolina State University** Commercial Leap Ahead for Wide-bandgap Semiconductors (CLAWS)	**The Research Foundation for The State University of New York (SUNY), on behalf of The SUNY Center for Economic Development** Northeast Regional Defense Technology Hub (NORDTECH)	**University of Southern California** California Defense Ready Electronics and Microdevices Superhub (California DREAMS)

https://microelectronicscommons.org

HETEROGENEOUS INTEGRATION ROADMAP

OSD/Crane State-of-the-Art Heterogeneous Integration Packaging (SHIP), STEAM PIPE and STAMP

IEEE | IEEE photonics Society | semi | IEEE ELECTRONICS PACKAGING SOCIETY | ASME | ELECTRON DEVICES SOCIETY

State-of-the-Art Heterogenous Integrated Packaging (SHIP) Program

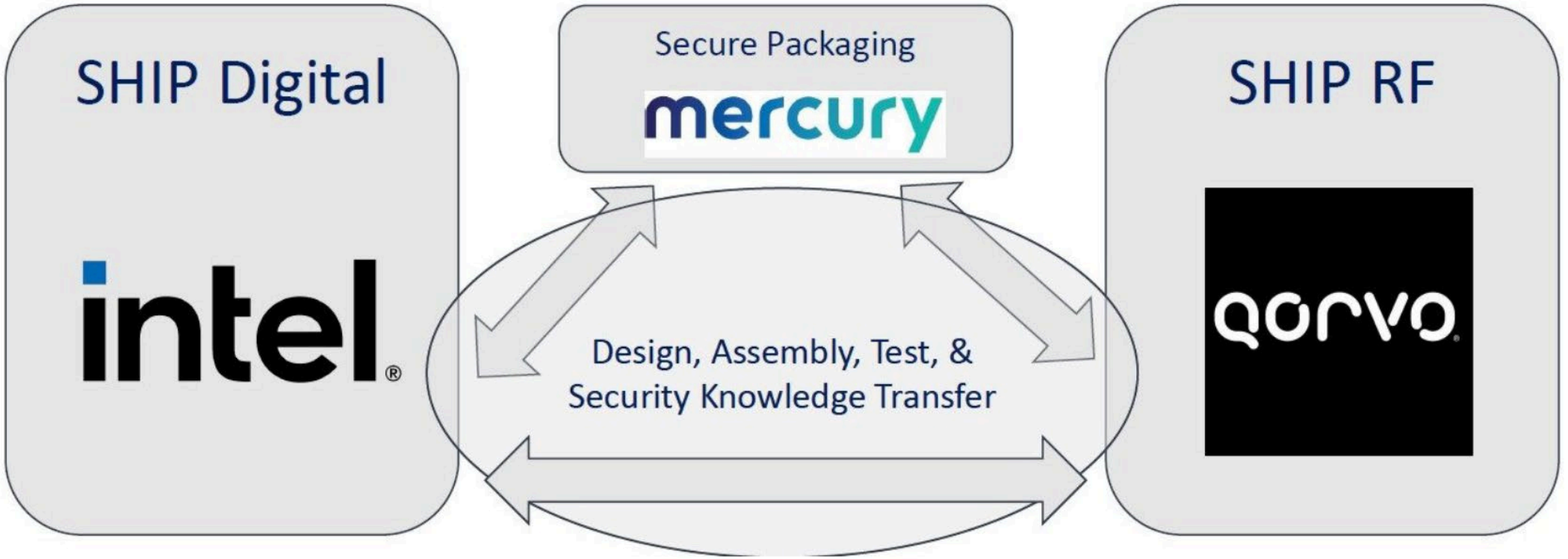


Figure 1: The DoD's SHIP Program.

OSD SHIP Program (Dr. Darren Crum)

- SHIP Program Manager: Dr. Darren Crum
  - Develop an economically viable, SOTA heterogeneous integration and packaging capability for DoD system performance enhancement and assurance/security applications, which currently do not exist.
  - Provide sustainable, quantifiably assured SOTA advanced packaging access to the DoD and defense industrial base (DIB).
- The SHIP program specifically addresses both digital and RF packaging technologies through the program leads Intel and Qorvo, respectively.
- The key focus of the SHIP digital program includes:
  - Multichip packaging products utilizing Intel's commercial packaging, assembly, and test
  - Create a catalog of available designs, die, chiplets, package types etc.
  - Reuse and standardization
  - Creation of demonstrators that use the SOTA technology
  - **Adoption and use in military systems (transition the technology into actual products)**

The key focus of the SHIP Rf program led by Qorvo includes:

- Design, packaging, and assembly as an onshore service
- Reshoring mature manufacturing, assembly, and test such as the high-volume flip-chip capability
- Enable access to advanced Rf packages by providing a full suite of design tools, advanced packaging platforms, and a wide selection of materials choices
- **Allow DoD and DIB access to this commercial design flow through PDKs and ADK to design custom devices**

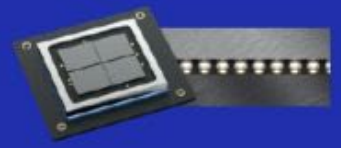
Intel – SHIP Digital (John Sotir)

Embedded Multi-die Interconnect (EMIB)

bump pitch ≤ **55 microns**

- leads industry
- first 2.5D embedded bridge solution
- products shipping since 2017

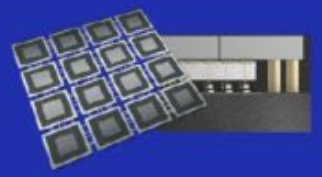
Foveros Technology



bump pitch **50-36 microns**

- wafer-level packaging capabilities
- first-of-its-kind 3D stacking solution

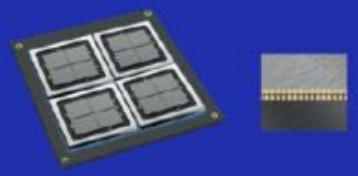
Foveros Omni



bump pitch **~25 microns**

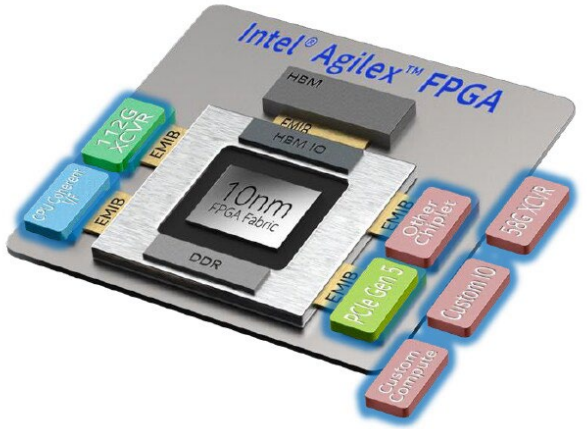
- next gen Foveros technology
- unbounded flexibility with performance 3D stacking technology for die-to-die interconnect and modular designs

Foveros Direct



bump pitch **< 10 microns**

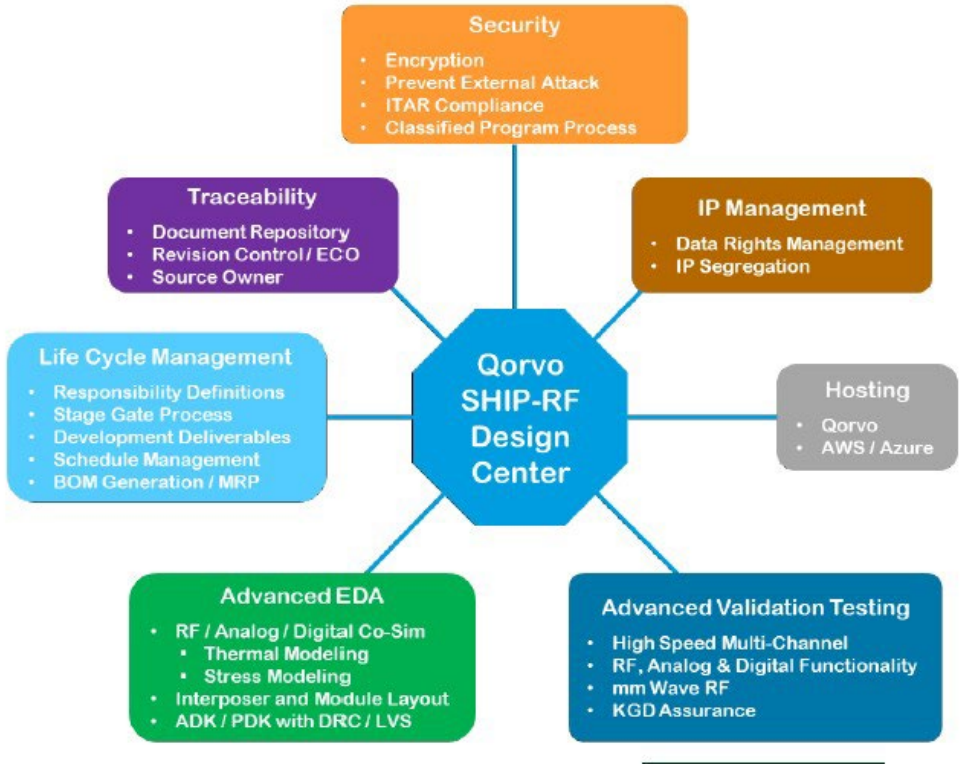
- direct copper-to-copper bonding for low resistance interconnects
- blurs the boundary between where the wafer ends and the package begins

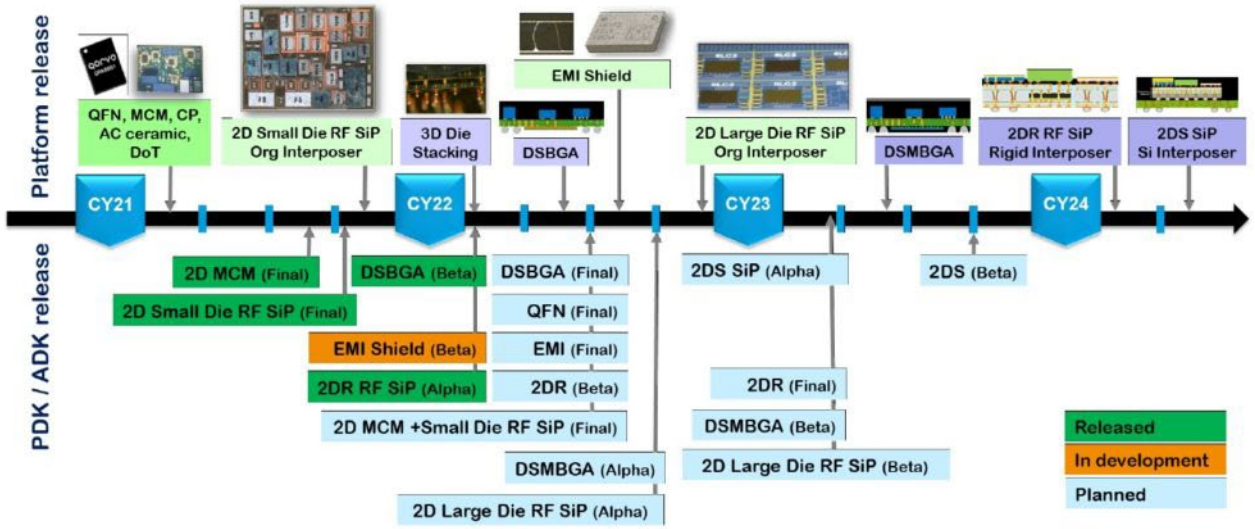


https://www.3dincites.com/2022/06/iftle-524-imaps-examines-the-dept-of-defense-ship-program/

Qorvo – SHIP RF (Ted Jones)

- The Qorvo ATC will be a US-based assembly and test factory offering access to SOTA manufacturing technologies at commercially competitive pricing. It will be based on Qorvo-proven commercial SOTA packaging technologies running at high volume manufacturing (HVM) rates offshore.





https://www.3dincites.com/2022/06/iftle-524-imaps-examines-the-dept-of-defense-ship-program/

Stimulating Transition for Advanced Microelectronics Packaging (STAMP)

- Leveraging alignment to existing DoD Programs to transition the MCP technology to a program of record system. Advantages for military system developers and integrators include:
- Access to processing devices specifically designed in collaboration with DoD to meet DoD computing needs
- Access to next-generation at-the-edge sensor computing designed in collaboration DoD
- SOTA technologies will provide your systems with cutting-edge technology improvements – dramatically accelerating your technology roadmap of processing/computing devices with significantly reduced SWAP and increased performance

https://nstxl.org/opportunity/stimulating-transition-for-advanced-microelectronics-packaging-stamp/

Stimulating Transition for Advanced Microelectronics Packaging (STAMP)

SHIP MCPs 1 and 2

Multi-chip package (MCP)

- MCPs 1 and 2 contain SOTA chiplets with advanced functionality, low power, smaller size, and cutting-edge performance along with Intel® Agilex™ advanced Field Programmable Gate Array (FPGA) technology
- The chiplets are Intel A-Tile Direct RF data converter tiles and Intel F-Tile advanced Serial/Deserial tiles
- These chiplets are connected to Intel® Agilex™ FPGAs with SOTA low power, low latency, Enhanced Multi-Die Interconnect Bridge (EMIB) parallel bus interconnect technology offered by Intel

MCP-1: Belmont Bay

Lead DIB Partner: BAE Systems
Use Case: Small Form Factor EW System
Expected SWaP Savings: 8x
Product Release: Expected April 2023

MCP-2: Laguna Bay

Lead DIB Partner: Lockheed Martin
Use Case: EW System
Expected SWaP Savings: 8x
Product Release: Expected December 2023

https://nstxl.org/opportunity/stimulating-transition-for-advanced-microelectronics-packaging-stamp/

Strategic Transition of Microelectronics to Accelerate Modernization by Prototyping and Innovating in the Packaging Ecosystem (STEAM PIPE)

HETEROGENEOUS INTEGRATION ROADMAP

Motivation

- Support the SHIP program goals to develop a US-based SOTA packaging capability for the DoD
- Enable system performance enhancement through the development of advanced prototypes and transition to military systems
- Emphasize transition strategy

Requirements

- Credible strategy to transition, including productization, qualification, and use
- Encouraged use of cost sharing and teaming
- Finalized third-party IP agreements, subcontracts, and purchase agreements according to originally proposed timeline
- Advanced packaging technologies and processes with a clear path to support DoD volume production

Current SHIP performer (Intel, Qorvo, Mercury) processes and products are not required.

STEAM PIPE can award prototypes with different product and process access models

Model 1	Model 2	Model 3
New devices and/or processes that will be made available across the DIB.	New capability of packaging technology or process made available to the DIB. Demonstrator devices may not be made available.	Devices that may be shared on a case-by-case basis with certain DIB members. If the prototype and process will not be shared with the entire DIB, a significant cost share is required.

https://nstxl.org/opportunity/strategic-transition-of-microelectronics-to-accelerate-modernization-by-prototyping-and-innovating-in-the-packaging-ecosystem-steampipe/

https://www.3dincites.com/2023/02/iftle-548-tsmcs-off-shore-production-steam-pipe/

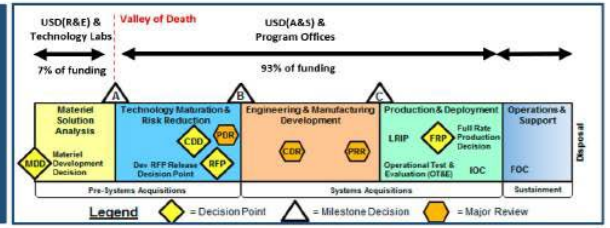
https://www.3dincites.com/2023/02/iftle-548-tsmcs-off-shore-production-steam-pipe/

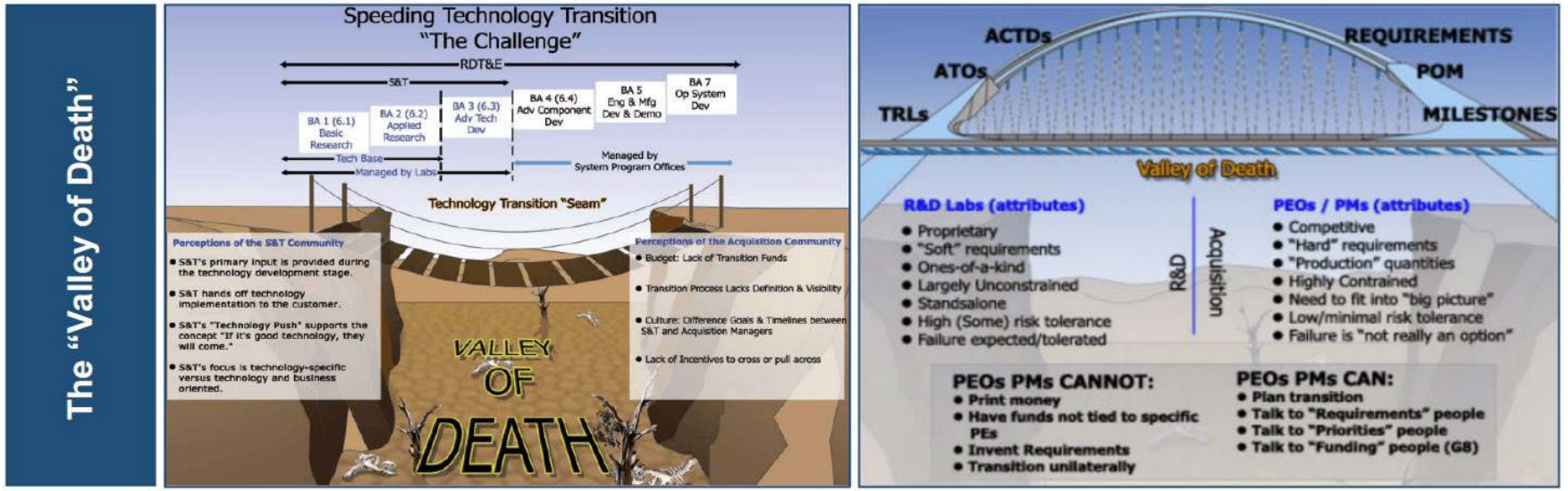
STAMP Objectives: Bridging the Technology Valley of Death

Transition Challenges

> "I think transition is clearly one of our biggest problems. The so-called 'Valley of Death,' scaling up to fielding and full-scale production is a piece of that. There are many places you can fall off the cliff in transition for the Defense Department."

Kathleen Hicks
Deputy Defense Secretary



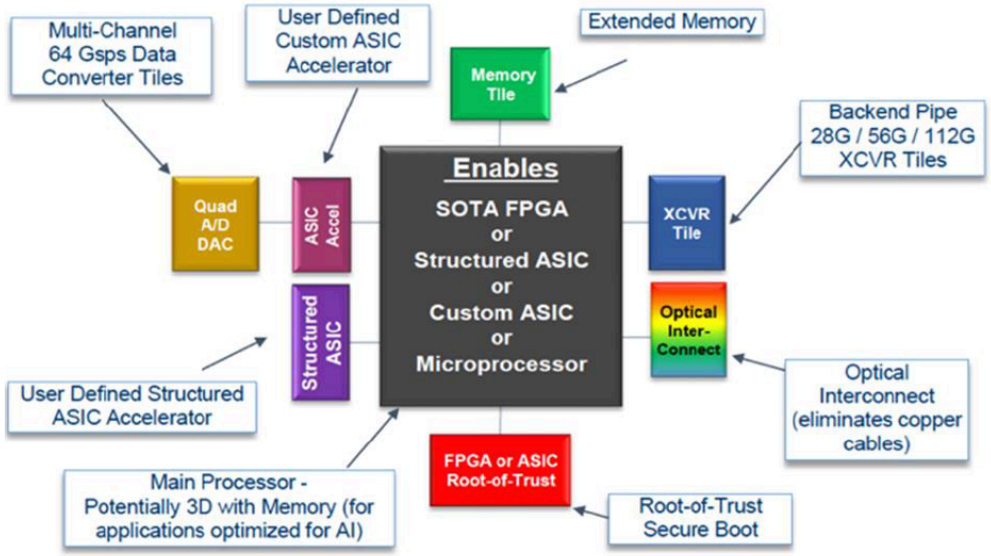


DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited 6

https://nstxl.org/opportunity/stimulating-transition-for-advanced-microelectronics-packaging-stamp/

Goals and Intended Outcomes

- New heterogeneously integrated packaged prototypes that achieve less power consumption and latency, reduced physical size, and improved system performance and reliability than current packaging methods.
- Address technology adoption risks and barriers resulting in follow-on Government sponsor funding.
- Unique and secure design tools and IP for multi-die heterogeneous integration of SOTA microelectronics.
- Strengthen the domestic advanced packaging ecosystem through the maturation of manufacturing processes and addition of SOTA devices.



Potential configurations for HI-enabled SOTA devices

https://nstxl.org/opportunity/strategic-transition-of-microelectronics-to-accelerate-modernization-by-prototyping-and-innovating-in-the-packaging-ecosystem-steampipe/

STEAM PIPE 2024 RFS Released

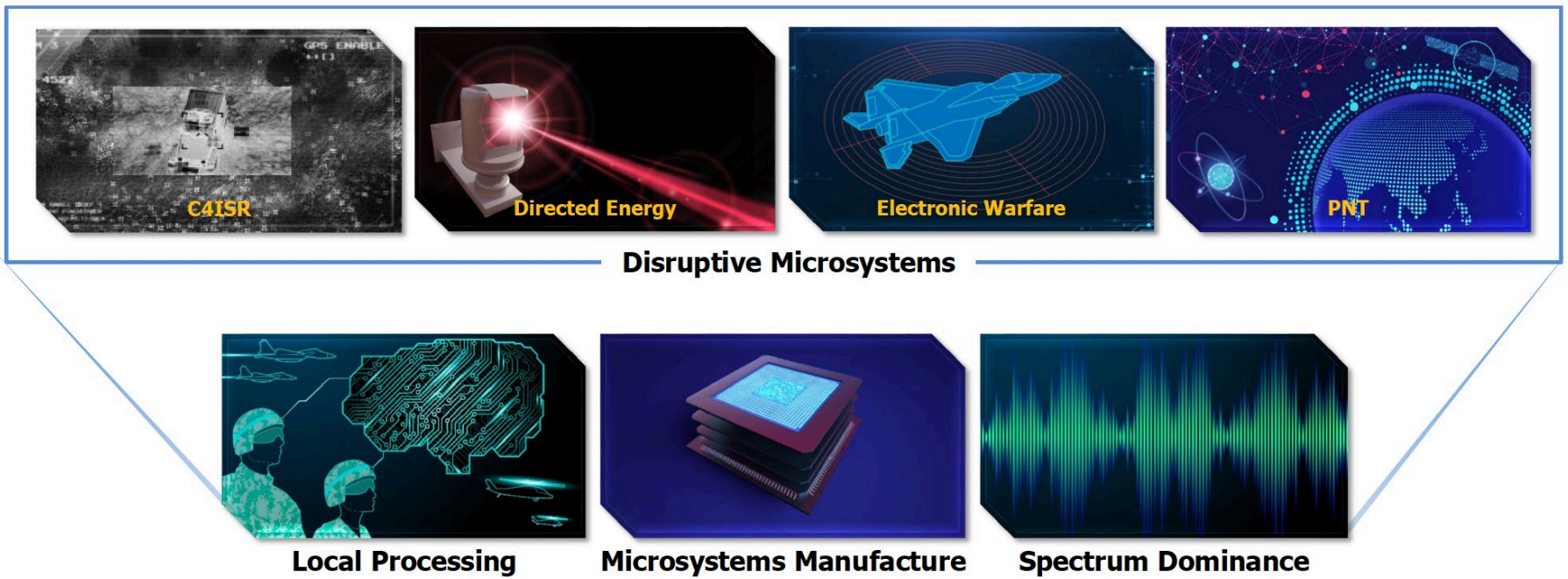
- As to the next iteration to STEAM PIPE, the Office of the Undersecretary of Defense, Research & Engineering (OUSD(R&E))'s Trusted & Assured Microelectronics program is seeking advanced packaging prototype devices that will 1) transition into a targeted military system and 2) be made available to the Defense Industrial Base (DIB) for broad use in military systems.
- Chiplet Prototyping
- Packaged Device Prototype Development
- Transition

https://nstxl.org/opportunity/steam-pipe-24/

DARPA

MTO
MICROSYSTEMS TECHNOLOGY OFFICE

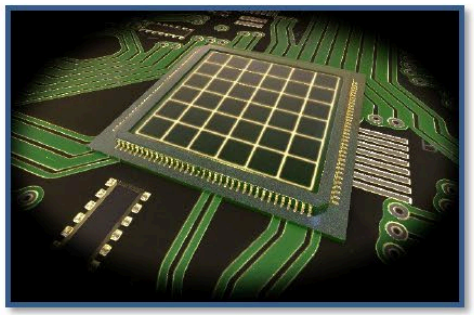
High-performance, intelligent microsystems and next-generation components



C4ISR: Command, Control, Communications, Computers, Intelligence, Surveillance, and Reconnaissance
PNT: Positioning, Navigation, and Timing

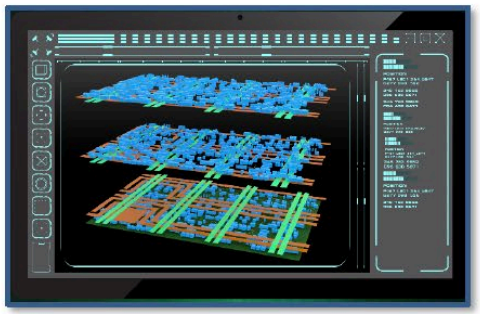
Microsystems Manufacture: Key challenges

Realizing heterogeneous 3D electronics



2D electronic interconnects limit throughput, functionality, miniaturization, and efficiency

Optimizing design and test for complex circuits and prototypes

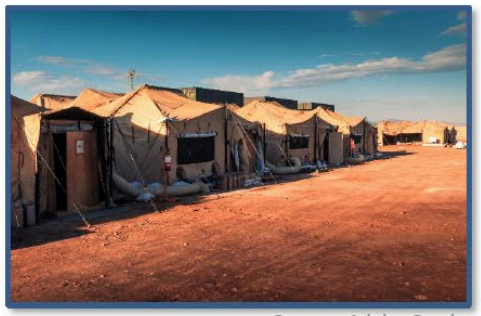


Increasingly complex circuits and assembly stretch the limits of current design, packaging, and test capabilities

Overcoming security threats across the entire hardware lifecycle

Persistent hardware threats limit the ability to access and utilize advanced electronics technology

Developing electronics for extreme environments



Source: Adobe Stock

Electronics performance and reliability are limited by extreme temperature, voltage, current, and radiation

2D: Two Dimensional
3D: Three Dimensional

https://www.darpa.mil/work-with-us/opportunities

Electronics Resurgence Initiative (ERI) 2.0 plan

HETEROGENEOUS INTEGRATION ROADMAP

Create national capability

NGMM

Source: Adobe Stock

New research focus

Manufacturing complex 3D microsystems

Source: Advanced Technology Services, Inc.

Developing electronics for extreme environments

Source: Adobe Stock

Today

ERI 2.0 Enhancement

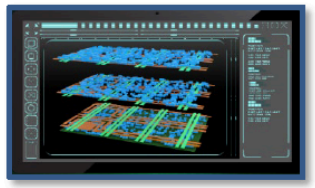
FY22 | FY23 | FY24 | FY25 | FY26 | FY27

Original ERI funding

ERI 2.0 Baseline

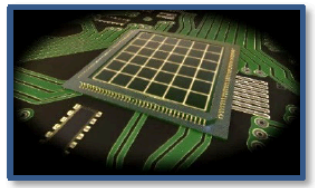
Maintain research base

Overcoming security threats across the entire hardware lifecycle



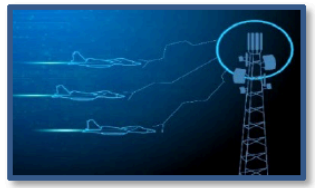
Optimizing design and test for complex circuits and prototypes

Increasing information processing density and efficiency



Realizing heterogeneous 3D electronics

Accelerating innovation in artificial intelligence hardware to make decisions at the edge faster



Securing communications

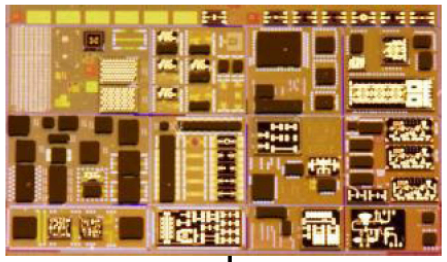
Source: Adobe Stock

NGMM: Next-Generation Microelectronics Manufacturing program

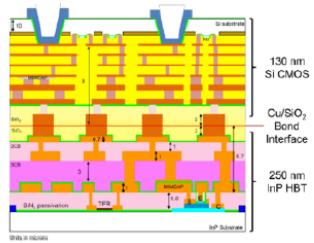
https://www.darpa.mil/work-with-us/opportunities

Heterogeneous Integration Evolution

DAHI (2.5D)



Source: DARPA

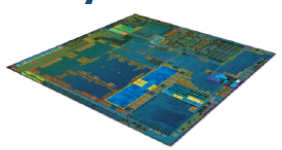


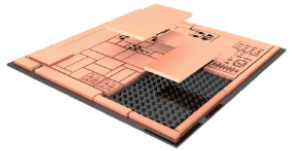
Source: Teledyne, DARPA DAHI

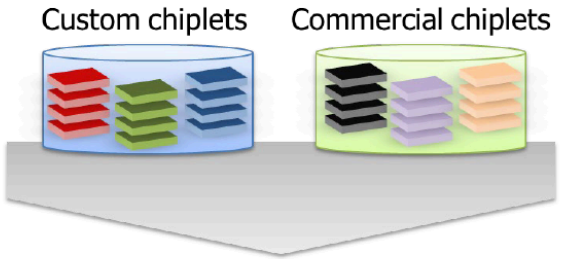
DAHI (3D)

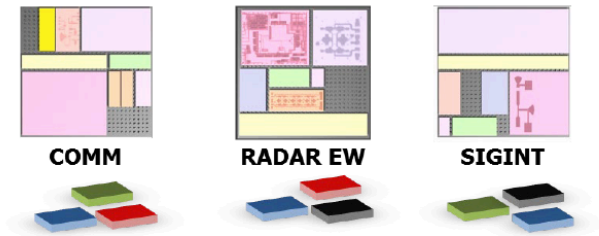
CHIPS (2.5D)

Today – Monolithic Tomorrow – Modular



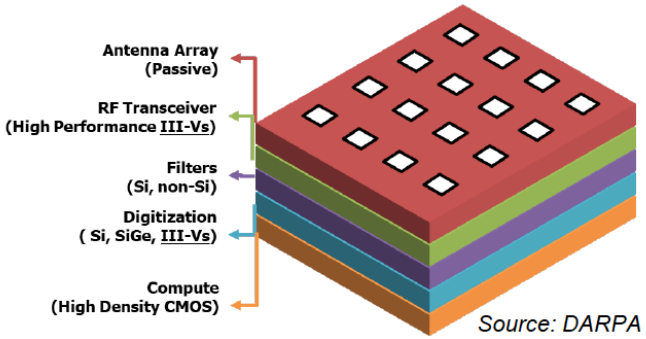






Source: DARPA CHIPS BAA

3DHI



Source: DARPA

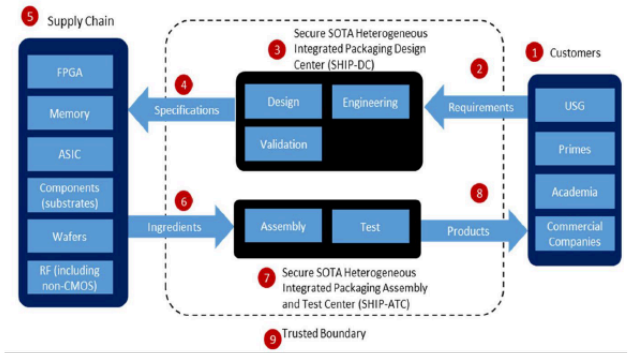
'Modular' stacking of heterogeneous technologies/functions allows tailoring for different applications

3D Heterogeneous Integration Provides a Path to Enhanced Performance, Increased Functional Density, Lower Size and Cost

https://www.darpa.mil/work-with-us/opportunities

Can it be Manufactured

OSD SHIP (2.5D)



Notional design and prototype manufacturing flow for delivering secure and SOTA packaging meeting the needs of defense and aerospace applications.

Source: OSD SHIP RFS

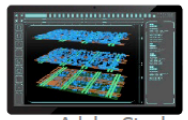
Sustainable, quantifiably assured SOTA advanced packaging for DoD and defense industrial base

NGMM (3D)

(Next Generation Microelectronics Manufacturing)

Manufacturing process

Source: SUSS



3DHI assembly design kit

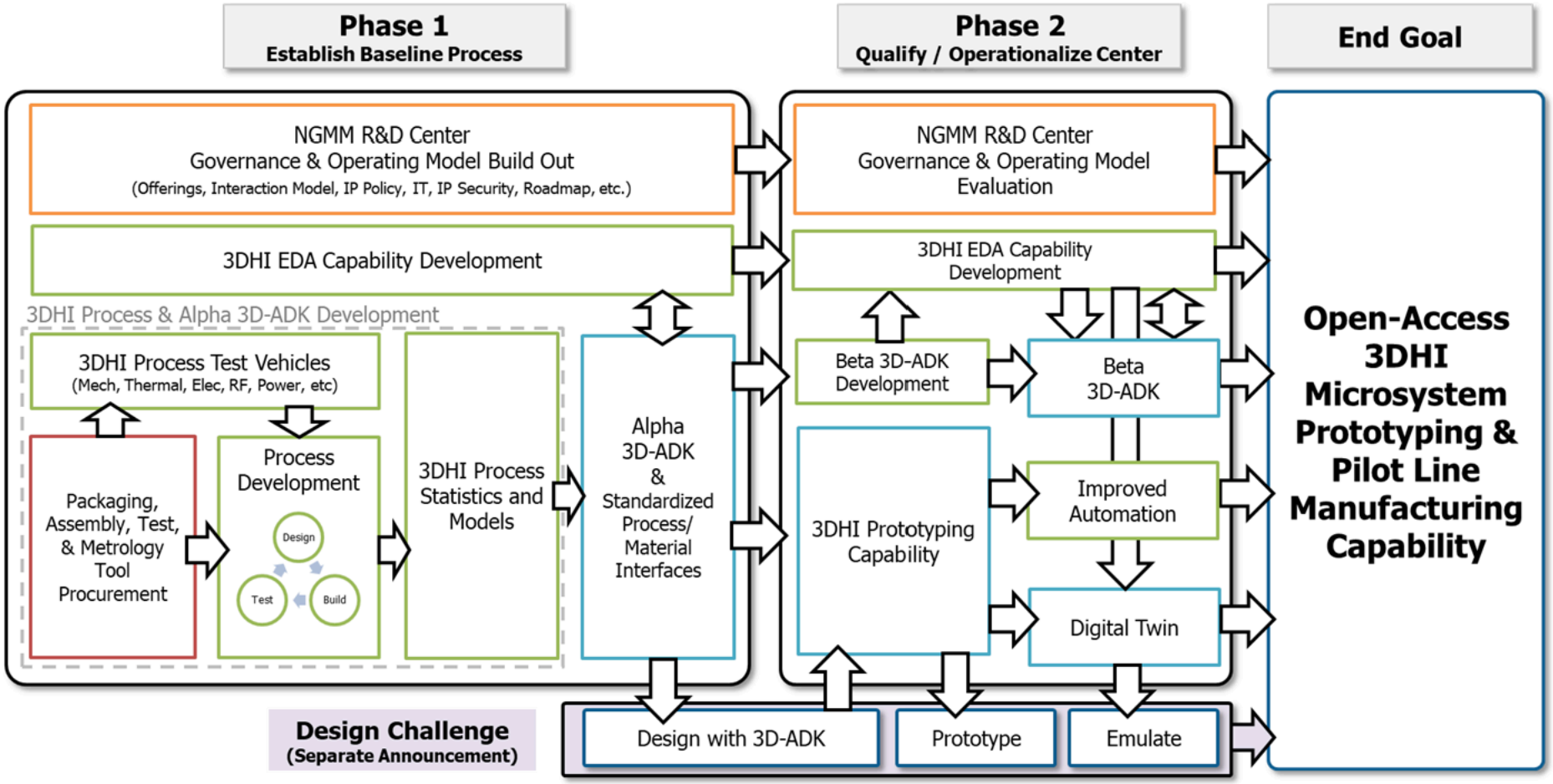
Source: Adobe Stock

National facility

3DHI R&D and low-volume manufacturing

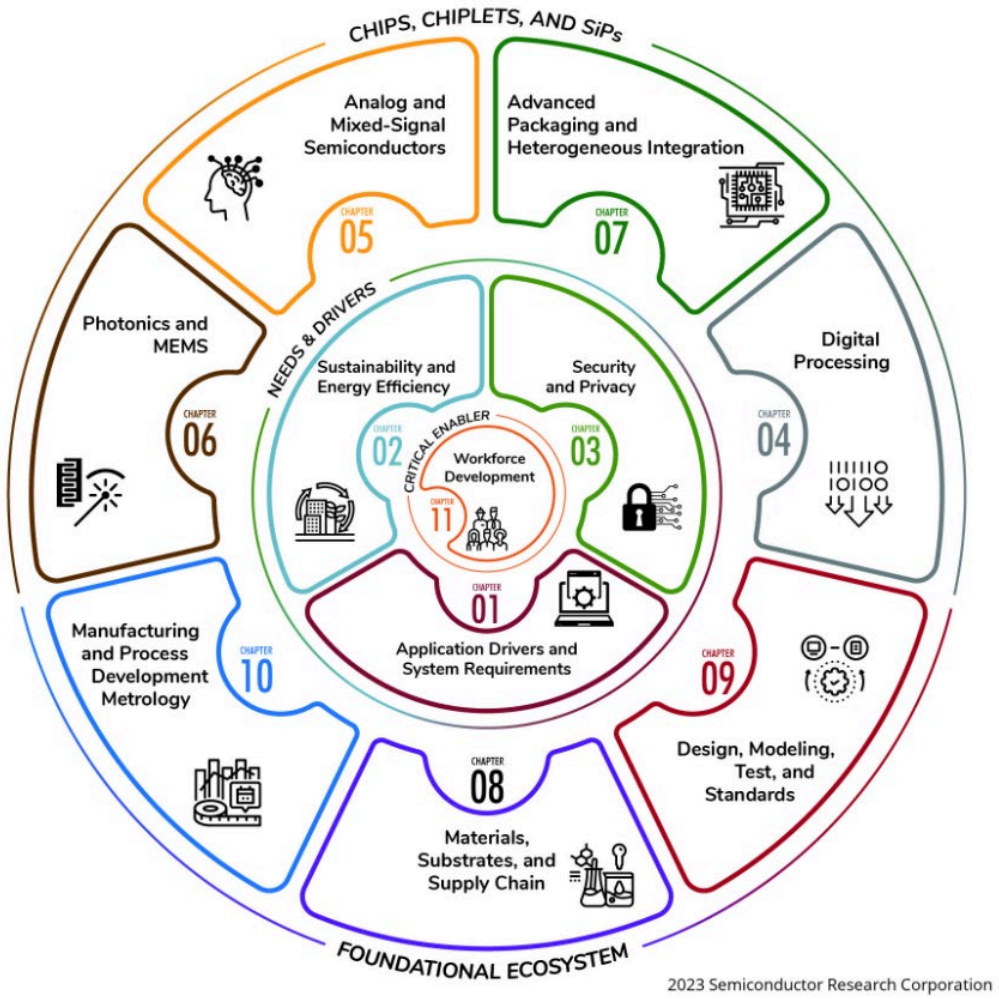
https://www.darpa.mil/work-with-us/opportunities

DARPA NGMM Program Structure



https://sam.gov/opp/dfdbe8ad7dfe4c27946b2220d64691dc/view

SRC MAPT Roadmap Released



https://srcmapt.org

Next Steps

- Monitor on-going and new programs
  - CHIPS Act appropriations and NIST White Paper
  - National Advanced Packaging Manufacturing Program
  - DoD / OSD
  - DARPA
  - EU CHIPS Act
- Expand coverage for other activities
  - Bring HIR members into discussion for their perspectives
  - MAPT Roadmap
    - https://www.src.org/about/nist-mapt-roadmap/
  - UCLA/SEMI Roadmap
    - https://samueli.ucla.edu/ucla-chips-and-semi-win-300k-in-nist-funding-to-create-heterogeneous-integration-roadmap/
  - EU CHIPS Act
    - https://commission.europa.eu/strategy-and-policy/priorities-2019-2024/europe-fit-digital-age/european-chips-act_en

HETEROGENEOUS INTEGRATION ROADMAP

Thank You!

https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html