HIR-Ch.21 – TWG „SiP and Module“

Heterogeneous Integration Roadmap (HIR) Spring Meeting 2024, San Jose

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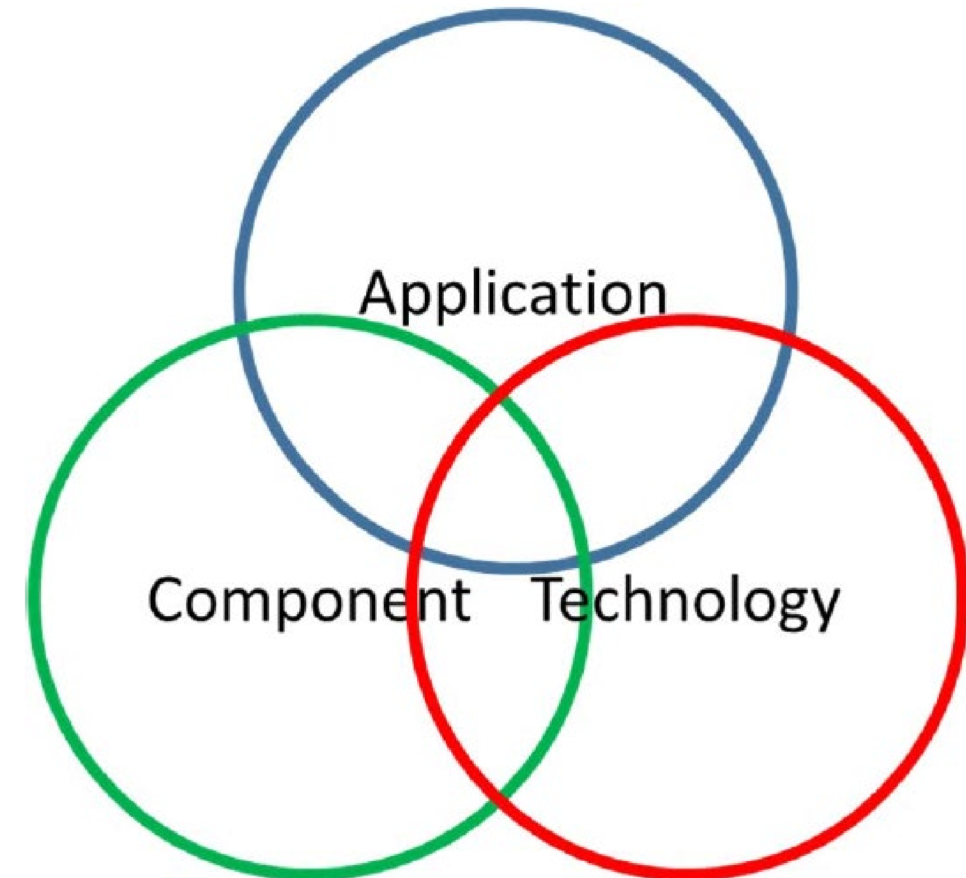
Outline

Definitions and Classification

Toolbox for SiP

Challenges

Outlook



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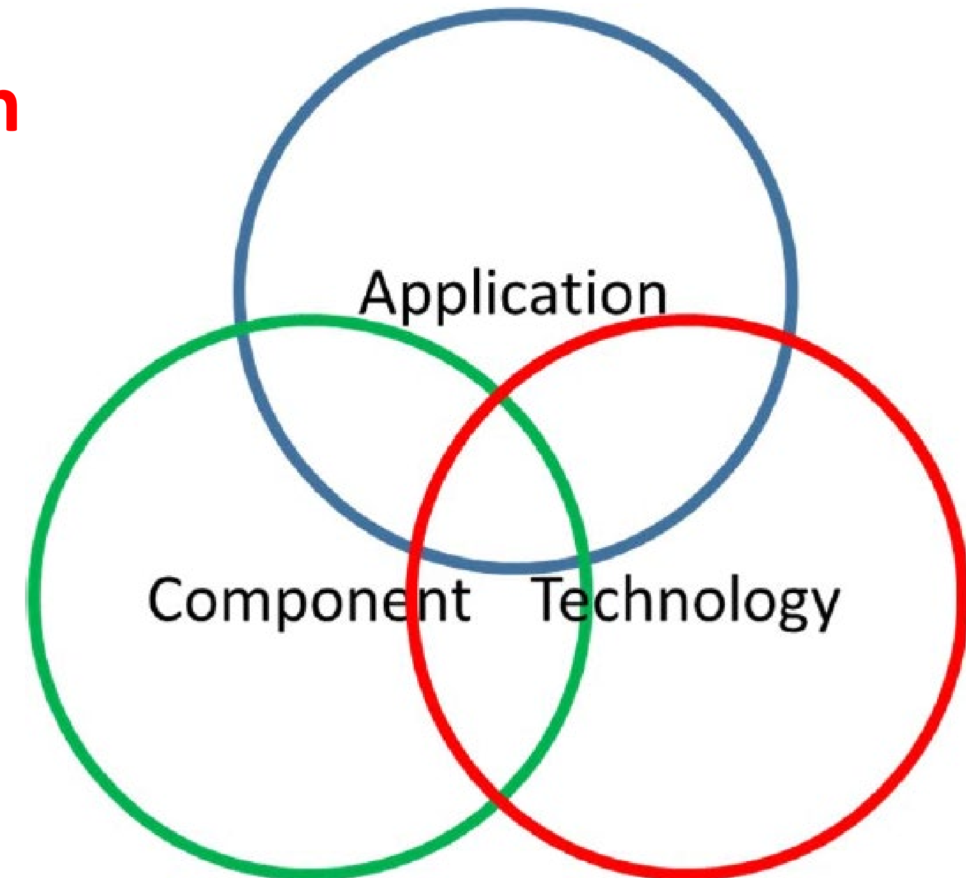
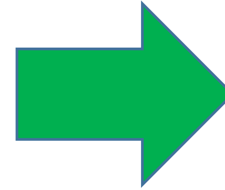
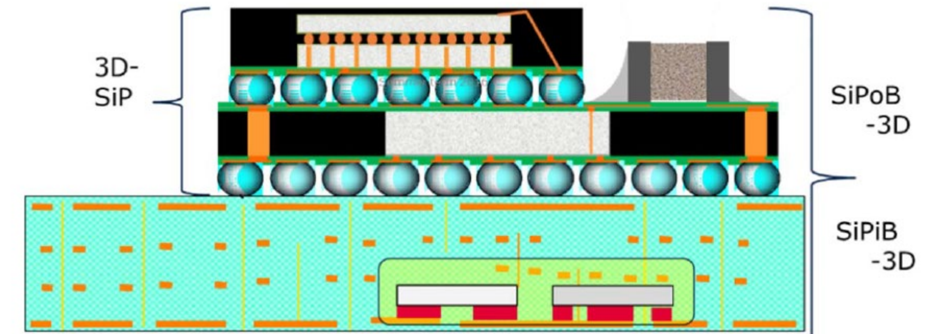
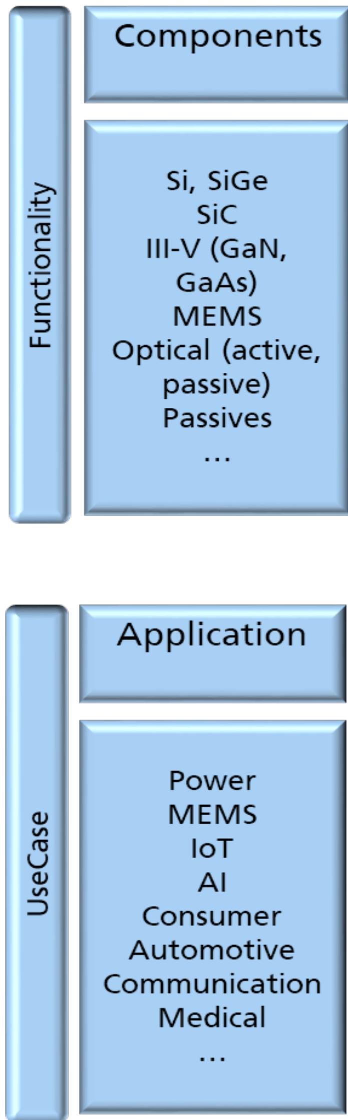






Definition of SiP

"SiP, or System-in-Package, refers to a package (such as SO, QFP, BGA, CSP,LGA) that has multiple die (Si, GaAs, SiGe, and or SOI) plus optional passives integrated together. The package is typically surface mounted to the main board."



Interconnecting Functions

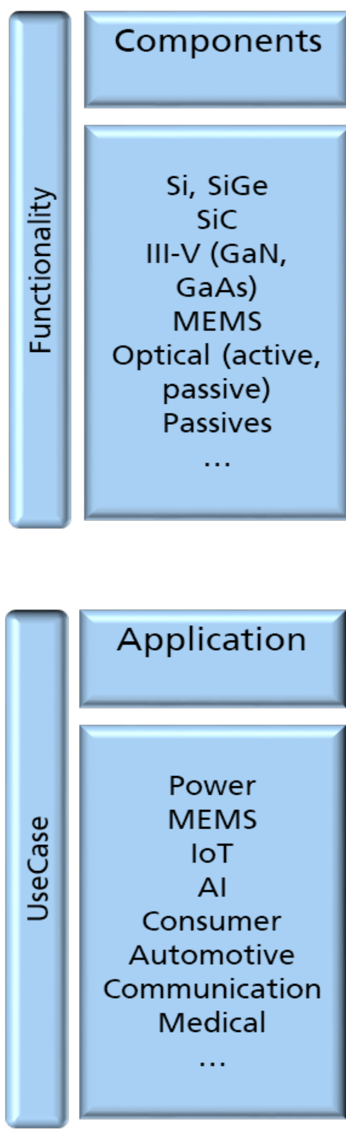
Material Focus

Architecture

Geometry and Footprint

Interconnect Vertical	Interconnect Horizontal	Encapsulation	Packaging Concept	Package Type	
Wirebond FlipChip TxV SolderBalls HybridBond	RDL Wirebond	Liquid (UF, GT, Mold) Powder (Mold) Laminate Print. Materials	Side by side 2.5 D 3D (3DIC, PoP) Fan Out xLP Embedding (WLP type, ECP type) 3D Printed Package …	BGA SO QFP LGA Folded Flex ECP eWLP …	Module, Functional Substrate w/ Battery, Display, Lens, …

Packaging Toolbox



Interconnecting Functions
Material Focus
Architecture
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Packaging Toolbox

DESIGN / STCO

Outline

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Toolbox for SiP

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SiP
ADVANCED SYSTEM IN PACKAGE TECHNOLOGY
VIRTUAL CONFERENCE

HIR
HETEROGENEOUS INTEGRATION ROADMAP

iMAPS International Microelectronics Assembly & Packaging Society

Interconnecting Functions

Interconnect
Vertical | Horizontal

Wirebond
FlipChip
TxV
SolderBalls
HybridBond

RDL
Wirebond

Material Focus

Encapsulation

Liquid (UF, GT, Mold)
Powder (Mold)
Laminate
Print. Materials

Architecture

Packaging Concept

Side by side
2.5 D
3D (3DIC, PoP)
Fan Out xLP
Embedding (WLP type, ECP type)
3D Printed Package
...

Geometry and Footprint

Package Type

BGA
SO
QFP
LGA
Folded Flex
ECP
eWLP
...

Module, Functional Substrate

w/ Battery, Display, Lens,
...

Packaging Toolbox

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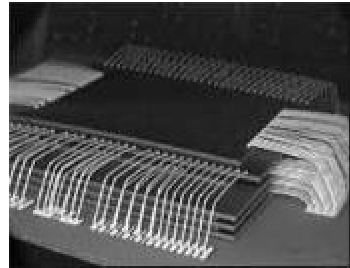
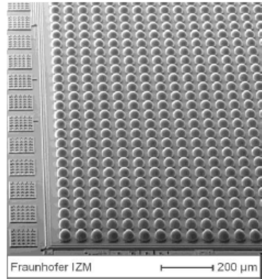
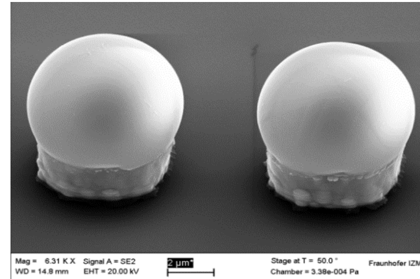
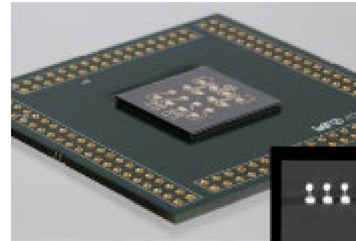
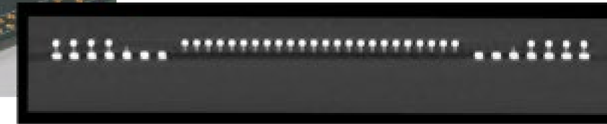
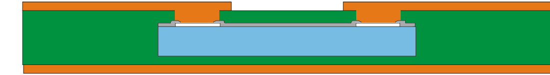
SiP Packaging Toolbox: *Interconnect*



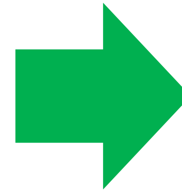




Evolution of standard interconnect

- *Wirebond* and stacked wirebonds incl. copper wire
- *Flip Chips* and stacked flip chips (w/ TSV)
- Package on Package (PoP) bump bonding

Challenges

- More IO/area, size of microbumps
- Thin chips for thinner stacks
- Warp and I/O arrangement for *More than Moore* SiP



New: Embedding Technology – *Interconnect by Electroplating*

- Embedding of thin active chips into the dielectric layers
- Embedding of passive components together with chips
- Embedding of SMD components for low volume and SME´s

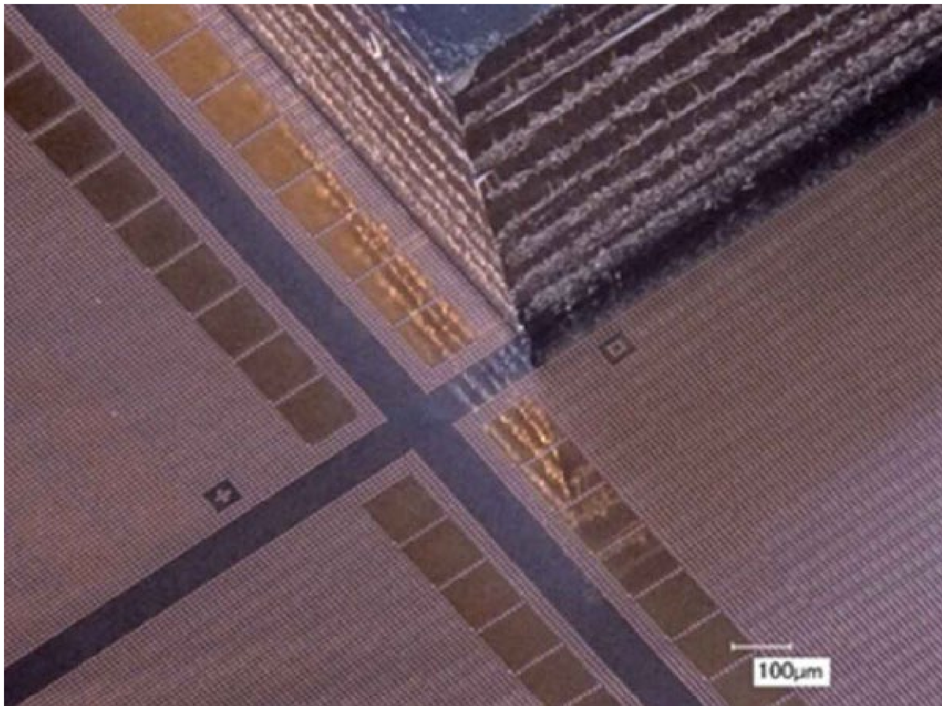
Challenges:

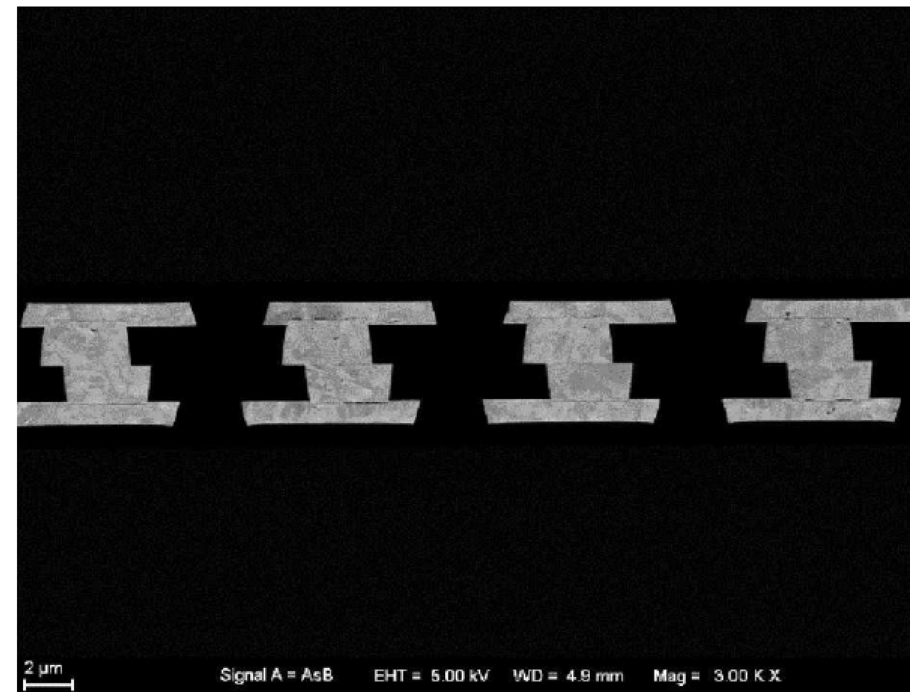
- Remaining dielectric thickness decreasing
- Lines/spaces and via Ø @ HDI substrates, by shrinking the chip pitch
- Multi material challenge (Si, dielectric, EMC, underfill, die attach …)

SiP Packaging Toolbox: *Interconnect*

SIP is also benefitting from processes stemming from other areas of technology:

Hybrid bonding



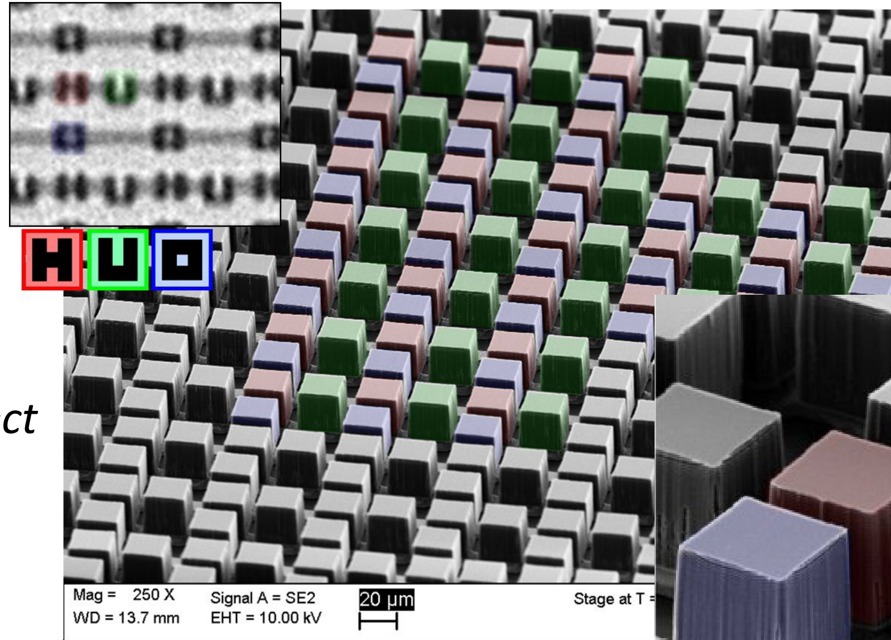


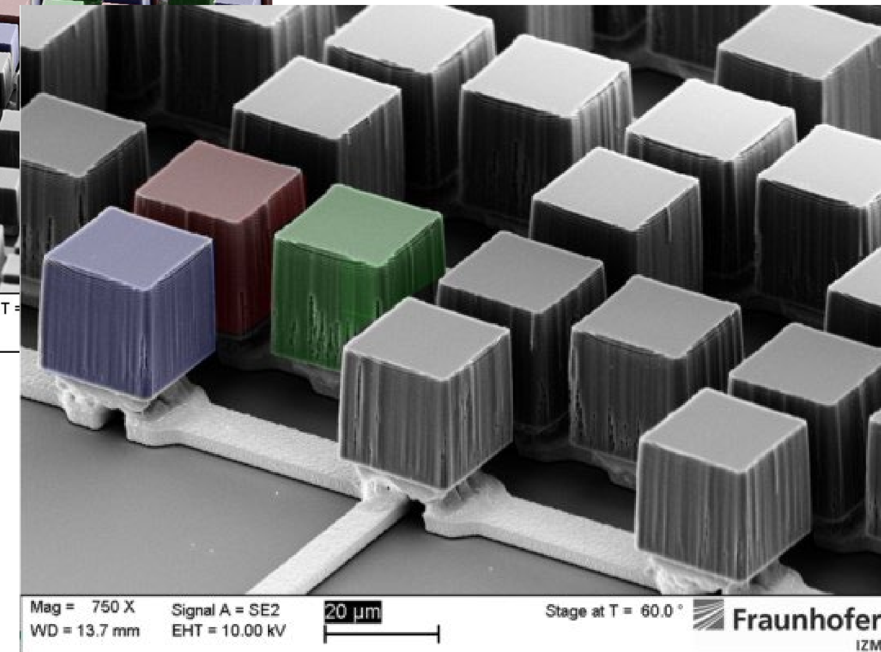
SiP Packaging Toolbox: *Interconnect*

SIP is also benefitting from processes stemming from other areas of technology:

Hybrid bonding

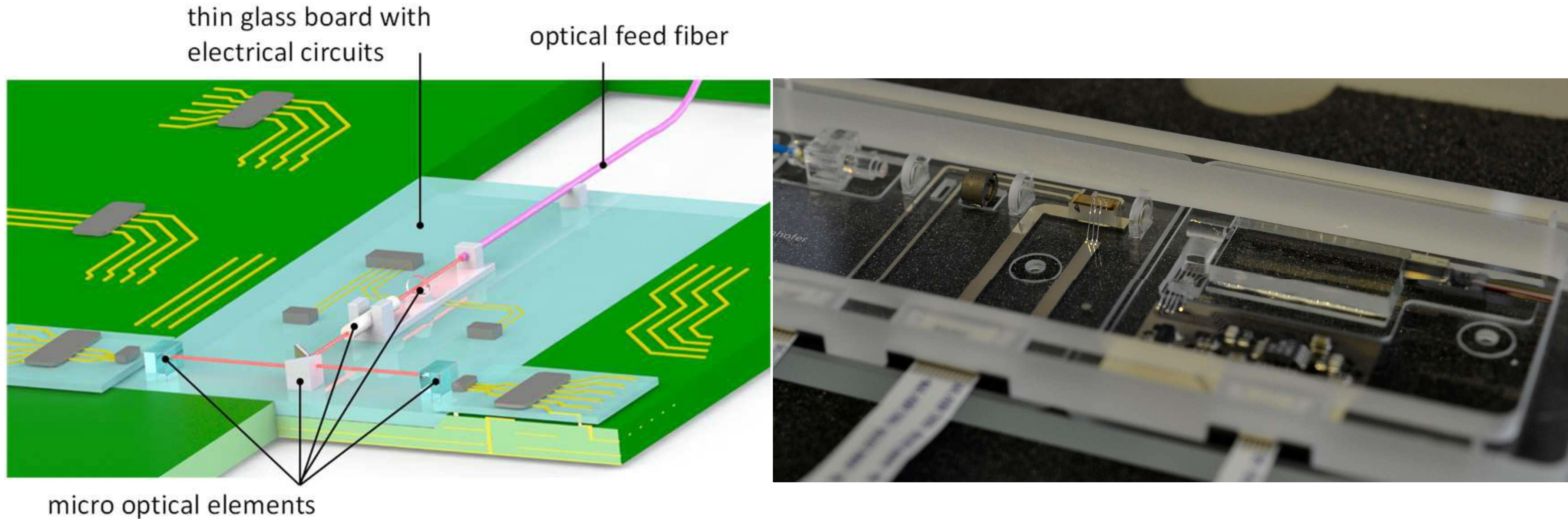
Massively parallel assembly and interconnect





SiP Packaging Toolbox: *Interconnect*

SIP is also benefitting from processes stemming from other areas of technology:



Optical Co-Packaging (optical interconnects)

SiP Packaging Toolbox: *Interconnect*

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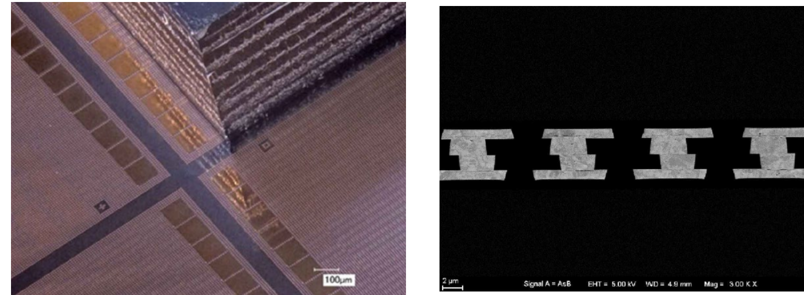
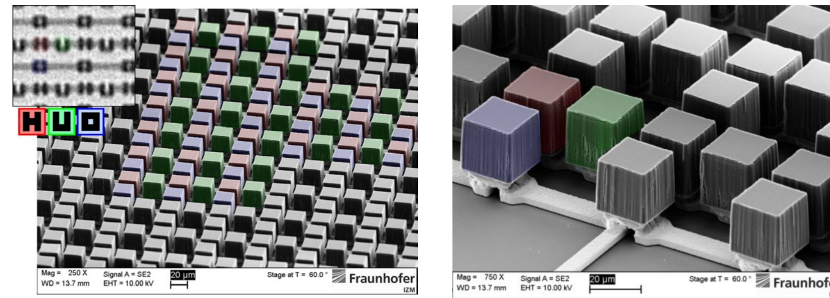
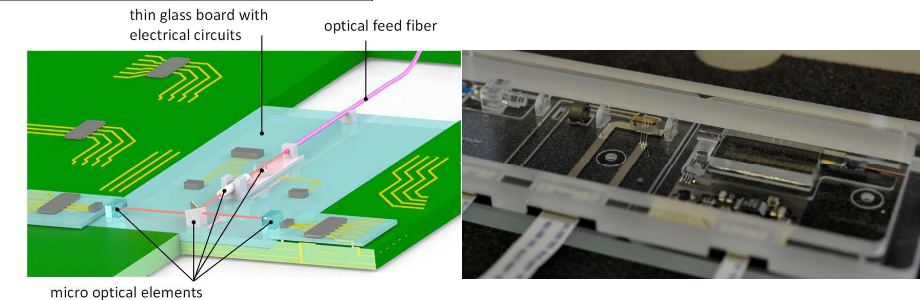
Hybrid bonding



Massively parallel assembly and interconnect



Optical Co-Packaging (optical interconnects)



SiP
ADVANCED SYSTEM IN PACKAGE TECHNOLOGY
VIRTUAL CONFERENCE

HIR
HETEROGENEOUS
INTEGRATION ROADMAP

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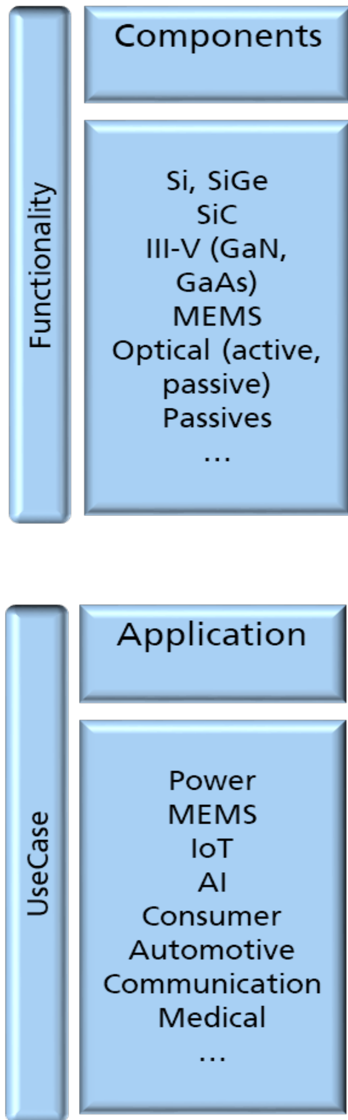

Interconnecting Functions

Material Focus

Architecture

Geometry and Footprint

Interconnect
Vertical Horizontal

Wirebond
FlipChip
TxV
SolderBalls
HybridBond

RDL
Wirebond

Encapsulation

Liquid (UF, GT, Mold)
Powder (Mold)
Laminate
Print. Materials

Packaging Concept

Side by side
2.5 D
3D (3DIC, PoP)
Fan Out xLP
Embedding (WLP type, ECP type)
3D Printed Package
…

Package Type

BGA
SO
QFP
LGA
Folded Flex
ECP
eWLP
…

Module, Functional Substrate

w/ Battery, Display, Lens,
…

Packaging Toolbox

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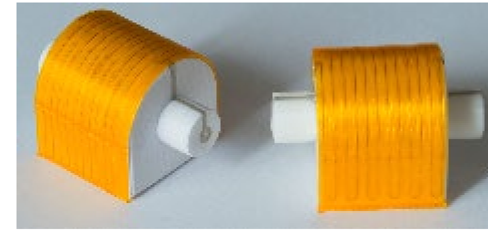
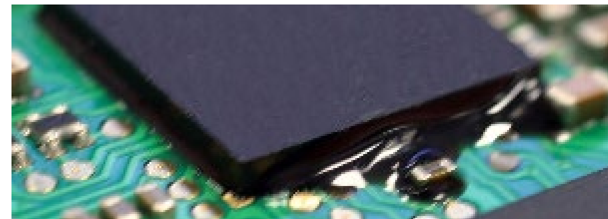
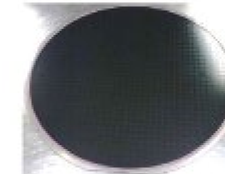
ASME
ELECTRON DEVICES SOCIETY

SiP Packaging Toolbox: *Encapsulation*







Workhorses:

Molding (Pellet)

Glob Top (Dispense)

UnderFill (Dispense)

Established:

Molding (Liquid, Compression)

Glob Top (Jet and Print)

UnderFill (Jet)

To Come:

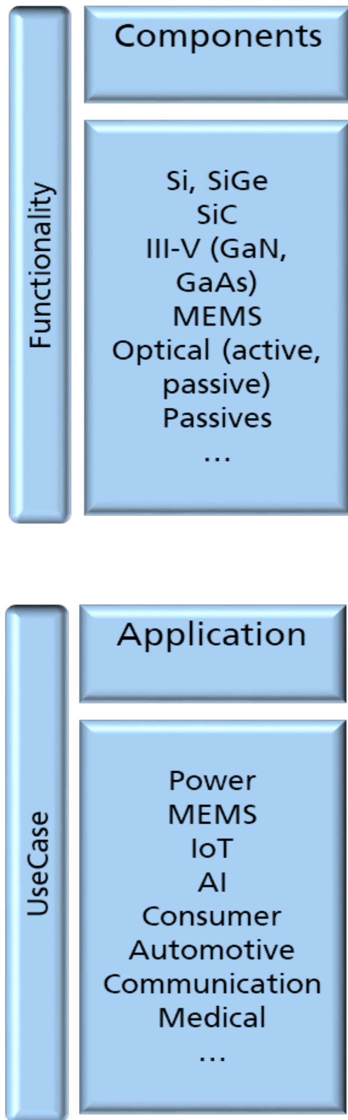
Lamination for thin/flat assemblies

3D Additive as „Structurally Integrated“

TWG on Additive Manufacturing

Material innovations, process innovations, conceptual innovations drive these advancements

Images: KCC, HybridCH, Finetech, Polymer Innovations, Neotech



Interconnecting Functions | Material Focus | Architecture | Geometry and Footprint

Interconnect — Vertical / Horizontal

- Vertical: Wirebond, FlipChip, TxV, SolderBalls, HybridBond
- Horizontal: RDL, Wirebond

Encapsulation

- Liquid (UF, GT, Mold)
- Powder (Mold)
- Laminate
- Print. Materials

Packaging Concept

- Side by side
- 2.5 D
- 3D (3DIC, PoP)
- Fan Out xLP
- Embedding (WLP type, ECP type)
- 3D Printed Package
- …

Package Type

- BGA, SO, QFP, LGA, Folded Flex, ECP, eWLP, …
- Module, Functional Substrate w/ Battery, Display, Lens, …

Packaging Toolbox

SiP ADVANCED SYSTEM IN PACKAGE TECHNOLOGY VIRTUAL CONFERENCE

SiP Packaging Toolbox

HIR HETEROGENEOUS INTEGRATION ROADMAP

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Packaging Concept

Concept	Material	Interconnection	
Side by Side	PCB	Solder Adhesive Wire bond	
	Flex Silicon	Solder Adhesive Wire bond	
Stacked / Folded	PCB	Solder Adhesive Wire bond	
	Flex	Solder Adhesive	
	Silicon	Solder Wire bond	
Embedding	PCB	Solder Electroplated	
	Flex	Solder Adhesive Electroplated	
	Thin film (Wafer Level)	Electroplated	
Fan Out Wafer/Panel Level	Mold compound	Solder Adhesive Electroplated	
Module	PCB Flex	Solder Adhesive Electroplated	

New Processes

- Wafer and Panel Level Packaging
- Reconstituted Wafers
- TSV´s for Silicon Interposer
- μ-Bumps
- Wafer Thinning and Handling
- Low *k* Polymers for RDL
- Merge of Front-end and Back-end

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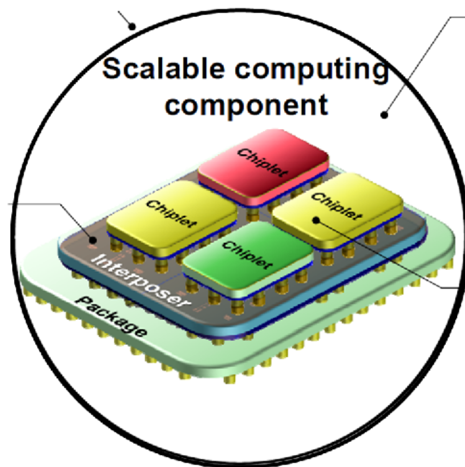
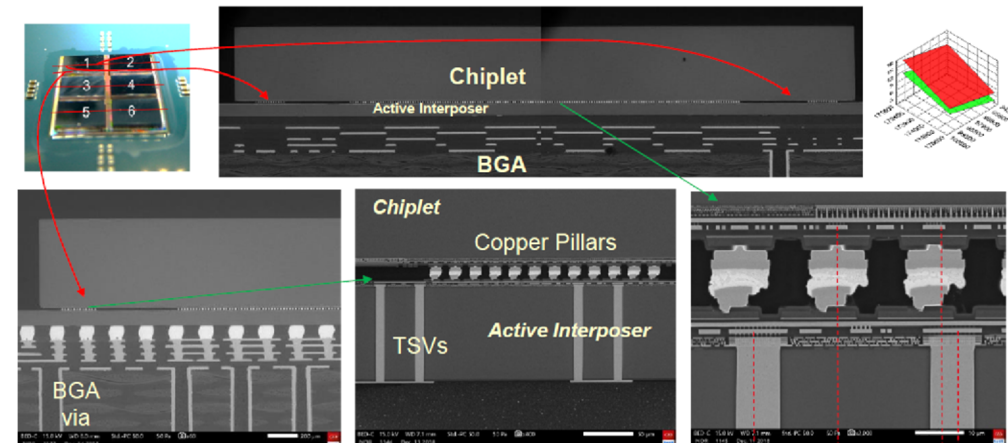
SiP Packaging Toolbox: Chiplet as a SiP momentum



- *More Than Moore* and ***More Moore*** **Integration in one SiP using Chiplet concept**
  - **Core technologies derived from previously mentioned tools**
  - **Active and passive interposer concept**

Issues to be adressed:

- KGD Issues
- EDA Issues
- Cost/Performance/Reliability considerations



Images from "Chiplet-based partitioning using Smart Interposer for High Performance Computing" by Patric Vivet, CEA Leti, 3D Summit, Dresden, Jan 2019

More CMOS Integration

Chiplet Integration Technologies[1]
- 2.5D (e.g INTEL FOVEROS, AMD EPYC, TSMC CoWoS, ASE FoCoS)
- 3D (e.g. AMD 3DVC, TSMC 3D-SoIC)

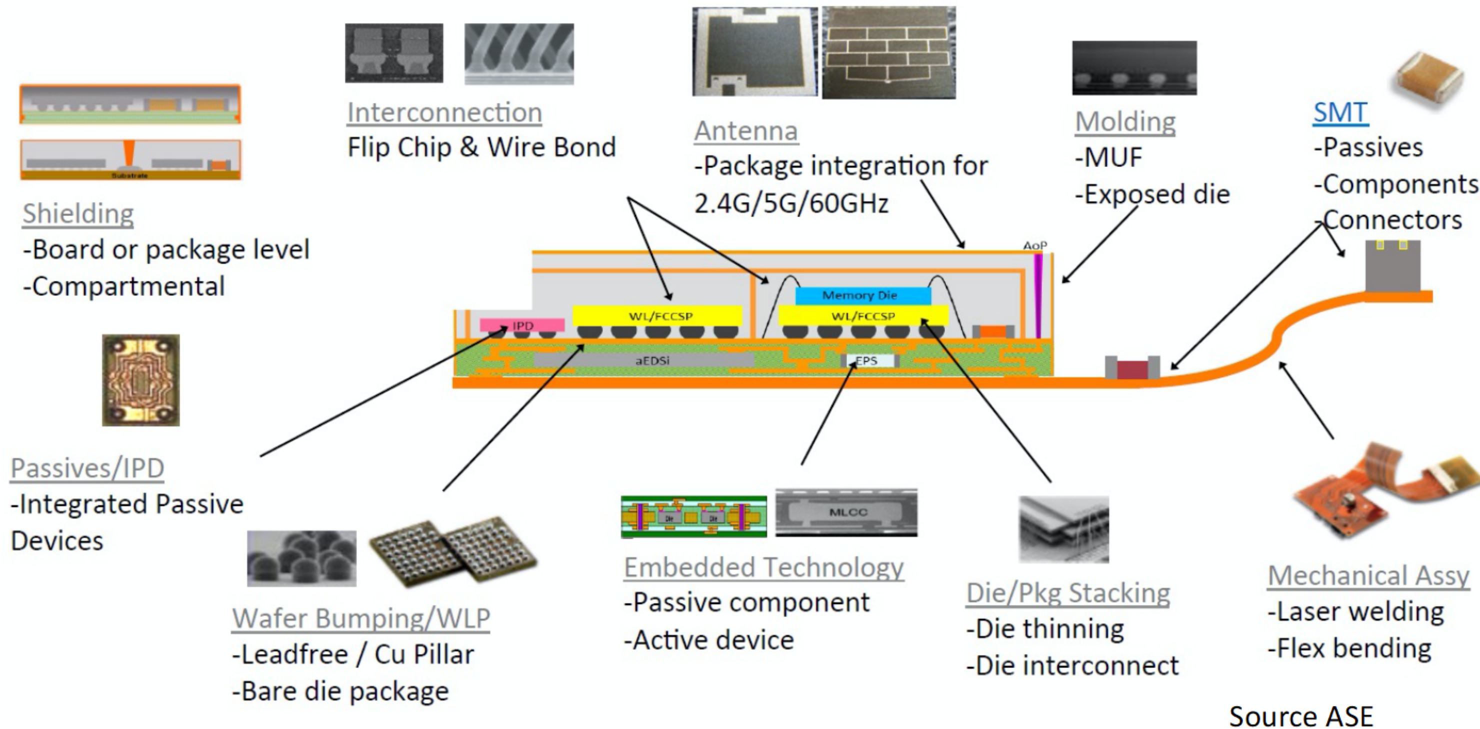
M3DI (CEA-LETI)[2]

QMI (INTEL)[3]

⇒ **HPC, Chapter 2**
⇒ **SCM/MCM, Chapter 8**
⇒ **2.5D/3D Interconnects, Chapter 22**

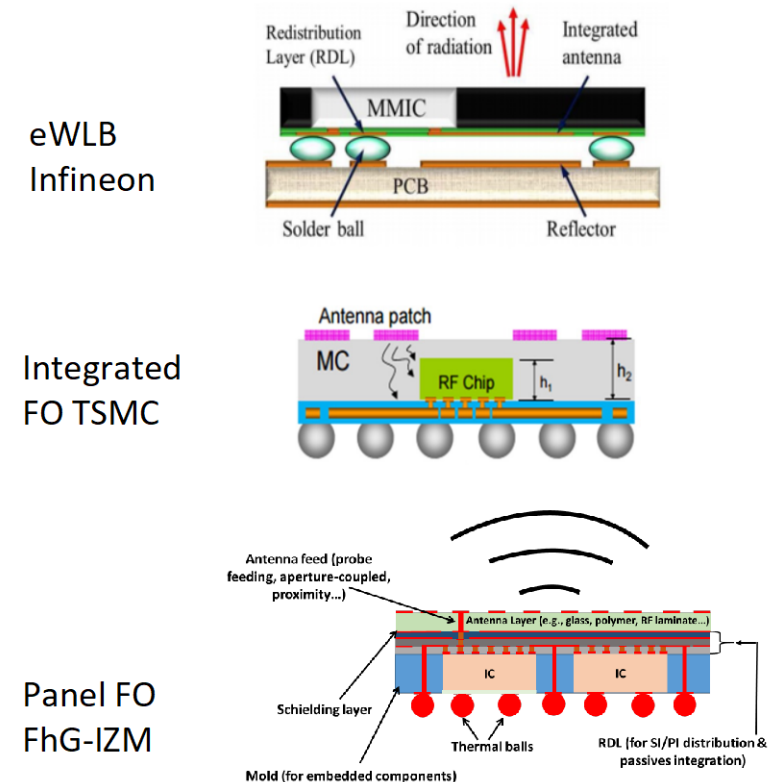
[1]: q.v. IEEE HIR, https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2021-edition.html, Ch. 2, 8, 22
[2]: DOI:10.1109/S3S.2014.7028194
[3]: J. Swan, „Extreme Heterogeneity: 3D Scaling & Challenges “, Semi 3D Summit, 2022, Dresden

SiP Packaging Toolbox –> "new functional blocks"



Source ASE

Example: Antenna Integration for FO

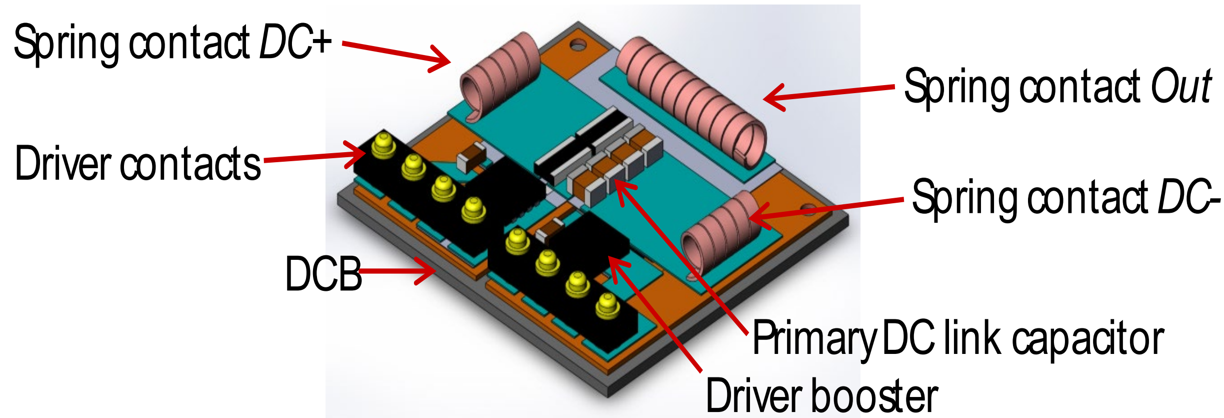


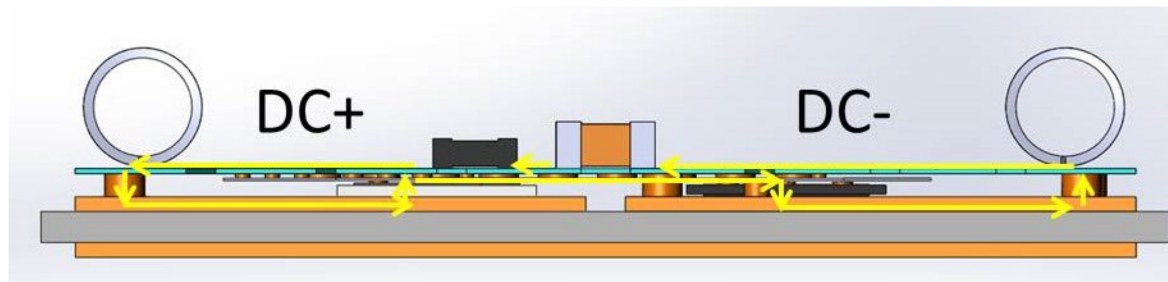
Aside from the **electrical domain**, also **multiple additional functionalities will emerge** for the SiP packaging toolbox.

Application Perspective - Power

(U)WBG semiconductors!

Switching Cell for Industrial Application

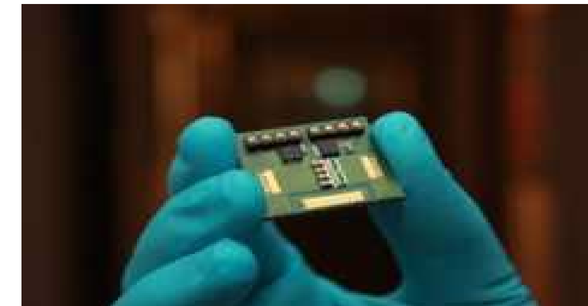




Photos source: Fraunhofer IZM

Challenges:

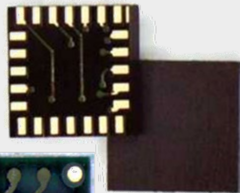
- "Switching Cell in Package"
- 2 component layers integrated: Chips and SMD
- Peripherals on the module
- Increasing Power Densities in Package: 200W/cm3
- Lower Parasitics Requirements
- Multi-Material Challenge: Si w/ III-V
- Thermal Transient Management
- EMC challenges
- Co-design with actives and passives

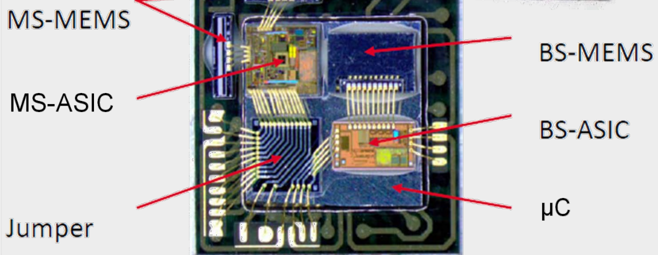


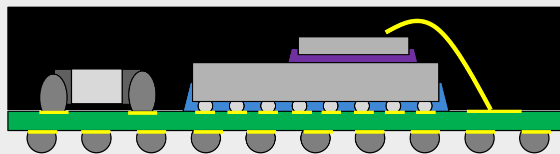
Application Perspective – MEMS Sensor

SmartSense – Intelligent 3D MEMS Compass

BOSCH

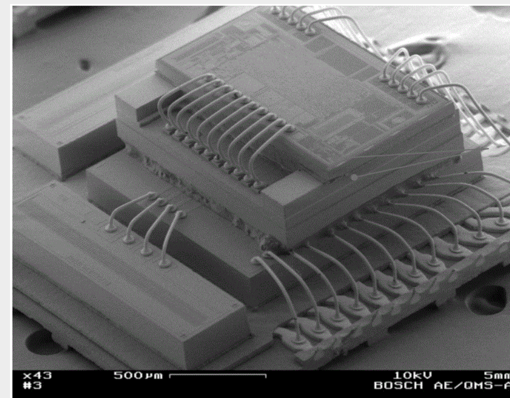






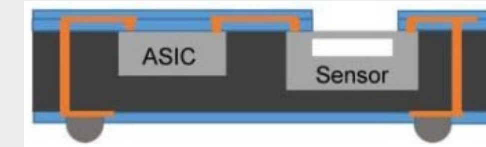
Heterogeneous Integration

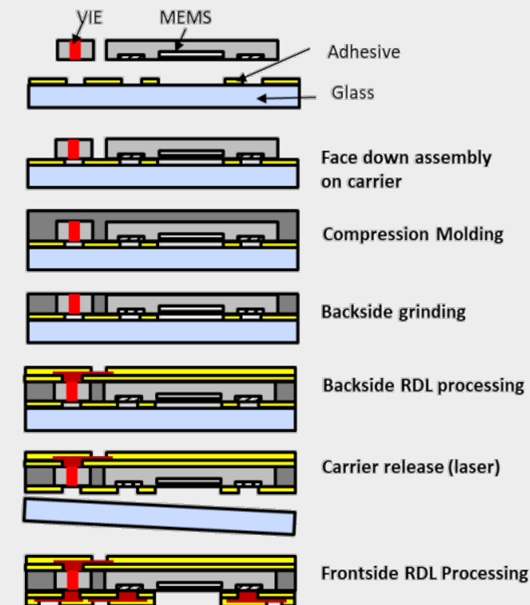
- BGA Multi-Sensor Package
- Evaluation of Material Combinations
- Reliability Investigations

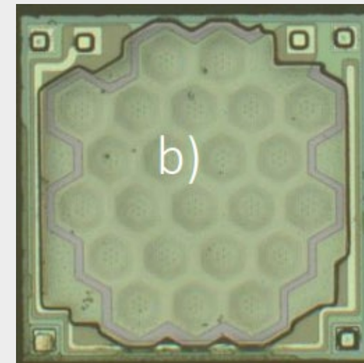


- Chip on Board technology
- Transfer molded LGA housing

Commercial Product for Consumer Market!



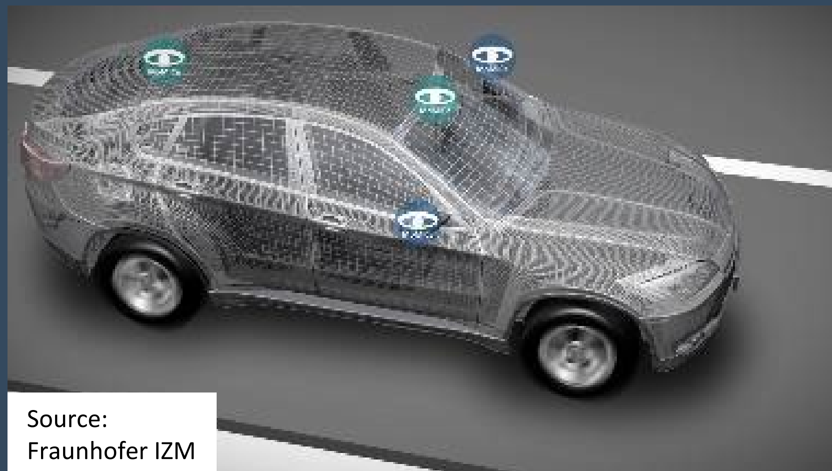


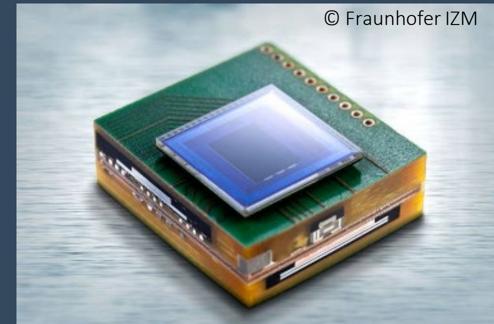


Platform Technology for NextGen MEMS Package

Application Perspective – AI (on edge)

Souce: NVIDIA


Source: Fraunhofer IZM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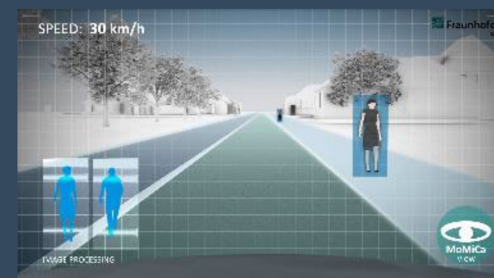


- SiP (electronic only) for autonomous driving
- SiP (multi domain functionality) for efficient autonomous driving
  - Specifications of Modular Micro Camera
    - Packaging of image sensors using embedding
    - Modular system with the option of integrating more sensors
    - Example: Dual Core ARM9 with350 MHz integrated image processing-DSP (APEX), 3M-Pixel CMOS sensor OmniVision, 16 MByte DDR SDRAM, 32 MByte NAND Flash, Mentor RTOS system software USB 2.0 device interface
  - Applications
    - Motion detection (protection against theft)
    - Pattern detection (traffic signs)
    - Edge detection (character recognition)
    - Real-time image processing

SiP Acceptance by Application

Industry competition
Moore
Processing
Information age

Industry competition
More than Moore
Sensing
Interaction age

Industry Competition
Beyond Moore
Actuating
Enhancement age

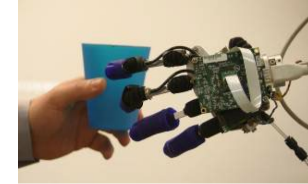
IBM, Google, Motorola, intel, Samsung, Apple, Facebook, SONY, BOSCH, SPACEX

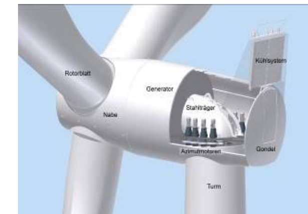
Personal Computers
Laptop
Smartphones
Tablets
Quantified self
Drones
Smart homes
Autonomous vehicles
Robotic Servants
Telekinesis

1980 — 2010 — 2020 — 2040

Acceleration

Source: Yole





SiP ADVANCED SYSTEM IN PACKAGE TECHNOLOGY VIRTUAL CONFERENCE
HIR HETEROGENEOUS INTEGRATION ROADMAP
iMAPS International Microelectronics Assembly & Packaging Society

Outline

Definitions and Classification

Toolbox for SiP

Challenges

Outlook

IEEE
IEEE photonics Society
semi
IEEE ELECTRONICS PACKAGING SOCIETY
ASME
ELECTRON DEVICES SOCIETY

New/future requirements derived from different application areas as indicators for roadmap targets => New challenges

Security

HPC

Mobile

Wearables

Drones

RF/THz

IoT

Autonomous Systems

Medical

Consumer

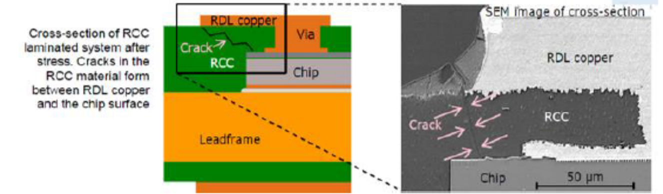
Power

Aerospace

Difficult Challenges for Implementing SiP

HIR HETEROGENEOUS INTEGRATION ROADMAP

Materials
- New materials (HF materials)
- Material interactions
- Failure modes
- Thermal mismatch



Cost
- New package platform (FO, embedding)
- Complex Systems

Link Controller Wi-Fi Module
Contains 2.4GHz Wi-Fi ATWILC1000, crystal, power inductor, and 21 L & C discretes

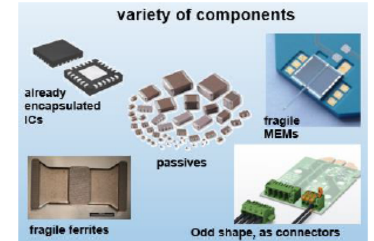
1st Generation

14.5 x 13.5 x 3.4 mm
4-layer PCB, metal shield

75% area reduction
25% lower cost

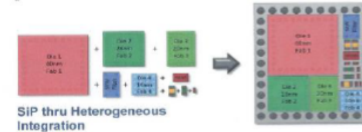
2nd Generation

7.0 x 7.0 x 1.2 mm
shielded module



Assembly
- Technology Diversity (Sensors, antenna, IC´s, passives
- Pitch, soldered and non-solderd components

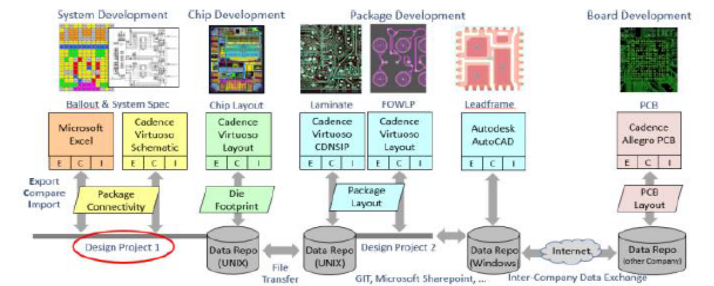
Standardization
common package type
- Footprint
- Dimensions
- Thickness



Customer Requirements
- Reliability and application specific requirements
- Temperature / cooling
- Performance
- Pitch, dimensions, thickness

Test
- Application specific (incl. mixed signal, media, etc.)
- Electrical, mechanical and thermal aspects
- Self testing, incl. BIST

Co-Design
- SiP Requiring a system <-> package co-design
- Different libraries in one project
- Multiple domains with different scaling properties
- Thermal, mechanical and electrical analysis



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Industrial Challenge Priorization

#	Priority	Challenge	State of the Art	Future Perspective
		Application Related		
1	Green	Functionality Increase	Single domain functionality	Multi domain functionality
2	Green	Non-electric functions	Separate SiP approach, separated value chain segment	Integrated in one flow of value chain creation
3	Yellow	Assembly	Single technology use	Choice from a technology menu built from a compatible tool box
4	Yellow	Reliability	Standards derived from "typical applications" and adapted to actual use case	Novel applications driven by new business models may render current standards obsolete
		Material Related		
5	Red	Material	Material evolution driven by integration requirements (e.g. high flow epoxies, CuPd wire)	Material revolution driving integration, disrupting industries' value chains
		Physics Related		
6	Red	Thermal Management	passive and active cooling built after simulation/validation assessment	Thermal-Electric and Mechanical Co-Design including the SiP integration site via CAD Tool
7	Yellow	Reliability	Empirically derived statistical models	Physics of Failure Modeling
8	Yellow	Form Factor	SiP design targeting maximum package efficiency limited by physical geometry	SiP design with as-needed efficiency, limited by cross-cutting aspects, interdependencies
9	Green	Signal Integrity	Individual design and test	Building blocks for S.I.
10	Green	Power requirements	<50W/cm³	200W/cm³

#	Priority	Challenge	State of the Art	Future Perspective
		Cross Cutting Aspects		
11	Red	Test	Single-domain testing, sequential test of multiple-domain functions	Simultaneous testing of multi-domain features to assess cross influences; testing specifically for target application
12	Yellow	EDA assisted CoDesign	Different, incompatible EDA suites	EDA suites with a common referral language and APIs
13	Green	WEEE	Electronics-only functionalities well addressed	Multi-domain functionalities difficult to address
14	Green	Standardization	Standards in formfactor of individual packages	Platform technology with interface to EDA tools ("VHDL for SiP")
15	Green	Security Aspects	No built-in security features	Depending on application, specific security features built into hardware may be needed
16	Yellow	Cost Reduction	Cost challenges are addressed only on one level in the value chain	System level perspective to leverage synergies surpassing individual levels of value chain

- Red: High Attention
- Yellow: Midterm Attention
- Green: No immediate action needs foreseen

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-

SiP and Modules are major directions in future microelectronics

Managing complexity will be a major challenge:

- Functional increase
- Complex material mix on semiconductor, package and board level
- Reliability caused by new applications (in addition => impact on sustainability)
- Power Delivery
- Thermal management
- Complex testing
- Co-design over various domains chip, package, board, subsystem, ….
- Cost constraints

HIR 2024 Outlook

Refining quantitative details……Strengthen Cross TWG relations…… Assess new/emerging developments (PIC and Quantum….)

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High Attention

Midterm Attention

No immediate action needs foreseen

SiP
ADVANCED SYSTEM IN PACKAGE TECHNOLOGY
VIRTUAL CONFERENCE

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Thank you for your attention!

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Images are referenced in the HIR – SiP&Module chapter, please see there

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