HIR Test TWG Update
HIR 2024 7th Annual Conference

Jeorge Hurtarte – Teradyne

Ken Butler - Advantest

February 22, 2024

HIR Test Chapter

Jeorge Hurtarte (Teradyne)

Ken Butler (Advantest)

Co-chairs

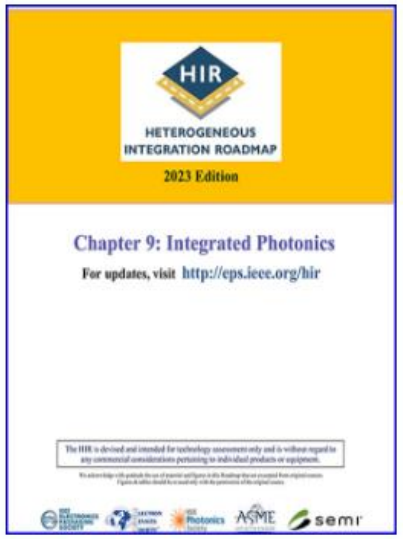
HETEROGENEOUS INTEGRATION ROADMAP

Sections and Leaders

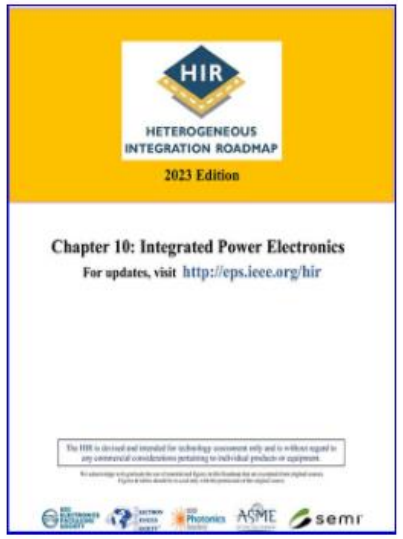
Section	Leader(s)
Executive summary	Ken Butler, Jeorge Hurtarte
RF Test	Jeorge Hurtarte (Teradyne)
Photonics	Dave Armstrong (Advantest)
Logic Test	Marc Hutner (Siemens)
Specialty Test	Wendy Chen (KYEC)
Memory Test	Phil Byrd (Micron)
Analog/Mixed Signal	Rich Dumene (Renesas, 2023)
Probe, handlers	Steve Ledford (Technoprobe, 2023)
System level test	Harry Chen (MediaTek)
Data analytics	Ira Leventhal (Advantest)
2.5D/3D Test	Morten Jensen (Intel), Boris Vaisband (McGill U.)
Test cost	Ken Lanier (Teradyne)

Heterogeneous Integration Roadmap 2023 Edition

Interested in hearing the latest updates and news on the Heterogeneous Integration Roadmap? Please sign up



Chapter 9: Integrated Photonics



Chapter 10: Integrated Power Electronics

Chapter 16: Emerging Research Devices

Chapter 17: Test

Chapter 17: Test

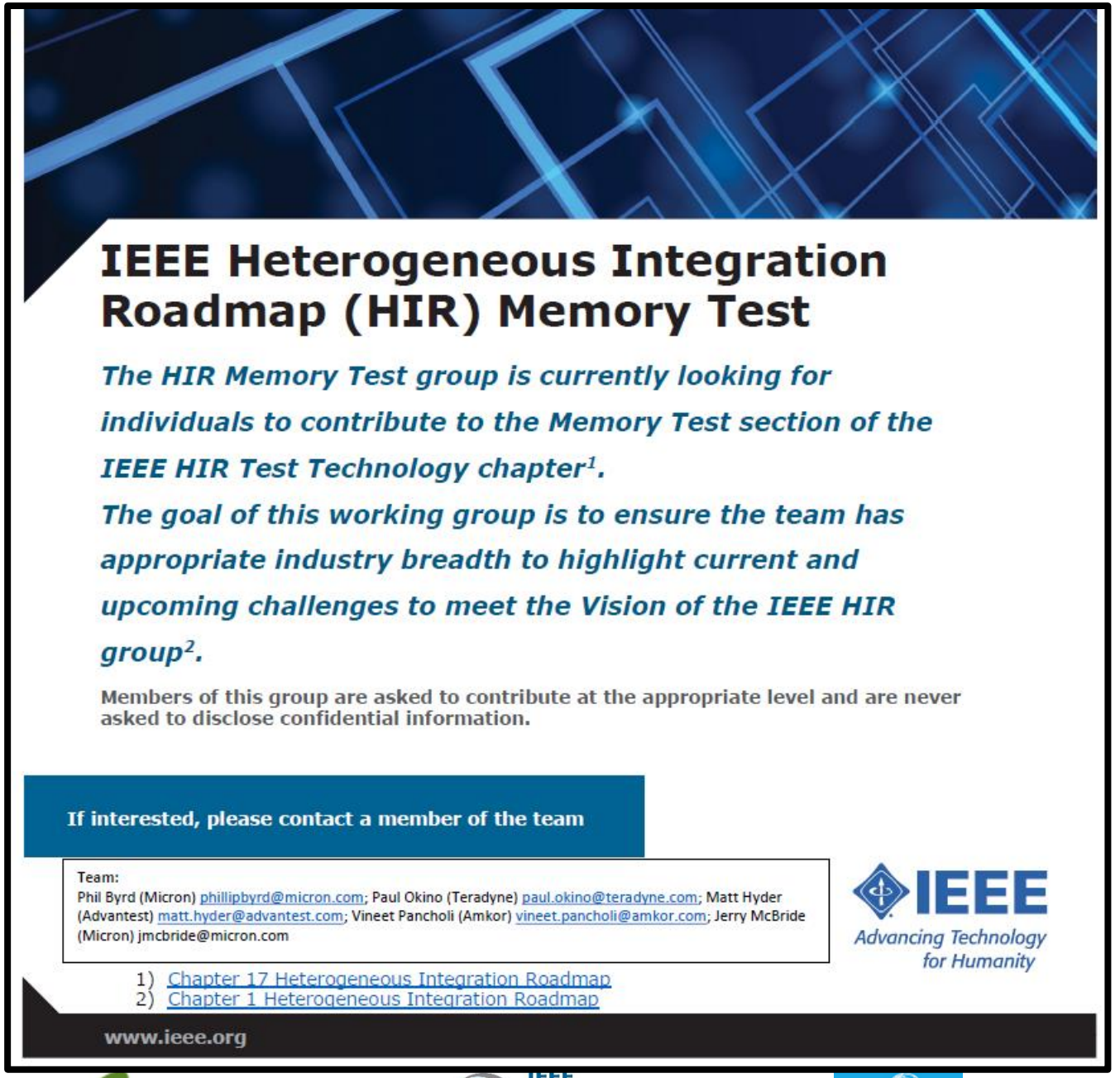
Full update on Test chapter (11 sections) completed in early 2023!

2024 HIR Test Chapter Update

- Full update on test chapter (11 sections) completed in early 2023!
- Cross-cut topic with many overlaps with the rest of HIR
- Test chapter leadership team met monthly in 2023
- Monthly meetings throughout the year, **inviting other HIR chapter groups to speak for cross-chapter collaboration**
- Multiple new section leaders, 110+ contributors, thank you!
- 2023 revision aimed at focusing on test trends and needs - less on providing extensive market context commentaries
- Move more content to online vs HIR PDF file to “slim down” chapter
  - 2022: 100 pages → 2023: 55 pages plus online content

e.g.:
- SIP and Module
- Automotive
- Single & Multichip Integration
- Integrated Power Electronics
- Thermal Management

Flyer:
Call for more Contributors



IEEE Heterogeneous Integration Roadmap (HIR) Memory Test

The HIR Memory Test group is currently looking for individuals to contribute to the Memory Test section of the IEEE HIR Test Technology chapter[1].

The goal of this working group is to ensure the team has appropriate industry breadth to highlight current and upcoming challenges to meet the Vision of the IEEE HIR group[2].

Members of this group are asked to contribute at the appropriate level and are never asked to disclose confidential information.

If interested, please contact a member of the team

Team:
Phil Byrd (Micron) phillipbyrd@micron.com; Paul Okino (Teradyne) paul.okino@teradyne.com; Matt Hyder (Advantest) matt.hyder@advantest.com; Vineet Pancholi (Amkor) vineet.pancholi@amkor.com; Jerry McBride (Micron) jmcbride@micron.com

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1) Chapter 17 Heterogeneous Integration Roadmap
2) Chapter 1 Heterogeneous Integration Roadmap

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HIR Test:
A Few Examples of Key Needs and Trends

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- Need: Known Good Die (KGD) design for test for 2.5D/3D enabling high quality wafer probe
- Need: Probe technology for testing singulated die
- Need Efficient methods for accessing, curating, managing, and analyzing data from on-chip sensors IP, equipment sensors, and test results
- Need: Test methodologies to address silent data corruption
- Trend: Increases in photonic lane counts, frequencies – need to contain test cost
- Trend: Specialty circuit (sensors, MEMS) integration into HI devices, need test methods to address them in embedded form
- Need: Test methods for chiplet-based designs with mixed technologies
- Need: High-volume over-the-air (OTA) handler-based testing for mmWave and THz

Test TWG Plans for 2024 and Beyond

- Add 5/10/15 year outlook for all Test chapter sections
- Full updates to Analog/Mixed Signal and Probe sections
- Why is test important, particularly for HI/chiplet devices
- Mobile/Automotive/other application affects test strategy?
- Redundancy in design and safety critical aspects
- DPPM modeling (focus on time zero vs reliability?)
- Trade-offs on test cost vs reliability
- Strategies for testing HI/chiplet-based products
- “Living document” with continuous updates on online content

Strategies for Testing HI/Chiplet-Based Products

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- HI devices limit direct access to the individual chiplets but still must be tested after assembly
- There will be increased reliance on DFT methodologies and test standards
  - IEEE 1149.x, IEEE 1687.1, IEEE P1838 (related to internal test access and control)
    - IEEE 1149 has been around since 1985 and is moving towards obsolescence
  - BIST to more thoroughly test chiplets in die form – KGD prior to assembly
- Advanced probing methods are making progress for TSVs and die stacks
- Stack repair is technically feasible but cost-prohibitive – redundant die in the stack is an option

Summary

- HI devices will be a growing part of the semiconductor marketplace
- Test is metrology for the entire semiconductor value chain
- Data analytics will play a much larger role for a wide range of applications – outliers, adaptive test, test time reduction, yield enhancement, …
- IEEE HIR Test TWG continues committed to identify and publish the test challenges and needs of the future.

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Executive Summary and Scope

The 2023 revision of the HIR test chapter aimed at focusing on test trends resulting from semiconductor market and technologies inflection points and emerging use cases, and less on providing extensive market context commentaries.

Sections Updated in 2023 Revision

Below we provide a high-level summary of the key test challenges and needs for each of the device types addressed in the test sections that were updated in this 2023 test chapter revision.

RF Test: Need 1) Non-frequency-gapped ATE RF test capability in the 0-100 GHz frequency, either for characterization, quality assurance, and/or high-volume production testing; 2) Higher ATE RF bandwidth production test capability up to 400 MHz for Wi-Fi 7 (with EVM in the 48+ dB range) and satellite; and up to 2 GHz to support 5G mmWave, UWB, and 6G THz; and 3) High-volume over-the-air (OTA) handler-based testing for mmWave and THz, and possibly automotive radar, will become increasingly relevant as DIB cabling for increased site count becomes cost-prohibitive.

Photonics Test: Need 1) novel test approaches for testing optics in co-packaged heterogeneous devices in high volume; and 2) Emphasis on test time containment and test time reduction as the number of lanes and wavelengths per fiber increase.

Logic Test: 1) Need new test methods for testing chiplet devices with mixed technologies (for example, need for retargetable test IP for next level of integration into SIP or system); and 2) test methodologies using Silent Data Corruption (SDC) logic testing methods.

Specialty Test: Need 1) higher test parallelism to reduce cost of test; and 2) multi-functional and cost-effective test capabilities as specialty devices become part of heterogeneous packages.

Memory Test: 1) Need test capabilities for addressing higher interface speed, power, and thermal management requirements; 2) Test capabilities for overcoming the challenges of electro-mechanical interface capability of wafer and component test as NAND memory density increases due to vertical scaling; and 3) Testing of higher DRAM bandwidth requirements.

Analog/Mixed Signal Test: Need 1) High speed instrumentation that can accept, force, and tolerate higher voltages and currents, driven by wide bandgap materials; 2) DC accuracy below 50 uV over the entire temperature range; 3) Closed-loop temperature forcing test capability at final test; 4) Test capabilities for A/MS devices housed in heterogenous packages; 5) Novel test solutions for overcoming the inherent physics of high voltage test at very high multisite testing; 6) High density floating resources with high accuracy, medium current capability, and large isolation voltages; and 7) Need for fully floating low-speed digital instrumentation for testing chip-to-chip communications devices which are shifted by tens to hundreds of volts above or below system ground.

System Level Test: Need 1) flexible DFT architectures for both structural and functional test content; 2) Effective SW/HW system failure diagnosis methods; and 3) Deep component parametric data extraction to Data analytics.

Data Analytics: 1) Need for advanced and comprehensive data analytics solutions that take full advantage of data from across the entire value chain; 2) Significant improvements in the development and adoption of key enablers such as communications infrastructure, data interchange formats, traceability, data security, and advanced data analytics algorithms; 3) Need efficient methods for accessing, curating, managing, and analyzing data from on-chip sensors IP, equipment sensors, and test results.

2.5/3D Test: Need 1) known-good-die DFT test methods that enable high quality wafer probe test – thus reducing fallout at final test; 2) Faster die-to-die communication standards that enable thorough testing at final test; 3) Standardized test and repair methodologies that considers new trends in 3D interconnects; 4) Yield prediction and analysis methods that ensure fallout at all levels of testing are understood; and 5) End-to-End data analytics capability that applies to all dies on the package.

Test Cost: 1) Need new probing technology which allows testing of singulated die; 2) Need new PCB and interposer technology to lower the cost and complexity of consumable material; 3) Need improvements in the test process by increased use of data analysis and machine learning based on measured data; and 4) Cost reduction of system-level testing.

Test Technology Working Group, Heterogeneous Integration Roadmap Leadership Team

Co-Chairs:	Ken Butler Jeorge Hurtarte		
RF Test:	Jeorge Hurtarte	**Analog/Mixed Signal Test:**	Rich Dumene
Photonics Test:	Dave Armstrong	**System Level Test:**	Harry Chen
Logic Test:	Marc Hutner	**Data Analytics**:	Ira Leventhal
Specialty Test:	Wendy Chen	**Test Cost:**	Ken Lanier
Memory Test:	Jerry McBride		
2.5D/3D Test:	Morten Jensen and Boris Vaisband		

2023 Test Chapter Edition Executive Summary

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Why is Test Important? Especially for HI?

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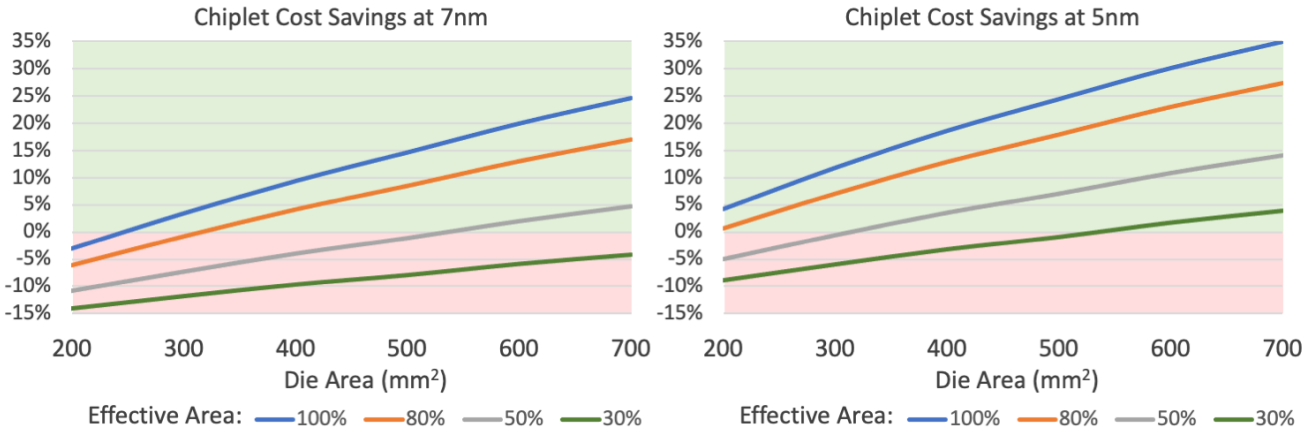

Figure 2. Chiplet cost scenarios. Chiplets are most cost effective for large die with little redundancy. In the 7nm node, the **crossover point for a design with 100% effective area is about 400 mm², whereas for 5 nm, the crossover is below 300 mm².**

L. Gwennap, "Chiplets Gain Rapid Adoption: Why Big Chips are Getting Small", The Linley Group, May 2021.

- HI devices more cost effective at smaller chip area with each new technology node
- HI requires known good die test (KGD) methods
- HI limits access points for each chiplet after assembly
  - Must test final product to ensure integrity of end product
  - Test is the only data source for functionality, performance

Think of test not as simply pass/fail, but the only metrology source available for packaged products

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Mobile/Auto/Other Application Affects Test Strategy?

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- Short answer: Absolutely!
- Automotive, industrial, space, and some other segments and companies very sensitive to time zero quality and reliability
  - Safe Launch – Req's for initial samples, test program qualification, ramp to production
  - Functional safety (ISO 26262) – Self-checking, "graceful failure" for safety-critical devices
  - Zero defects – Track all returns, containment for each within days/weeks
  - Parts per billion expectation for time zero quality
  - Temperature testing – cold/hot/room – adds cost and complexity
  - Stress testing and/or burn-in at multiple insertions – wafer, package, ...
- Other segments have varying, typically lower levels of test/quality requirements

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Redundancy in Design and Safety Critical Aspects

- Primary use of redundancy is for yield improvement
  - Embedded SRAMs have had redundant rows/columns for many years
  - Memory Built-in Self Test (MBIST) engines capture fail data, post-processed for repair solution
    - Historically, post-processing done off chip, on the ATE
  - More challenging in the HI context
    - Motivates use of soft repairs that can be recomputed across the lifetime
    - Built-in Self Repair
  - For products with high-speed serial links (USB, PCIe, UCIe, etc.), similar idea to create spare “lanes” that can be swapped in for defective ones
    - Emerging capability to use on-die sensors to monitor lane behavior, measure eye diagrams, etc.
- Some safety critical systems build in redundancy for fail safe operation, but limited use compared to yield redundancy in my experience

Trade-offs on Test Cost vs Reliability

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- Test for reliability can be expensive
  - Test at voltage and temperature extremes
  - Burn-in can be a bottleneck process, limiting material shipments
- Techniques to preserve reliability while holding down costs
  - Predictive analytics – detect which units are high/low risk for early life failures and alter the flows for both
    - High risk receive more rigorous testing, low risk can see lower/less testing (e. g., reduced burn-in)
    - Some of these methods can be run offline (e. g., post-wafer test) so zero test time impact/cost
  - On-die sensors for reliability mechanisms
    - Detect excessive and/or asynchronous aging and adjust test recipe to match use conditions
    - Attach sensors to on-chip test networks that can be accessed from the field
      - Devices detect reliability issues in-field and “phone home” for maintenance/repair