Heterogeneous Integration Roadmap
Thermal Technical Working Group (TWG)

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On behalf of the Thermal TWG
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Thermal TWG will consider three areas:
(a) Die level.
(b) Package integration/SIP/module Level.
(c) System Level (limited to board level).

Thermal TWG will focus on articulating the following in quantitative and qualitative terms:
(i) Canonical problems with thermal challenges;
(ii) Cooling limits for known solutions;
(iii) Advanced concepts and research.

Years 1-4 (2019-2022)
• Thermal effort kicked off in 2018.
• ~50 industry & university experts
• 2019-2022 chapters published
• Past focus
  • Canonical industry problems
  • Research advances
  • Emerging challenges and cooling technologies

2023 Update
• Silicon micro-channels mfg

Plan for 2024 Update
• Two confirmed collaboration: Additive Manufacturing, Modeling & simulation
• A few more to explore
1. 2D chip with stacked memory on a silicon/glass interposer

2. 3D stacked die with conduction interfaces

3. 3D stacked die with embedded liquid cooling

4. Optics/photonics based Heterogeneous package

5. Harsh environment (military, aerospace, automobile)

6. Mobile application chipset (package on package, fan out, bridge)

7. Voltage Regulators in a Heterogenous Package
Advanced Thermal Technologies & Research

[A] Thermal Interface Materials

[B] System thermal limits for HPC multi-chip modules

[C] Embedded liquid cooling of chip and chip stacks

[D] Advanced Thermal Materials for Thermal Management

'E] Thermomechanical Modeling for Heterogeneous Integration
The Si Microchannels study was convened by SEMI to identify materials, processes, and technologies that improve thermal management, performance, and yields for high performance computing (HPC) processors. A crucial part of this study is identifying stakeholders in implementing Si microchannels in high-performance devices, the process and equipment changes required, and any potential blocking elements or “deal-breakers” to adopt on.

The study also sought to understand why silicon microchannels have not yet been implemented in production – is it technology, economics, or both?

Finally, as the silicon manufacturing supply chain will need to work together on models/simulations that take materials and manufacturing processes into account and estimate the economic impacts of scaling to volume manufacturing,
Wafer-level approaches: two Design Options

SOC and HBM with different height

SOC and HBM with same height
Key Issues and Next Steps

Potential Concerns:
- Scalable to future IT roadmap (increasing substrate size and package stress)
- Test, Yield, Assembly
- Pressure drop across the manifold
- System integration

Next Steps:
- Prioritize the development of microchannel-based chip cooling approaches as part of the CHIPS program.
- Move forward with a Si Microchannels Phase II program with the goal of creating test vehicle(s).

*Need a collaborative approach with the data center industry community to address SOC package, coolant compatibility, cooling solution distribution, and total cost of ownership*
Thermal TWG 2024 Planned Activities

Confirmed HIR Collaboration b/w Thermal TWGs and
- Additive Manufacturing for Electronics on Cooling Enhancement (Eric Dede)
- Modeling and simulation on warpage and 3D package (Christopher Bailey and Xuejun Fan)

More Collaboration in Consideration
- Thermal/mechanical technical committee (EPS) (Sreekant Narumanchi)
- Other roadmaps, such as MAPT (Tim Chainer)
- Dielectric fluids in Embedded application, e.g. electric vehicles (Sreekant Narumanchi)
- Thermal challenge and solutions for test (Ken Butler, Jeorge Hurtarte)

Please reach out to us if your group have specific needs on the thermal investigation.
**HIR Thermal TWG Contributors**

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