Advanced Packaging in the Era of HPC and AI

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Samsung Electronics

2024 Heterogeneous Integration Roadmap (HIR)
Semiconductors in the Era of AI

- AI drives explosive growth in data processing and computing power

![Graph showing growth in computing power and data storage from 2005 to 2025. Source: IDC, Seagate, DataAge, Cisco, IHS, Gartner, Statista]

![Graph comparing computing power of Chat GPT 1 vs Chat GPT 4. Source: Sevilla et al., 2023, Our World in Data]
The human brain far exceeds the current level of logic and memory semiconductors.

Logic/Memory semiconductor innovation is needed for AI growth.

**Semiconductors vs. the Human Brain**

- Memory:
  - HBM
  - 460 GB/s

- Storage:
  - 25 TB/s

- Performance:
  - 1 PFLOPS/W

- Logic:
  - 7nm NPU
  - 0.00333 PFOPLS/W

2024 Heterogeneous Integration Roadmap (HIR)
Logic Performance Innovation: Rise of HI

- Overcoming Cost/Performance challenges with ‘Beyond Moore’ Adv. PKG solutions

**Cost Challenge**
Manufacturing costs continue to increase in advanced process technology era

- Cost per Yielded mm² for a 250 mm² Die
  - 45nm: 1.0
  - 32nm: 2.0
  - 28nm: 3.0
  - 20nm: 4.0
  - 14/16nm: 5.0
  - 7nm: 6.0

- Die Size Increasing over Time
  - Reticle Limit

**Beyond Moore Solution**
High yielding smaller chips and optimal process selection

- Node N
- N / N / N-1 Specialty

**Performance Challenge**
Moore’s law slowdown due to technological difficulties

- Processor Frequency Increasing over Time
  - (Source: Intel CPU Trend, Wikipedia)

- 2024 Heterogeneous Integration Roadmap (HIR)
  - ~100um pitch
  - ~um pitch
Memory Bandwidth Innovation: Rise of Adv. PKG

- Overcoming the Logic-Memory bandwidth gap through Adv. PKG integration

**Memory BW Challenge**

Memory Bandwidth acts as system performance bottleneck

**Logic-Memory BW Improvement**

Heterogeneous Integration w/ Advanced Package

Performance Growth Compute vs. DDR Bandwidth

<table>
<thead>
<tr>
<th>Signal Path</th>
<th>~ 10cm</th>
<th>~ cm</th>
<th>~ mm</th>
<th>~ um</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O #</td>
<td>8</td>
<td>64</td>
<td>1,024</td>
<td>&gt;&gt;1,024</td>
</tr>
<tr>
<td>B/W</td>
<td>~5.6GB/s</td>
<td>~76.8GB/s</td>
<td>~1TB/s</td>
<td>&gt;&gt;2.5TB/s</td>
</tr>
</tbody>
</table>

2024 Heterogeneous Integration Roadmap (HIR)
Contents

Introduction

Samsung AVP Platform Solutions

HPC / AI
- HBM
- 3D Logic Stacking
- I-Cube

Mobile AI
- Mobile AP
- Low Power Wide I/O Memory

Heterogeneous Integration Eco System

2024 Heterogeneous Integration Roadmap (HIR)
HBM Roadmap

- Increased needs for HPC/AI applications call for high-stack, high-performance HBM
  1) HBM3 12H world first mass production (’23.7~)
  2) HBM4 16H HCB technology in development
  3) HBM4 customized HBM in development

<table>
<thead>
<tr>
<th></th>
<th>2023</th>
<th>2024</th>
<th>2025~</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>HBM Product</strong></td>
<td>HBM3</td>
<td>HBM3E</td>
<td>HBM4</td>
</tr>
<tr>
<td><strong>HBM Thickness</strong></td>
<td>720um</td>
<td>720um</td>
<td>775um</td>
</tr>
<tr>
<td><strong>Stack #</strong></td>
<td>8/12H</td>
<td>8/12H</td>
<td>12/16H</td>
</tr>
</tbody>
</table>

### Architecture
- **Structure**
  - 8H-Stack
  - 12H-Stack
  - 16H-Stack
  - Customized HBM

### Technology
- **Joint Gap**
  - TCB: 9um/7.3um
  - HCB: 7.3um
  - <7.0um
  - Gapless

2024 Heterogeneous Integration Roadmap (HIR)
TCB HBM-12H in mass production (’23), HBM-16H sample developed

**Advantages of TCB**

- **Joint Thermal Resistance**
  - Up to 35% vs MR-MUF
  - Higher Bump Density
  - Less Joint Gap

- **Chip Thickness for High-Stack**
  - Up to 15% vs MR-MUF
  - Less Joint Gap

**Samsung Exclusive Material & Equipment**

- **NCF Material**
  - Thinner Hybrid NCF

- **CoW Bonder**
  - High Accuracy & Chip Tilt Control

**TCB HBM-16H Sample (2023)**

- DC Yield > 9x%

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2024 Heterogeneous Integration Roadmap (HIR)
HBM-HCB Technology

- HBM 12H function sample developed with HCB ('23), 16H D/C sample developed

**TCB**
Thermo-Compression Bonding

**HCB**
Hybrid Cu Bonding

**Advantages of HCB**
- High-stack
  - Up to 33% \(^1\) vs TCB
- PKG Thermal Resistance
  - Up to 20% \(^1\) vs TCB

**Samsung Exclusive Equipment & Technology**

**HCB Bonder**
- High accuracy & chip tilt control
- Facilities internalization by Samsung

**μ-Particle control**
- Class 1 facilities
- Protection layer coating

**BEOL Metal design for HCB**
- Surface topology control
- Cu pad expansion control

12H Function Sample (2023), 16H D/C Sample (2023)
(Presented at '23 ECTC)

2024 Heterogeneous Integration Roadmap (HIR)

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\(^1\) Same Chip & HBM PKG Thickness
AVP History for 3D Logic Stacking

- High I/O density and fine pitch development required for HPC/AI applications
3D Logic Stacking Roadmap

- 3D logic readiness through technology verified in memory mass production

### TCB
- **Bump Pitch**: 24 um, 21 um, 18 um, <15 um (28-)
- **IO density (Bump/mm²)**: 1,736, 2,267, 3,086, 4,444 (28-)
- **PDK**: SF5/4, SF3P/2
- **Mass Product**: 1)

### HCB
- **PAD Pitch**: 4 um, 2.5 um, <2 um
- **IO density (Pad/mm²)**: 62.5K, 160K, >250K
- **PDK**: SF3P/2
- **Mass Product**: AP, HBM2)

1) 16 HBM2, 18 CIS-3Stack MP
2) Mass production ready

2024 Heterogeneous Integration Roadmap (HIR)
3D Logic Stacking-TCB Technology

- 25um pitch ready for mass production through TCB-NCF technology

**Advantages of TCB-NCF**
- High IO density, Low Thermal Resist.
  - Up to \( x2 \) in IO count
  - Up to 5% \( T_j \) at AP
- High Productivity
  - Up to 13% reduction in Assy. step
  - Fine Pitch
  - Less Joint Gap
  - Less Process step
  - MP Proven

**25um Pitch MP ready (‘23)**

**TCB-NCF**
- Thermo-Compression Bonding
- Non-Conductive Film
  - >25um
  - >10um

**MR-CUF**
- Mass Reflow-Capillary Underfill
  - >35um
  - >30um

**Samsung MP Proven Tech.**

**Process & Material**
- TC Profile & NCF Viscosity control

**Infra**
- Exclusive tool
- Equip. Compatibility

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2024 Heterogeneous Integration Roadmap (HIR)
3D Logic Stacking-HCB Technology

- 3μm ultra fine pitch technology verification complete

3D HCB
(3μm Pitch, Joint Gap 0μm)

3D TCB
(25μm Pitch, Joint Gap 12μm)

Samsung Exclusive Process

Process & Tool
- High precision alignment & bonding

Structure
- Thin bottom structure without Thermal dummy

Advantages of Samsung’s 3D HCB

I/O Density
Up to X70
3μm vs. 25μm Pitch

Allowable Power
Up to 33%
vs. μ-bump

3μm Ultra Fine Pitch Feasibility (~23)
for Adv. Node Device (SF4/5, ~26 PDK release)

2024 Heterogeneous Integration Roadmap (HIR)
I-Cube Roadmap

- I-Cube enables larger interposer, more HBM's and multi-die for AI/Date center applications

<table>
<thead>
<tr>
<th>2018</th>
<th>2020</th>
<th>2022</th>
<th>2024</th>
<th>2026</th>
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</thead>
<tbody>
<tr>
<td><strong>Interposer Size (Reticle)</strong></td>
<td>In Mass Production('20)</td>
<td>In Mass Production('20)</td>
<td>Production Planned (MP '24)</td>
<td><strong>2x</strong></td>
</tr>
<tr>
<td><strong>PKG Size</strong></td>
<td><strong>65x65 mm²</strong></td>
<td><strong>85x85 mm²</strong></td>
<td><strong>100x100 mm²</strong></td>
<td><strong>130x130 mm²</strong></td>
</tr>
<tr>
<td><strong>ISC Cap density</strong></td>
<td><strong>1500nF/mm²</strong></td>
<td><strong>2200nF/mm²</strong></td>
<td><strong>2750nF/mm²</strong></td>
<td><strong>4400nF/mm²</strong></td>
</tr>
</tbody>
</table>

2024 Heterogeneous Integration Roadmap (HIR)
I-Cube E Technology

- I-Cube E is the cost-effective PKG solution with panel level technology.

![Samsung I-Cube E Platform](image)

**Cost Efficiency + Expandability**
- Si Interposer → Si Bridge + RDL

  - Si Interposer Net Unit 12ea/Wf
    - *12xHBM (51x68mil)
  - Si Bridge Net Unit 1,060ea/Wf
    - *Si-Bridge 87x66mil (13 ea/PG)

**Productivity**
- Wafer Level → Panel Level

  - 12ea/Wf → *x3
    - >36ea/Wf

**Performance**
- Low Loss @ SerDes 112G

  - Loss(SerDes 112G) : TSV > Cu Post w/ EMC
    - *HBM3E 8Gbps & Adv. UIC: 32Gbps is equivalent

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2024 Heterogeneous Integration Roadmap (HIR)
Samsung AVP Solutions for AI: Mobile Roadmap

<table>
<thead>
<tr>
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<tr>
<td><strong>Memory</strong></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>* # of I/O, BW</td>
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<tr>
<td>LPDDR5</td>
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<tr>
<td>LPDDR6</td>
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<tr>
<td>LP Wide I/O</td>
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<td><strong>2D PKG</strong></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>* Thermal</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>* Fine Pitch</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
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<tr>
<td>2D FO-WLP 7/8µm RDL, Mono Die</td>
<td>23.1Q</td>
<td>23.2Q</td>
<td>24.4Q</td>
<td>25.4Q</td>
<td>25.1Q</td>
<td>25.4Q</td>
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<tr>
<td>2D FO-WLP HPB</td>
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<td></td>
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<tr>
<td>2D FO-WLP 5/6µm RDL, Multi-Die</td>
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<td></td>
</tr>
<tr>
<td>3D FO-WLP HCB 4µm Bump Pitch</td>
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<tr>
<td><strong>3D PKG</strong></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>* Fine Pitch</td>
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<td>3D TCB</td>
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<td>24.4Q</td>
<td>24.4Q</td>
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<td>3D HCB</td>
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</tbody>
</table>

2024 Heterogeneous Integration Roadmap (HIR)
## Fan-Out PKG Roadmap

- FOWLP with chip last & double sided RDL is in mass production for mobile AP (‘23~)
- Key technologies are under development for On-Device applications such as mobile AP and LPW memory.

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Mobile AP</th>
<th>2024</th>
<th>2025</th>
<th>2026</th>
<th>2027</th>
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<tbody>
<tr>
<td><strong>Structure</strong></td>
<td>I-PoP Memory</td>
<td>FOWLP Memory</td>
<td>FOWLP-HPB Memory</td>
<td>FOWLP-SIP Memory</td>
<td></td>
</tr>
<tr>
<td><strong>Heat resist.</strong></td>
<td>x 1.00</td>
<td>x 0.85</td>
<td>x 0.55</td>
<td></td>
<td></td>
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<tr>
<td><strong>UClle I/O</strong></td>
<td></td>
<td></td>
<td></td>
<td>x 16</td>
<td>x 32</td>
</tr>
<tr>
<td><strong>LPDDR</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Structure</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>I/O density</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>x 512</td>
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<tr>
<td><strong>Tech.</strong></td>
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<tr>
<td><strong>Si thickness</strong></td>
<td>110um</td>
<td>215um</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td><strong>Double Side RDL</strong></td>
<td>7/8um</td>
<td>2/2um</td>
<td></td>
<td></td>
<td>1/1um</td>
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<tr>
<td><strong>Cu Post AR</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>≥6:1</td>
</tr>
</tbody>
</table>

2024 Heterogeneous Integration Roadmap (HIR)
Fan-Out PKG Technology for Mobile AP

- Samsung’s Fan-out PKG with Advantages for TAT, Architecture and Thermal Performance.

### Samsung’s MP Proven Processes

- **Chip Last**
  - Samsung’s CoW technique

- **Double-sided RDL**
  - Unique tape carrier (exclusive)
  - High AR Cu Post process

### Advantages of Chip Last-D.RDL (AVP)

- **Process TAT**
  - Up to \( \times 33\% \) vs Chip First/D.RDL
  - Pre-made F.RDL

- **Architecture Flexibility**
  - Back side RDL

- **Heat resistance**
  - Up to \( \times 45\% \) vs I-PoP
  - Heat path block

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2024 Heterogeneous Integration Roadmap (HIR)
Fan-Out PKG Technology for Low Power Wide I/O Memory

- FOPKG with Vertical Interconnection of multi-die stacks enables to increase I/O density & BW.

### Wire Bonding
- FBGA

### Vertical Interconnection
- VWB
  - *VWB: Vertical Wire Bonding*
- VCS
  - *VCS: Vertical Cu PostStack*

### Samsung’s New Architecture & Process
- **Cu Post**
  - High AR Cu Post ≥6:1 (24)
- **RDL/Bumping**
  - Wafer Level Fine Pitch RDL & Bump Process (MP Ready)

### Advantages of VCS (AVP)

#### I/O Density, Band Width
- Up to \( \times 8 \) vs FBGA
- Up to \( \times 2.6 \) vs FBGA

#### High Productivity
- Up to \( \times 9.0 \) vs VWB

- Finer pitch (≤60μm)
- High AR Cu Post (≥6:1)
- Shorter process time (≥ I/O x256)
- Wire bond → Cu Post

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2024 Heterogeneous Integration Roadmap (HIR)
Heterogeneous Integration Eco System

- Overcoming semiconductor technology challenges through collaboration between Samsung AVP’s HI platforms and our partners’ specialized expertise

EDA Design methodology
- Cadence
- Synopsys
- Ansys
- Siemens

Chiplet IF Including memory
- UCIe
- JEDEC
- Samsung Foundry
- Cadence
- Synopsys

OSAT Cooperation
- Amkor Technology
- ASE
- JCET

PCB & More Supply Chain
- IBIDEN
- KYOCERA
- Samsung
- Shinko
- TOPPAN

2024 Heterogeneous Integration Roadmap (HIR)
Samsung AVP R&D Across the Globe

- Multiple portals for research and development collaboration between Samsung and Partners

2024 Heterogeneous Integration Roadmap (HIR)
Thanks

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