SAMSUNG

Advanced Packaging in the Era of HPC and AI

Vincent (Woopoung) Kim, Ph.D.

EVP, Advanced Package(AVP) Business
Samsung Electronics

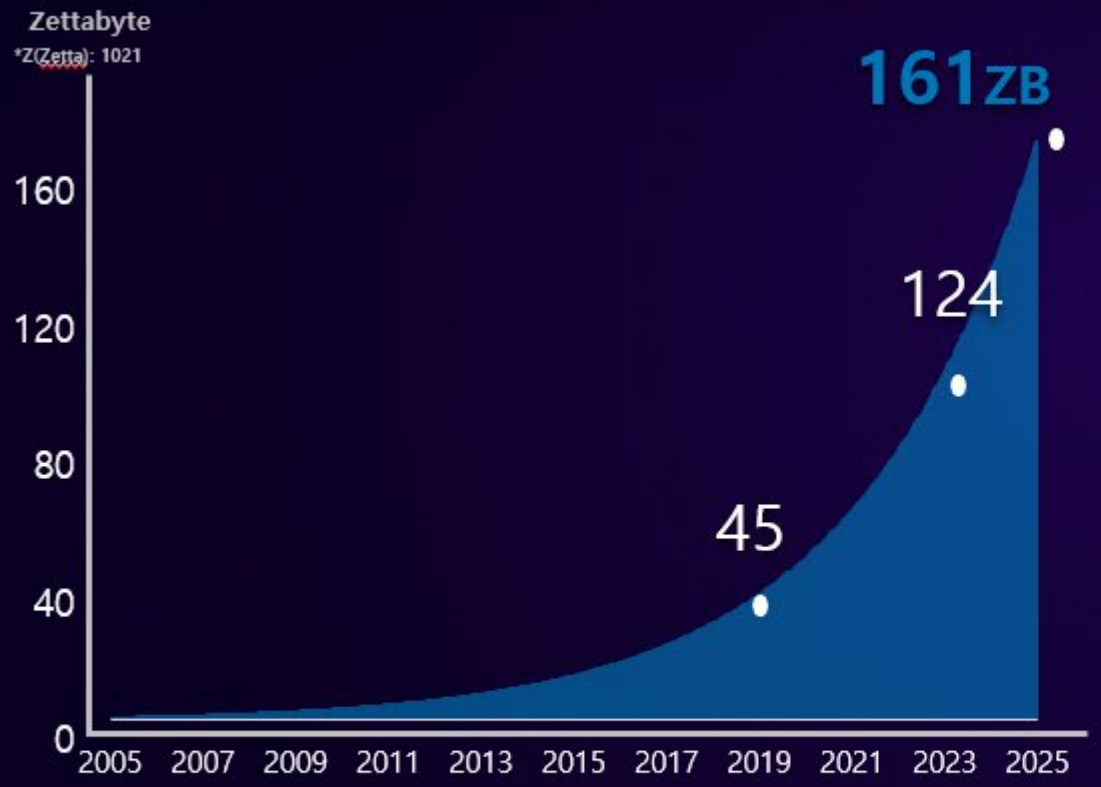
2024 Heterogeneous Integration Roadmap (HIR)

SAMSUNG

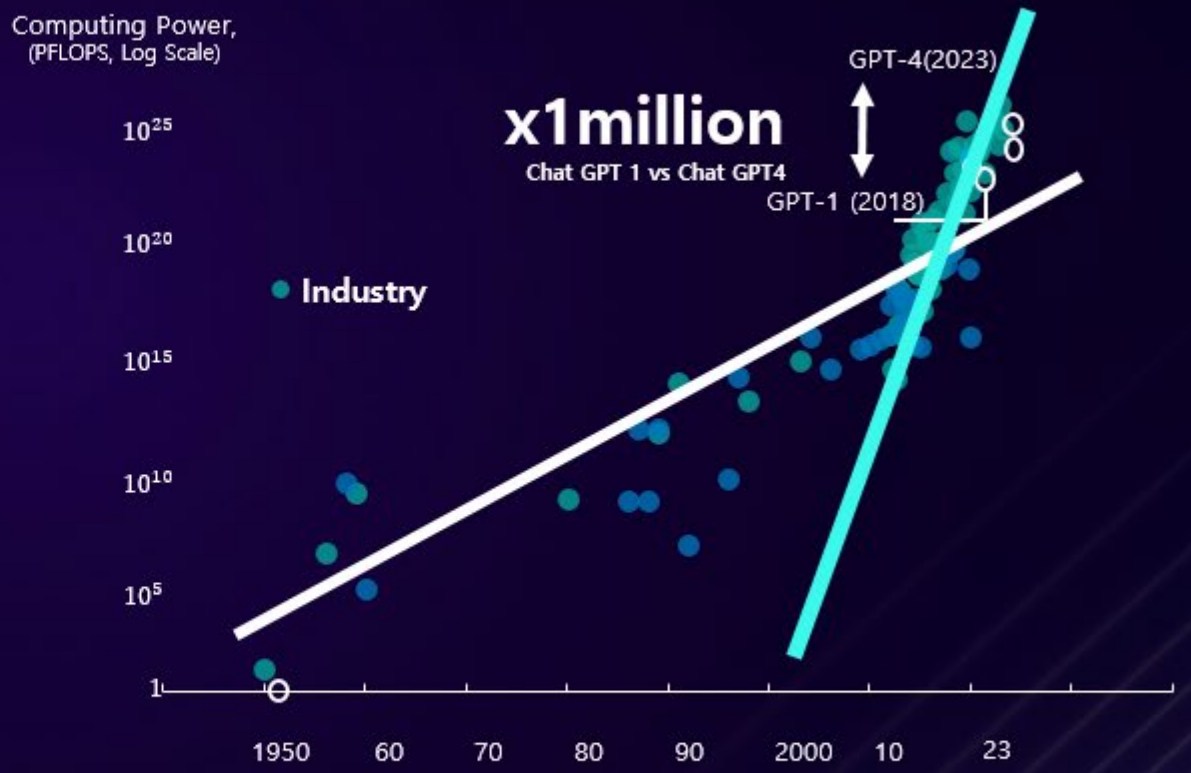
Contents

Semiconductors in the Era of AI

- AI drives explosive growth in data processing and computing power



Source: IDC Seagate DataAge, Cisco, IHS, Gartner, Statista

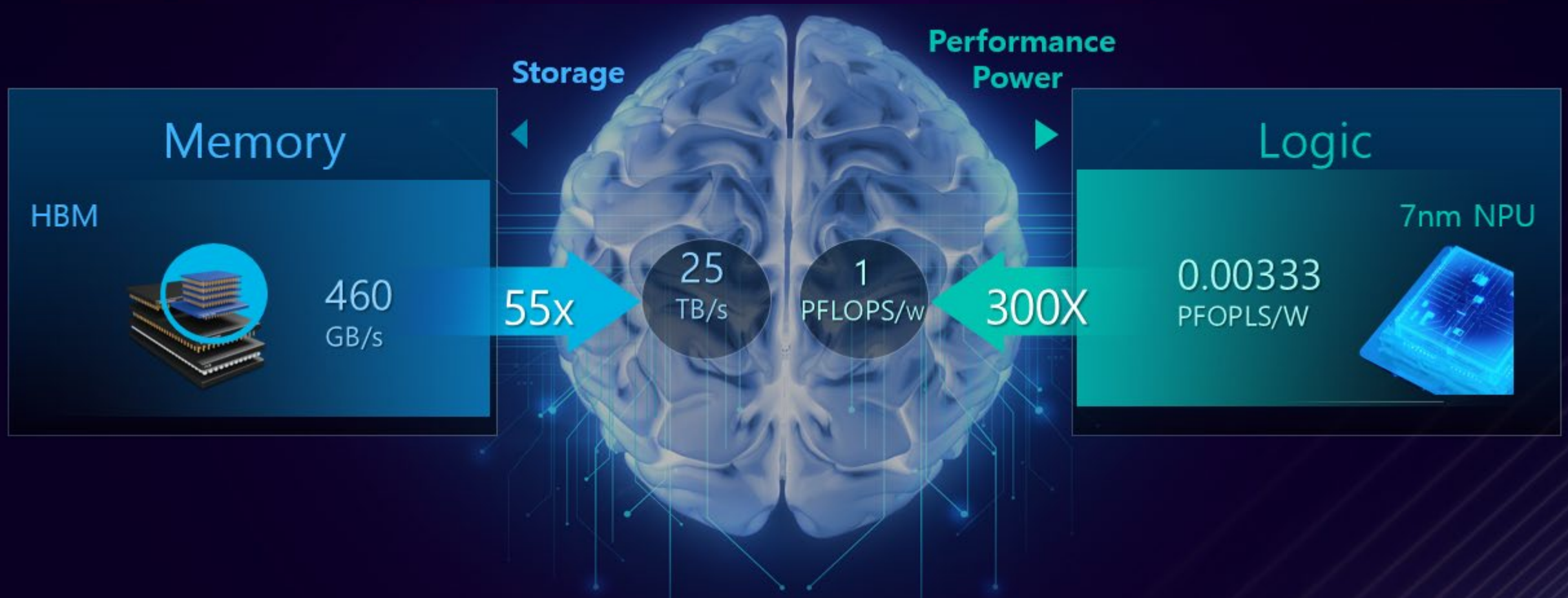


Source : Sevilla et al., 2023, Our World In Data

SAMSUNG

Semiconductors vs. the Human Brain

- The human brain far exceeds the current level of logic and memory semiconductors
- Logic/Memory semiconductor innovation is needed for AI growth



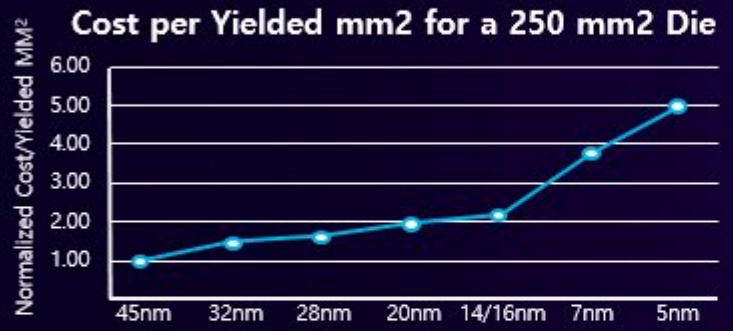
2024 Heterogeneous Integration Roadmap (HIR)

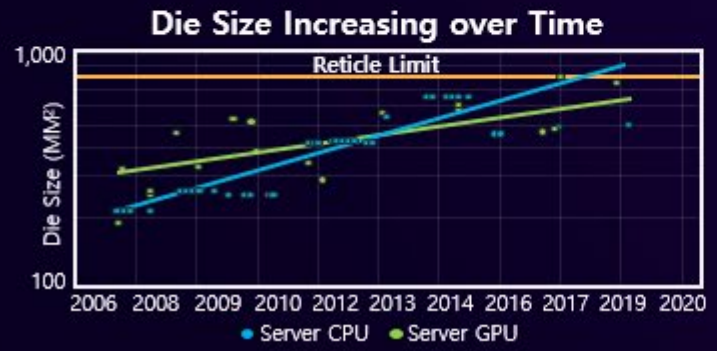
Logic Performance Innovation : Rise of HI

- Overcoming Cost/Performance challenges with 'Beyond Moore' Adv. PKG solutions

Cost Challenge

Manufacturing costs continue to increase in advanced process technology era

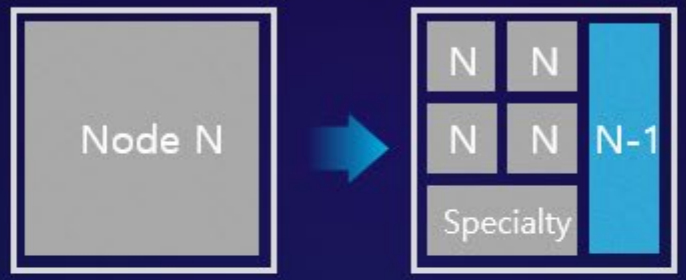




(Source: AMD, Hotchips 2019)

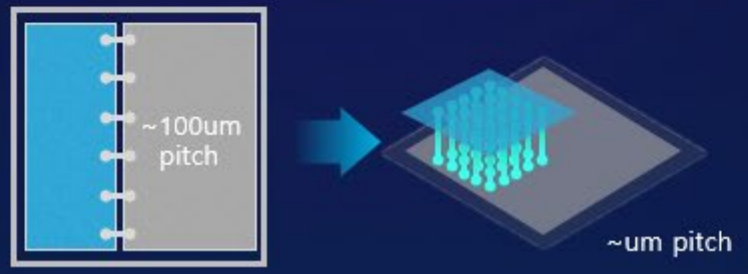
Beyond Moore Solution

High yielding smaller chips and optimal process selection



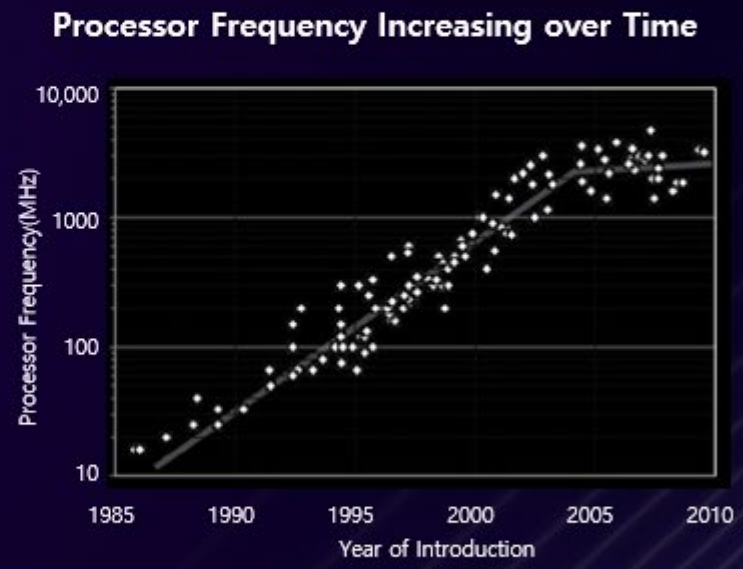
Heterogeneous Integration w/ Advanced Package

Fine pitch & massive interconnect



Performance Challenge

Moore's law slowdown due to technological difficulties



(Source: Intel CPU Trend, Wikipedia)

2024 Heterogeneous Integration Roadmap (HIR)

SAMSUNG

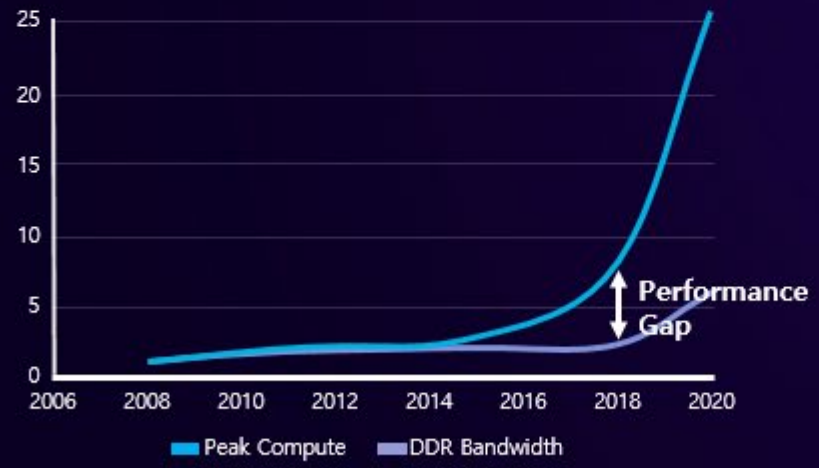
Memory Bandwidth Innovation: Rise of Adv. PKG

- Overcoming the Logic-Memory bandwidth gap through Adv. PKG integration

Memory BW Challenge

Memory Bandwidth acts as system performance bottleneck

Performance Growth Compute vs. DDR Bandwidth



Logic-Memory BW Improvement

Heterogeneous Integration w/ Advanced Package

Signal Path	~ 10cm	~ cm	~ mm	~ um
I/O #	8	64	1,024	>>1,024
B/W	~5.6GB/s	~76.8GB/s	~1TB/s	>>2.5TB/s

2024 Heterogeneous Integration Roadmap (HIR)

SAMSUNG

Contents

Samsung AVP Solutions for AI : HPC Roadmap

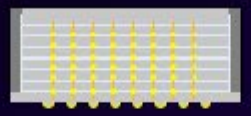
SAMSUNG

Tech Ready — MP Ready

Platform	'23	'24	'25	'26	'27	'28

Memory
* High Stack

TCB HBM 12H



24.4Q HCB HBM

HCB HBM 16H — 26.1Q

LLC — 25.4Q

*Buffer : Logic Process

2.xD PKG
* Interposer Size

2.5D 2xHBM 20.4Q MP

Wafer Process

24.1Q 2.5D 8xHBM Si Int (≤2800㎟) — 24.3Q

Si Interposer

3.5D — 25.1Q

3.5D 8xHBM 2.5D + 3D Logic

Panel Process

24.3Q 2.3D

2.3D 12xHBM RDL+Bridge (>2800㎟) — 3.3D — 26.2Q

3.3D 12xHBM RDL+Bridge (>2800㎟)

Si Bridge(<2/2um)

RDL Interposer(L/S≥2/2um)

RDL Interposer — Si Bridge

24.4Q ISC

3D PKG
* Fine Pitch

23.4Q 3D TCB — 24.4Q 3D HCB

3D TCB >20um Pitch

3D HCB 4um Pitch

* TCB : Thermo-Compression Bonding
* HCB : Hybrid Cu Bonding
* LLC : Last Level Cache
* RDL : Redistribution Layer

2024 Heterogeneous Integration Roadmap (HIR)

SAMSUNG

HBM Roadmap

- Increased needs for HPC/AI applications call for high-stack, high-performance HBM

  1) HBM3 12H world first mass production (’23.7~)

  2) HBM4 16H HCB technology in development

  3) HBM4 customized HBM in development

2024 Heterogeneous Integration Roadmap (HIR)

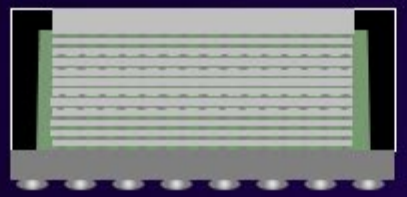
HBM-TCB Technology

- TCB HBM-12H in mass production (‘23), HBM-16H sample developed

MR-MUF
Mass Reflow-Molded Underfill

vs.

Samsung Technology
TCB-NCF
Thermo-Compression Bonding
Non Conductive Film



Samsung Exclusive Material & Equipment

NCF Material
- Thinner Hybrid NCF

CoW Bonder
- High Accuracy & Chip Tilt Control

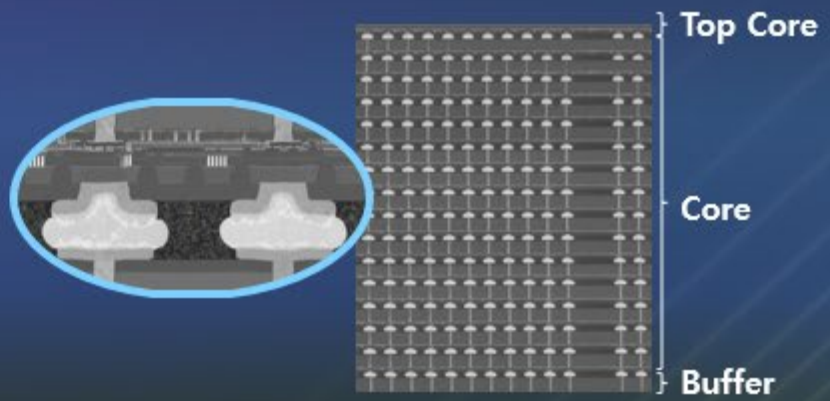
Advantages of TCB

Joint Thermal Resistance
Up to **35%** ↓
vs MR-MUF
- Higher Bump Density
- Less Joint Gap

Chip Thickness for High-Stack
Up to **15%** ↑
vs MR-MUF
- Less Joint Gap

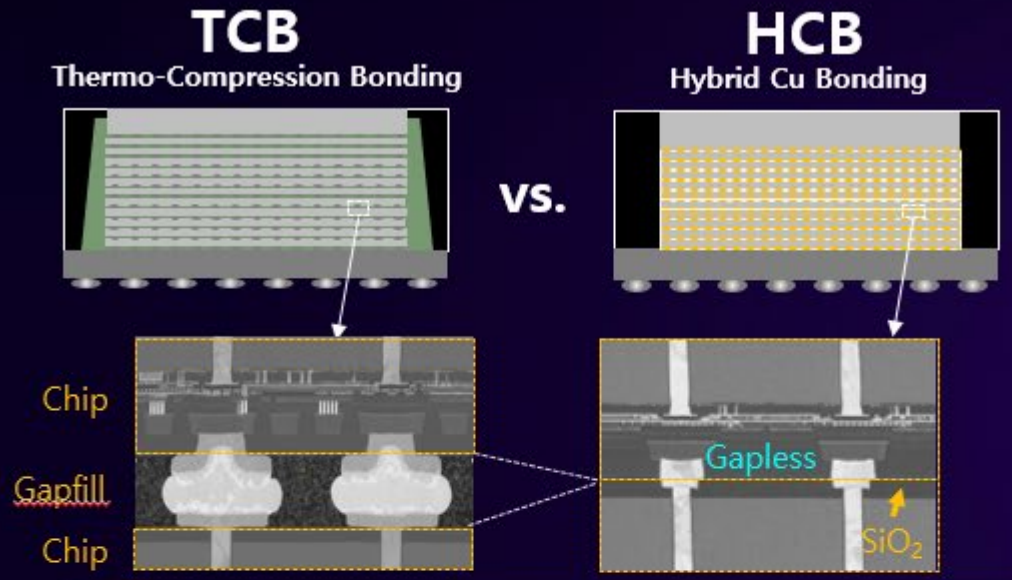
TCB HBM-16H Sample (2023)

DC Yield > 9x%



HBM-HCB Technology

- HBM 12H function sample developed with HCB (’23), 16H D/C sample developed



Samsung Exclusive Equipment & Technology

HCB Bonder

- High accuracy & chip tilt control
- Facilities internalization by Samsung

µ-Particle control

- Class 1 facilities
- Protection layer coating

BEOL Metal design for HCB

- Surface topology control
- Cu pad expansion control

Advantages of HCB

High-stack

Up to **33**[1)] **%** vs TCB

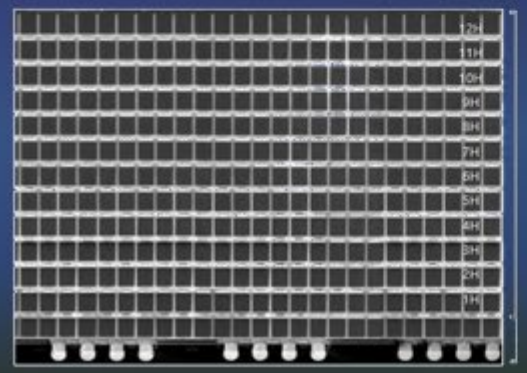
PKG Thermal Resistance

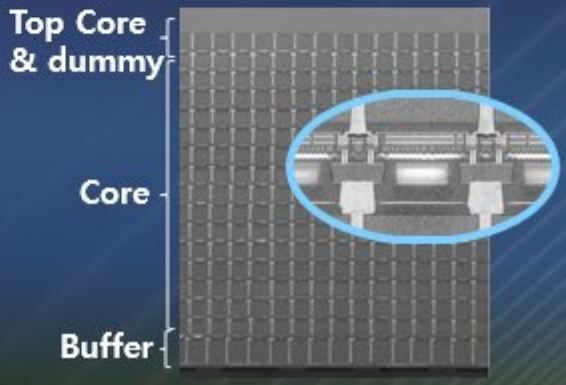
Up to **20%** vs TCB

1) Same Chip & HBM PKG Thickness

12H Function Sample (2023), 16H D/C Sample (2023)

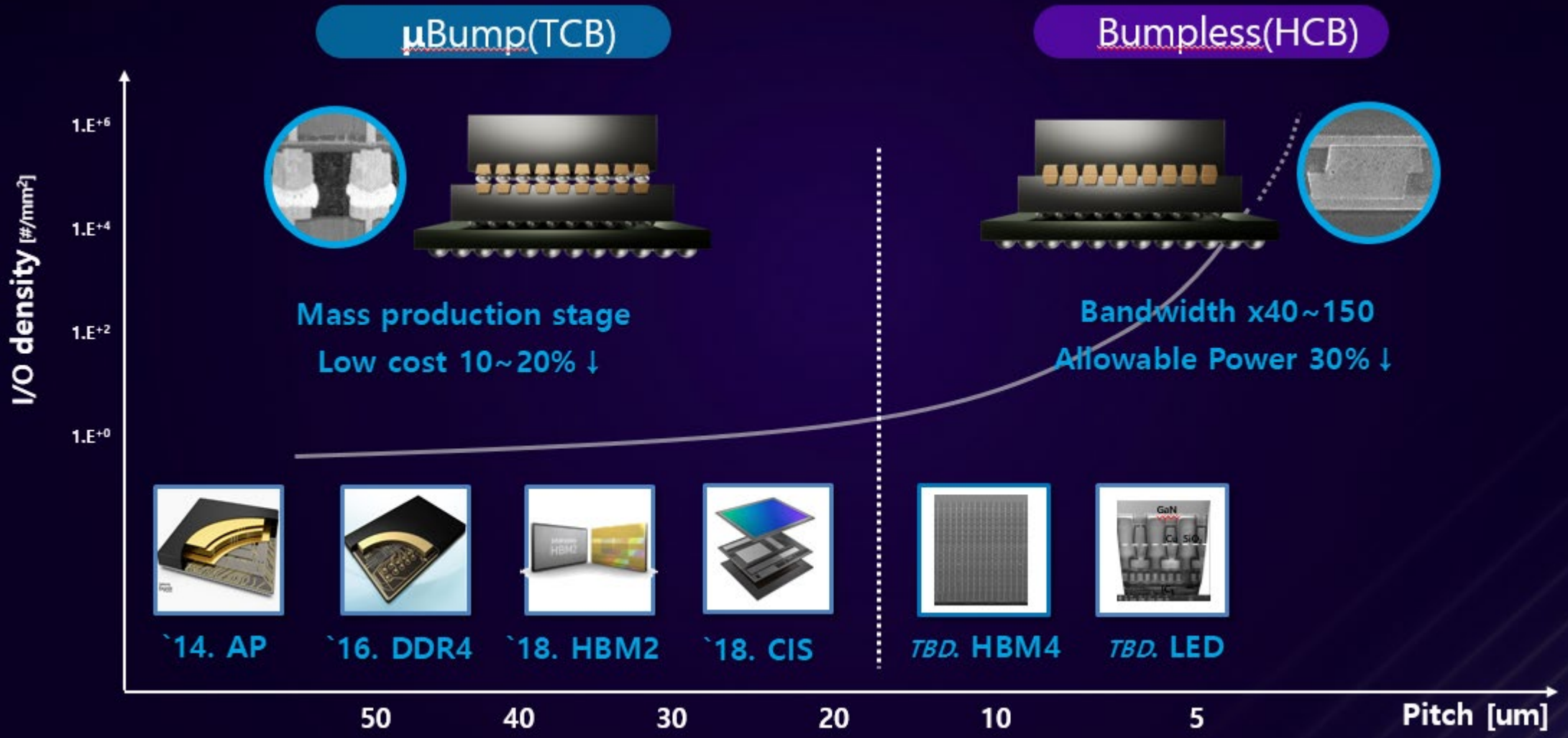
(Presented at ’23 ECTC)





AVP History for 3D Logic Stacking

- High I/O density and fine pitch development required for HPC/AI applications



2024 Heterogeneous Integration Roadmap (HIR)

3D Logic Stacking Roadmap

- 3D logic readiness through technology verified in memory mass production

		2023	2024	2025	2026	2027 -
TCB 	Bump Pitch	24 um	21 um		18 um	<15um (`28~)
	IO density (Bump/mm²)	1,736	2,267		3,086	4,444 (`28~)
	PDK		SF5/4		SF3P/2	
	Mass Product.[1]		AP, XR[2]			TBD

		2023	2024	2025	2026	2027 -
HCB 	PAD Pitch	4 um		2.5 um		≤ 2 um
	IO density (Pad/mm²)	62,5K		160K		>250K
	PDK					SF3P/2
	Mass Product.					AP, HBM[2]

1) '16 HBM2, '18 CIS-3Stack MP 2) Mass production ready

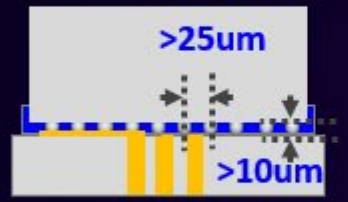
2024 Heterogeneous Integration Roadmap (HIR)

3D Logic Stacking-TCB **Technology**

- 25um pitch ready for mass production through TCB-NCF technology

TCB-NCF

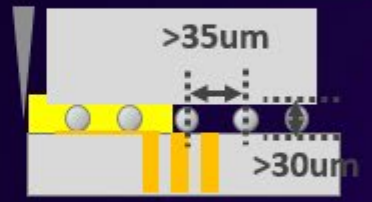
Thermo-Compression Bonding
Non Conductive Film



vs.

MR-CUF

Mass Reflow-Capillary Underfill



Samsung MP Proven Tech.

Process & Material

- TC Profile &
  NCF Viscosity control

Infra

- Exclusive tool
- Equip. Compatibility

Advantages of TCB-NCF

High IO density, Low Thermal Resist.

Up to

x2 ↑ IO count

5% ↓ Tj[°C@AP]

- Fine Pitch
- Less Joint Gap

High Productivity

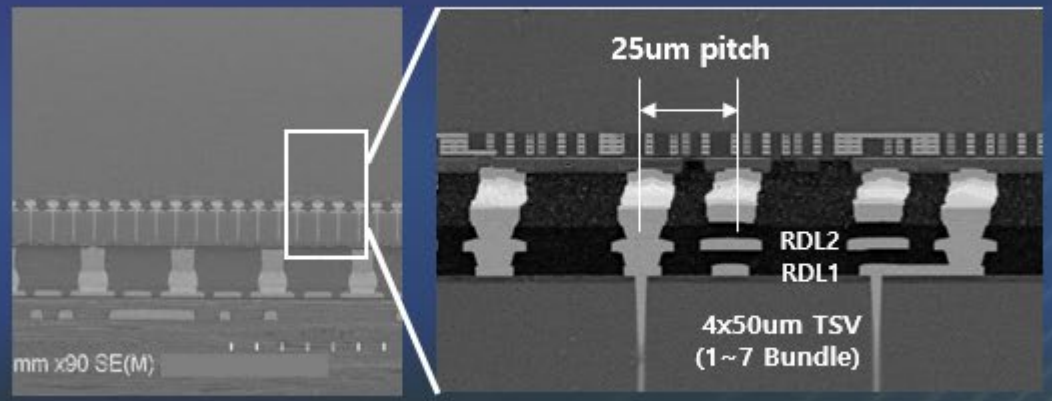
Up to

13% ↓ Assy. step

- Less Process step
- MP Proven

25um Pitch MP ready (`23)

for Adv. Node Device (SF3/2, `24 PDK release)

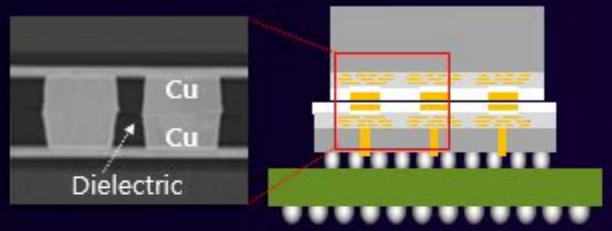


SAMSUNG

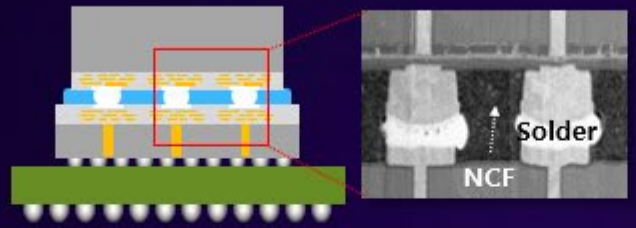
3D Logic Stacking-HCB Technology

- 3um ultra fine pitch technology verification complete

3D HCB
(3㎛ Pitch, Joint Gap 0㎛)



3D TCB
(25㎛ Pitch, Joint Gap 12㎛)



Samsung Exclusive Process

Process & Tool
- High precision alignment & bonding

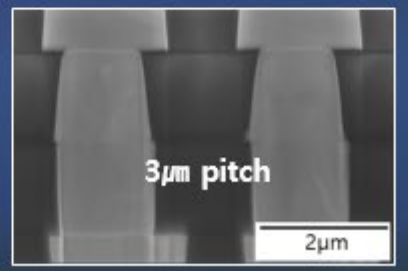
Structure
- Thin bottom structure without Thermal dummy

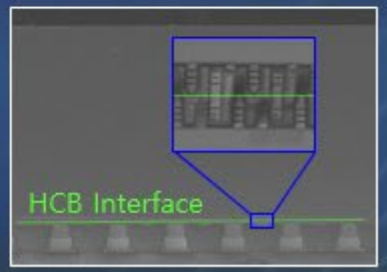
Advantages of Samsung's 3D HCB

I/O Density
Up to **X70**
3㎛ vs. 25㎛ Pitch

Allowable Power
Up to **33%**
vs. μ-bump

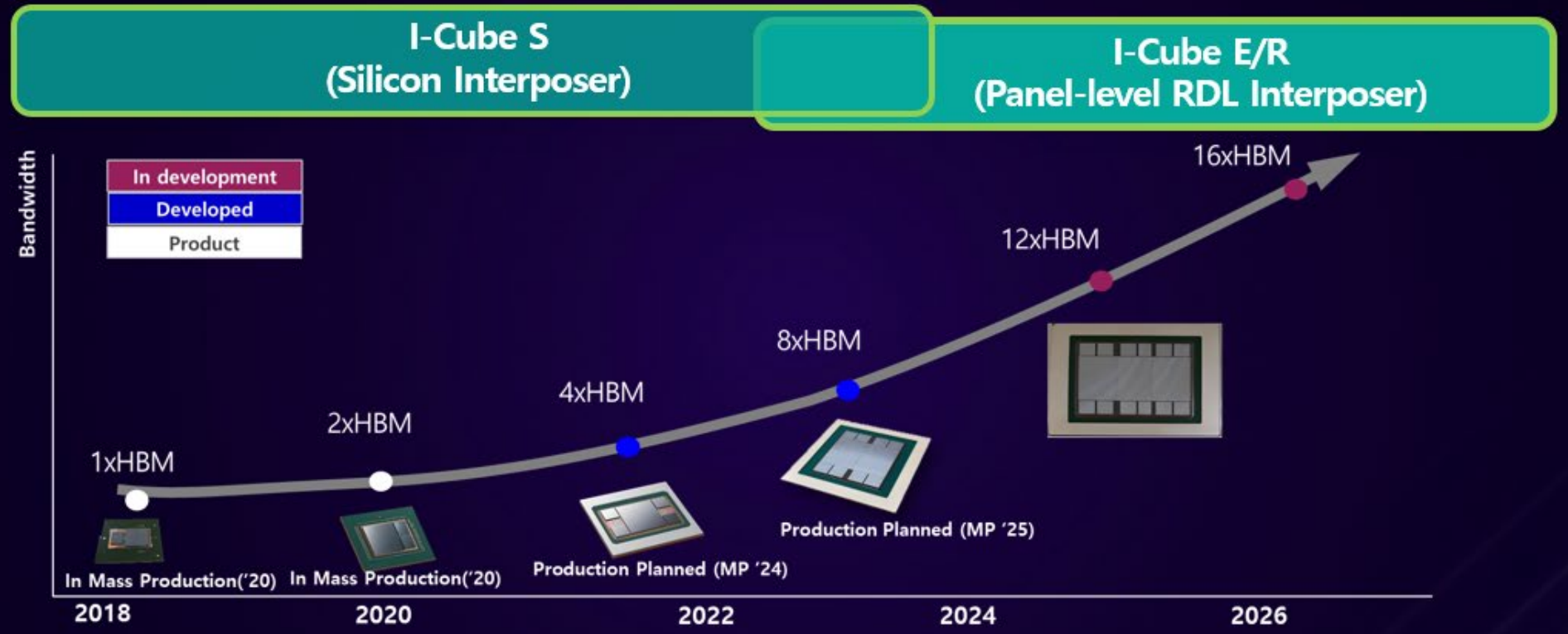
3um Ultra Fine Pitch Feasibility(`23)
for Adv. Node Device (SF4/5, `26 PDK release)





I-Cube Roadmap

- I-Cube enables larger interposer, more HBMs and multi-die for AI/Date center applications

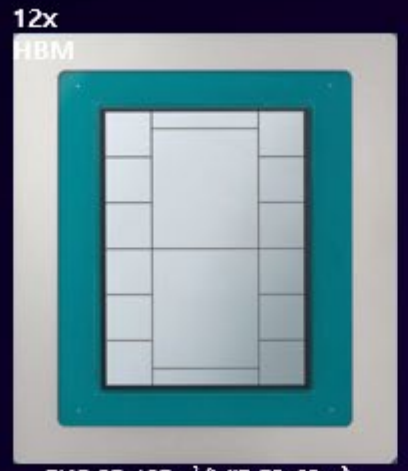


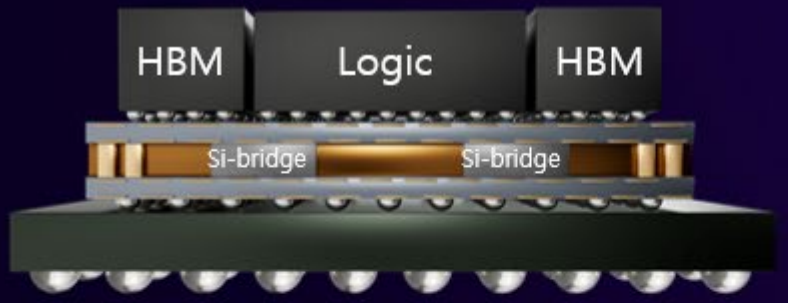
	2022	2024	2026	
Interposer Size (Reticle)	2x	3.3x	4x	6x
PKG Size	65x65 mm²	85x85 mm²	100x100 mm²	130x130 mm²
ISC Cap density	1500nF/mm²	2200nF/mm²	2750nF/mm²	4400nF/mm²

2024 Heterogeneous Integration Roadmap (HIR)

I-Cube E Technology

- I-Cube E is the cost-effective PKG solution with panel level technology





Samsung I-Cube E Platform

- **Cost Efficiency + Expandability** — Si Interposer → Si Bridge + RDL

Si Interposer Net Unit 12ea/Wf
※ 12xHBM (51x68㎟)

Si Bridge Net Unit 1,060ea/Wf
※ Si-Bridge 8.7x6.6㎟ (13 ea/PKG)

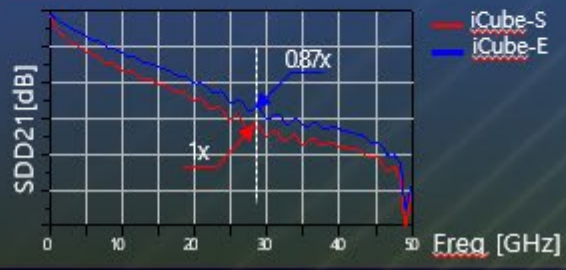
- **Productivity** — Wafer Level → Panel Level

12ea/Wf

>36ea/Wf

- **Performance** — Low Loss @ SerDes 112G

Loss(SerDes 112G) : TSV > Cu Post w/ EMC
※ HBM3E 8Gbps & Adv UCIe 32Gbps is equivalent



SAMSUNG

Contents

Samsung AVP Solutions for AI : Mobile Roadmap

SAMSUNG

Tech Ready — MP Ready

Platform	'23	'24	'25	'26	'27	'28

Memory
* # of I/O, BW

LPDDR5

LPDDR6
WB, x96

LPW
25.1Q

LP Wide I/O
VCS, x512

2D PKG
* Thermal
Fine Pitch

2D FO-WLP
7/8㎛RDL, Mono Die
23.1Q — 23.4Q

2D FO-WLP
HPB
24.4Q

2D FO-WLP
≤5/5㎛RDL, Multi-Die
25.4Q

3D FO-WLP
HCB 4㎛ Bump Pitch

3D PKG
* Fine Pitch

3D TCB
23.4Q

3D HCB
24.4Q

3D TCB
>20 ㎛ Pitch

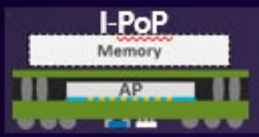
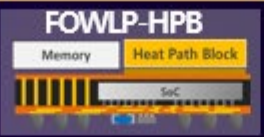
3D HCB
4 ㎛ Pitch

* WB : Wire Bonding
* VCS : Vertical Cu Post Stack
* HPB : Heat Patch Block

SAMSUNG

Fan-Out PKG Roadmap

- FOWLP with chip last & double sided RDL is in mass production for mobile AP (`23~)
- Key technologies are under development for On-Device applications such as mobile AP and LPW memory.

			~2022	2023	2024	2025	2026	2027
Architecture	Mobile AP	Structure						
		Heat resist.	x 1.00	x 0.85		x 0.55		
		UCIe I/O					x 16	x 32
	LPDDR	Structure						
		I/O density	x 64				x 512	
Tech.	Si thickness		110um	215um		Heat Path Block		
	Double Side RDL		7/8um	2/2um		1/1um		
	Cu Post AR			2.2:1		≥6:1		

2024 Heterogeneous Integration Roadmap (HIR)

Fan-Out PKG Technology for Mobile AP

- Samsung's Fan-out PKG with Advantages for TAT, Architecture and Thermal Performance.

Chip First-S.RDL
Single-sided RDL

Chip Last-D.RDL
Double-sided RDL

SAMSUNG's

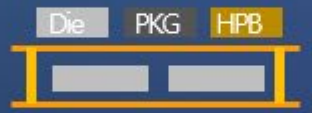
Samsung MP Proven Processes

Chip Last
- Samsung's CoW technique

Double-sided RDL
- Unique tape carrier (exclusive)
- High AR Cu Post process

Advantages of Chip Last-D.RDL (AVP)

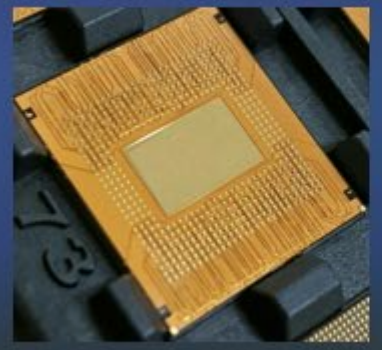
Process TAT
Up to
x33% ↓
vs Chip First/D.RDL
- Pre-made F.RDL

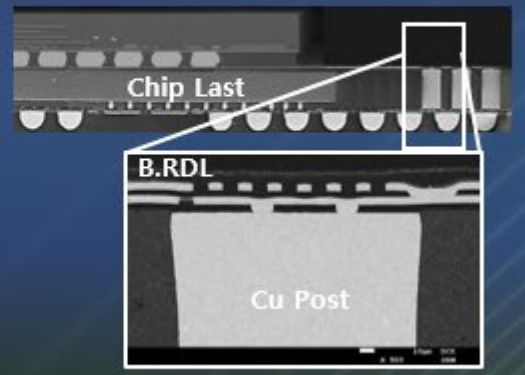
Architecture Flexibility


vs S.RDL
- Back side RDL

Heat resistance
Up to
x45% ↓
vs I-PoP
- Heat path block

FOWLP Mobile AP MP(`23)





SAMSUNG

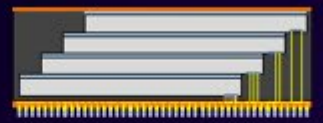
Fan-Out PKG Technology for Low Power Wide I/O Memory

- FOPKG with Vertical Interconnection of multi-die stacks enables to increase I/O density & BW.

Wire Bonding

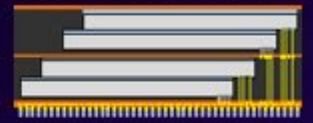
FBGA

Vertical Interconnection



VWB

* VWB : Vertical Wire Bonding



VCS

* VCS : Vertical Cu Post Stack

Samsung's New Architecture & Process

Cu Post

- High AR Cu Post ≥6:1(`24)

RDL/Bumping

- Wafer Level Fine Pitch RDL & Bump Process (MP Ready)

Advantages of VCS (AVP)

I/O Density, Band Width

Up to **x8** ↑ vs FBGA

Up to **x2.6** ↑ vs FBGA

- Finer pitch (≤60um)
- High AR Cu Post (≥6:1)

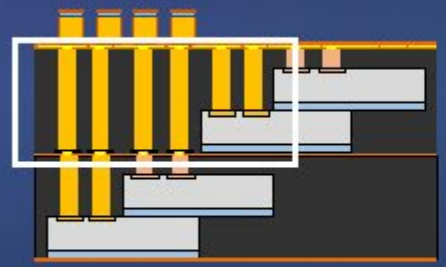
High Productivity

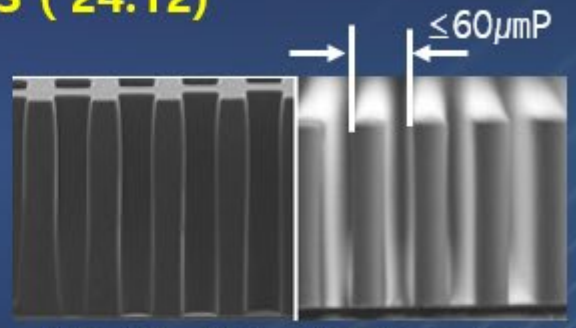
Up to **x9.0** ↑ vs VWB

- Shorter process time (≥ I/O x256)

* Wire bond → Cu Post

VCS FS ('24.12)





【PR A/R≥ 6:1】 【Cu Post ≤60μmP】

SAMSUNG

Contents

Heterogeneous Integration Eco System

- Overcoming semiconductor technology challenges through collaboration between Samsung AVP's HI platforms and our partners' specialized expertise

EDA Design methodology

cadence, SYNOPSYS

P&R, PEX, PSI, STA, DFT

ANSYS, SIEMENS

IR-Drop, EM Verification

Chiplet IF Including memory

UCIe, JEDEC, SAMSUNG Foundry, cadence, SYNOPSYS

Samsung AVP HI Platform

OSAT Cooperation

Amkor Technology, ASE, JCET

PCB & More Supply Chain

IBIDEN, KYOCERA, SAMSUNG ELECTRO-MECHANICS, SHINKO, TOPPAN

Samsung AVP R&D Across the Globe

- Multiple portals for research and development collaboration between Samsung and Partners

SAMSUNG

Thanks

- Introduction
- Samsung AVP Platform Solutions
  - HPC / AI
    - HBM
    - 3D Logic
    - I-Cube
  - Mobile AI
    - Mobile AP
    - Low Power Wide I/O Memory
- Heterogeneous Integration Eco System