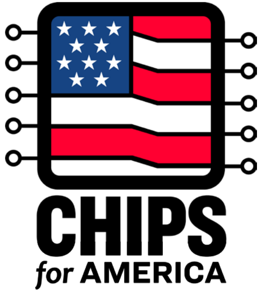
National Advanced Packaging Manufacturing Program

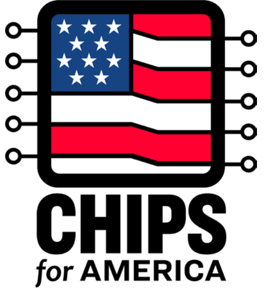


Subramanian Iyer

January 23,2024

NIST
NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

Disclaimer

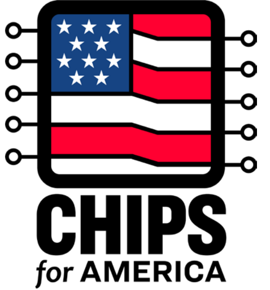


Statements and responses to questions about advanced microelectronics research and development programs in this webinar:

- Are informational, pre-decisional, and preliminary in nature.
- Do not constitute a commitment and are not binding on NIST or the Department of Commerce.
- Are subject in their entirety to any final action by NIST or the Department of Commerce.

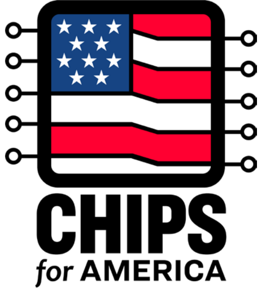
Nothing in this presentation is intended to contradict or supersede the requirements published in any future policy documents or Notices of Funding Opportunity.

Agenda



- Opportunities in Advanced Packaging
    - Context
    - Background
- NAPMP vision, mission, and outcomes
- NAPMP investment areas
- Upcoming funding opportunities

The Role of the package



Mechanical protection
- Handling
- Stability

Environmental protection
- Moisture
- Hermeticity
- Corrosion

Thermal protection
- Heat spreading
- Heat sinking
- Hotspot reduction

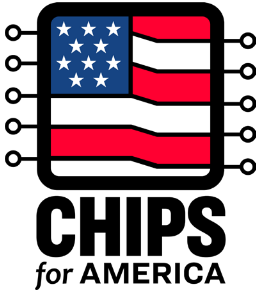
To protect and to serve

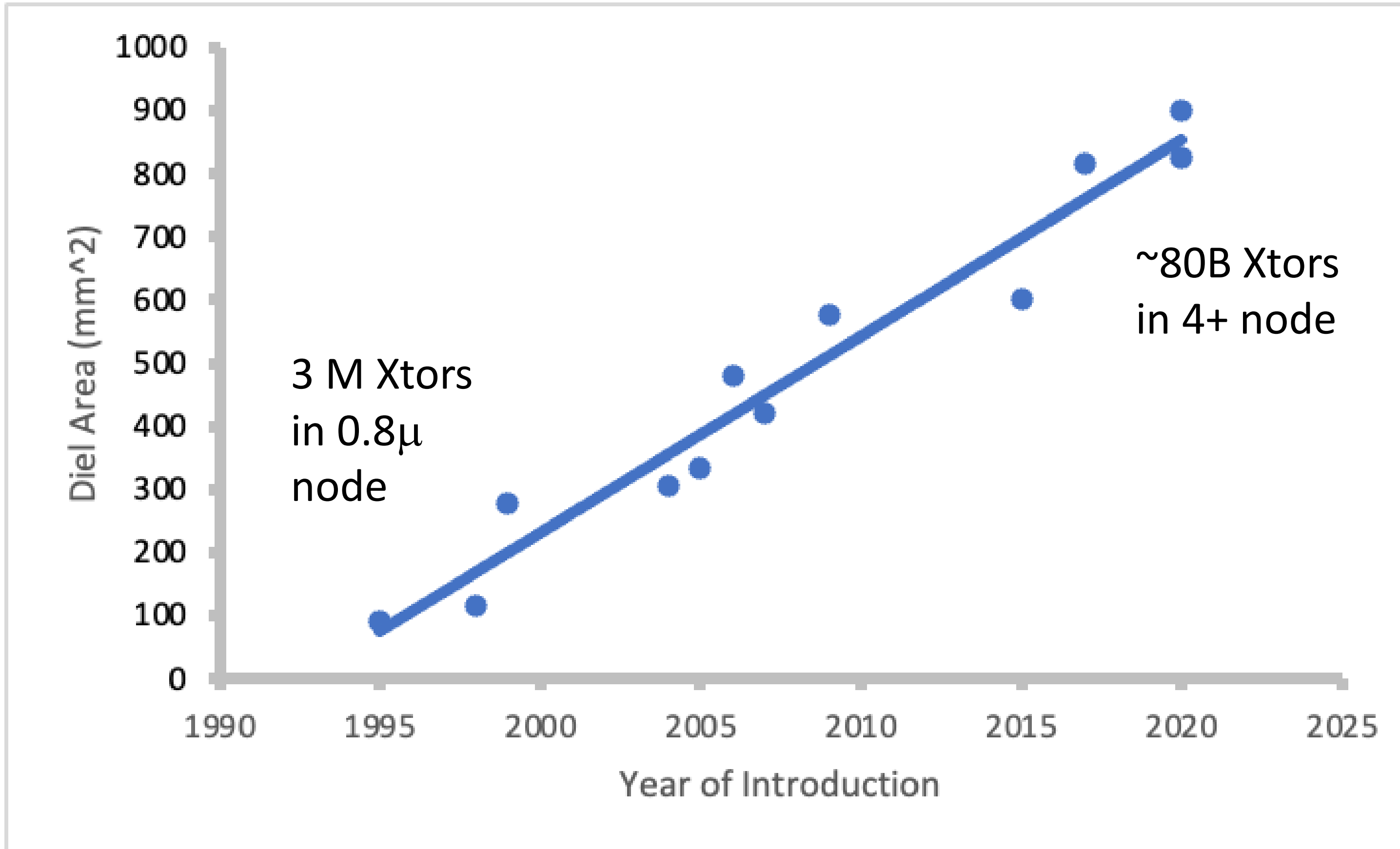
Connect electrically to other chips

Deliver power

Stable test and integration platform

Even though transistors have scaled dramatically, die sizes have grown larger





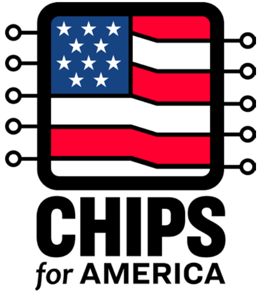
This chart shows past and current die size scaling trend

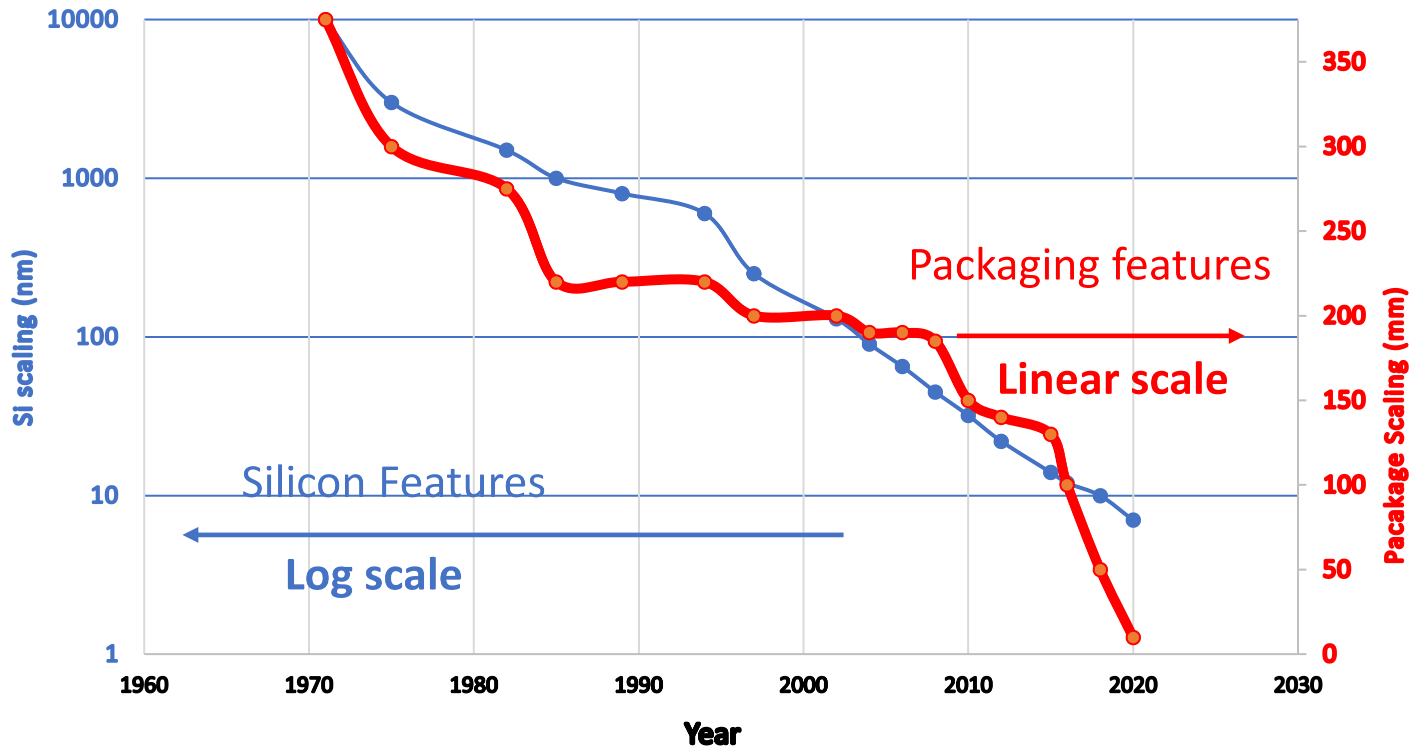
- Monolithic dies still outperform multi-chip packaged assemblies
  - Because packaging scaling has not kept up with silicon scaling (~10X Vs 10^6 X)
  - But high-performance dies have reached reticle limits
- Packaging is evolving to emphasize system integration rather than single chip packaging with the increasing adoption of silicon processing techniques

PACKAGING CHIPS for AMERICA

**Die size data from commercial product spec sheets*

Packages have not scaled significantly over the last five decades when compared to silicon CMOS scaling





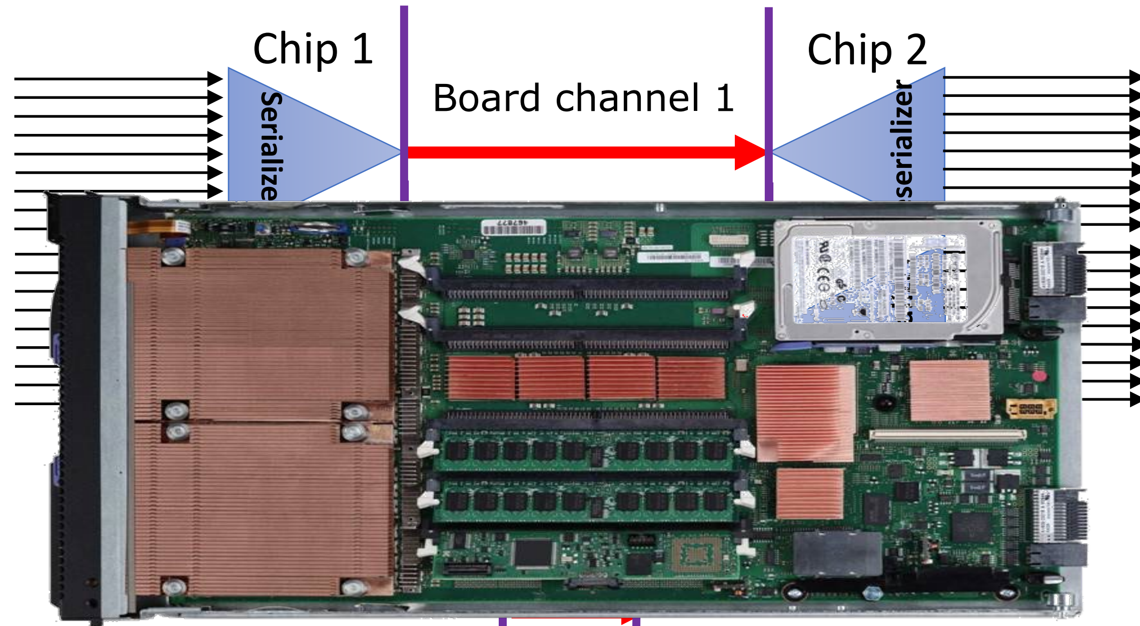
- The last five years have seen an improvement in the scaling of package features.
- This has been possible because of the use of silicon technology including silicon substrates for packaging
- Even so, package features are quite large when compared to even coarse silicon features

This chart shows the past, present and future trend of transistor and packaging feature size scaling.

Jangam and Iyer, T-CPMT (2019)

Heterogeneous integration is not new

The difference now is scale:



Lower power, lower latency and higher bandwidths

Simper I/Os, more useful chip area

- More Channels on the package
  - Finer "bump/pillar" pitch
  - Approach on-chip via pitches (<1 µm)
- Finer Trace Pitch
  - Approach on-chip wiring pitches
- Shorter inter die distance
  - ~ µm

Scale Down

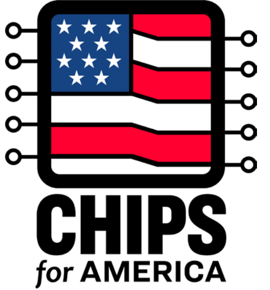
- Significantly more intimately connected Silicon

Scale Out

PACKAGING CHIPS for AMERICA

CHIPS for AMERICA

Advanced packaging blurs the line between a monolithic chip and a packaged assembly of heterogeneous chips



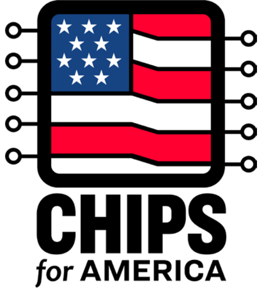
Scaling down features on the package:

- Making the features on the package approach those at the top level on a monolithic CMOS chip
- Connecting the dies to the package at pitches approaching the final via pitches on a chip
- Reducing the distance between dies that are assembled on a multi-chip package to approach the distance between IP blocks on a monolithic chip

Scaling out the package

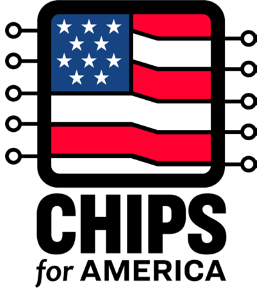
- Accommodate a larger number of closely packed heterogeneous dies
- Address the power delivery, thermal dissipation and external connection challenges
- Develop standards and protocols to accommodate this large and diverse set of chips (chiplets)

Chiplets and Dielets



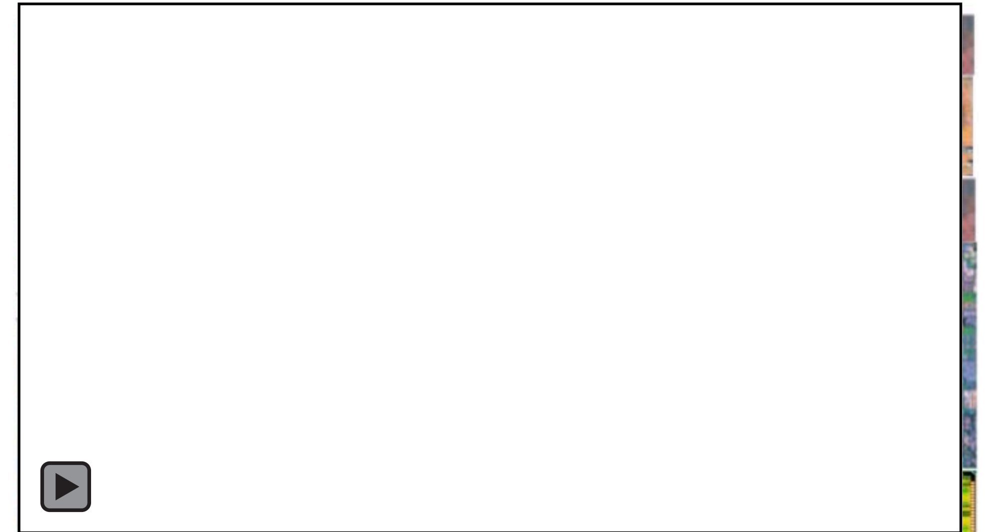
- Chiplets are relatively small (a few mm on a side) designs
  - Chiplets are not just small chips; they need to be closely connected to other complementary chiplets to function
  - Mechanical and electrical standards are crucial
- Chiplets may be designed in diverse technologies
- Chiplets may not be independently functional
- Chiplet designs are fabricated and singulated into dielets
- Many dielets are integrated (physically and electrically) on an interconnect fabric (substrate)
- The integrated assembly has more functionality at lower power with potentially higher yield with lower NRE costs and shorter time to market

Advanced packaging allows us to change the way we put complex systems together



Adapting SoC methods to packaged systems[1]

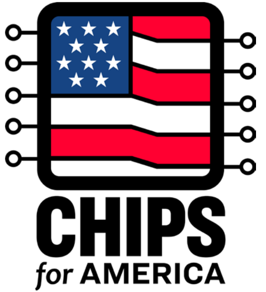
- IP blocks transformed into hardware verified dielets[2] (chiplets)
- Bare dielets stacked (3D) or integrated side by side at fine pitch on an Interconnect Fabric (substrate)
- Dielets are heterogeneous
- A simpler and flatter hierarchy is possible



PACKAGING CHIPS for AMERICA

[1]S.S. Iyer T-CPMT (2016)
[2]"Dielets" were defined earlier.

But today's packages are incredibly complex and costly



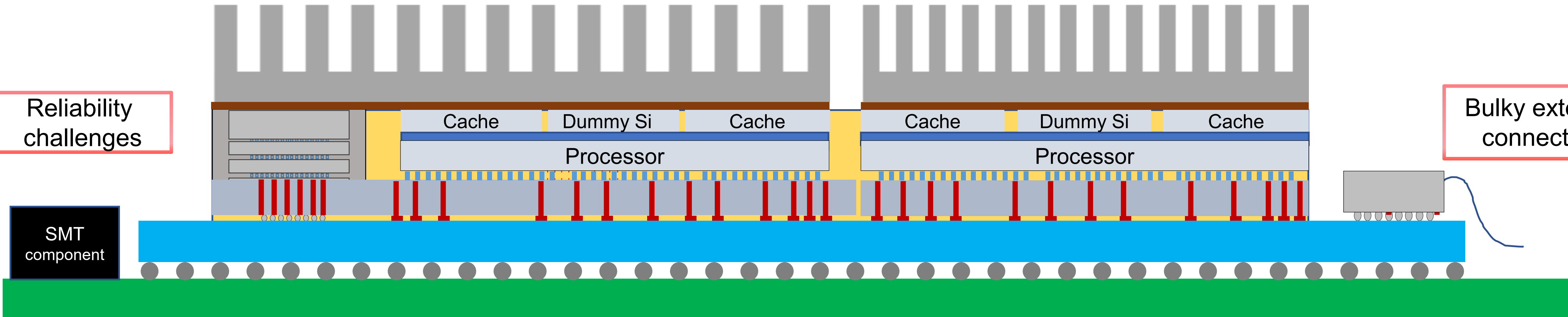
Known good die, testing and rework challenges

Materials with large CTE mismatches and high stresses

Thermal and hot spot challenges
Power delivery challenges

Reliability challenges

Bulky external connectors



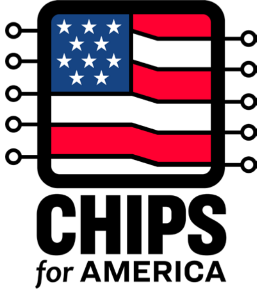
Increasingly complex hierarchies (e.g.: interposers) and assembly techniques

Organic substrates and laminates with large warpage and coarse pitches with embedded and SMT passives and expensive interposers

Simplify packaging and make it cost effective to manufacture in the US

CTE: coefficient of thermal expansion; SMT: surface mount technology

Establishing Advanced Packaging in the US



Packaging Roadmaps

- NIST sponsored roadmaps: MRHIEP, MAESTRO and MAPT
- Other roadmaps: HIR and IRDS

Technology Development Thrusts

- All aspects of technologies required to develop a leading-edge on-shore advanced packaging manufacturing capability

The Advanced Packaging Piloting Facility (APPF)

- Validates & practices NAPMP thrusts
- Piloting and prototyping functions

The Chiplet and Design Ecosystem

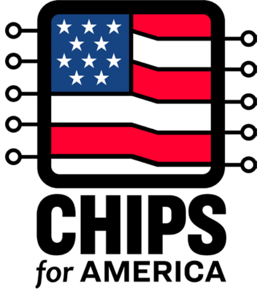
- Chiplet discovery, disaggregation and reaggregation methodologies, protocols, standards, fabrication and warehousing design for test, repair and reliability and holistic design tools and methodologies

Design in the U.S., build in the U.S., and Sell Worldwide

- Product-like prototyping exercise to be built and "qualified" in the APPF

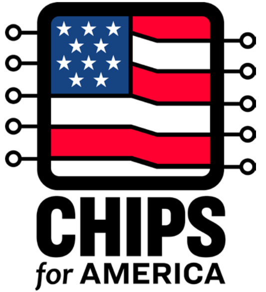
PACKAGING CHIPS for AMERICA

Road mapping is very important



- Heterogeneous integration roadmap (available at IEEE EPS website)
- SRC Microelectronics and Advanced Packaging Roadmap (available at SRC website)
- iNEMI 5G/6G mmWave Materials and Electrical Test Technology Roadmap (available at iNEMI website)
- Manufacturing Roadmap for Heterogeneous Integration and Electronics Packaging (available at the UCLA CHIPS website)

NAPMP Structure: six hardware and eco-system thrusts + piloting facility + prototyping challenges



Substrates & materials are the platform for heterogeneous integration of dielets

Equipment, tools & processes are needed to pattern substrates and assemble dielets and passivate assemblies

Thermal management and efficient power delivery are critical needs

Photonics and connectors allow the assembly to interact with the outside world

Automated design for test, repair, security, and reliability; substrate and process dependent

Materials and substrates

Equipment, tools and processes

Power delivery, thermal management

Photonics and connectors

Co-design, EDA

Chiplet ecosystem

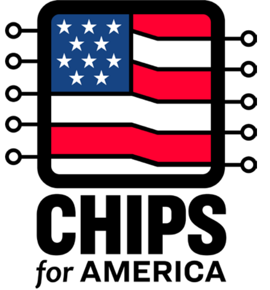
Advanced Packaging Piloting Facility

The NAPPF provides a test bed for integration of the different investment areas and also functions as a piloting and prototyping facility

The chiplet eco system is crucial for any implementation of advanced packaging

NAPPF:national advanced packaging piloting facility

Materials and Substrates

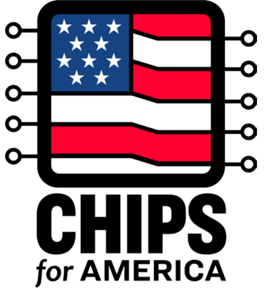


"The key requirements of new substrates include multiple levels of fine wiring and via pitches, low warpage, large area, and the ability to integrate active and passive components."

- Materials and substrates are the platform on which advanced packaging is built.
- These substrates or interconnect fabrics (IF) may be based on silicon, glass, or organic materials and can include fan-out wafer-level processes.
- The IF needs to be
  - compatible with advanced and legacy nodes and different semiconductor material systems
  - have integrable active and passive components
  - compatible with either mass reflow, thermal compression bonding or hybrid bonding
- Meet environmental and sustainability goals

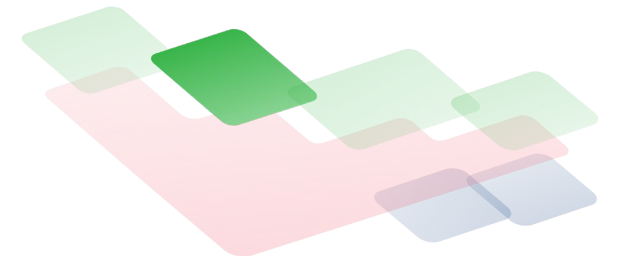
PACKAGING
CHIPS
for AMERICA

Equipment, Tools, and Processes



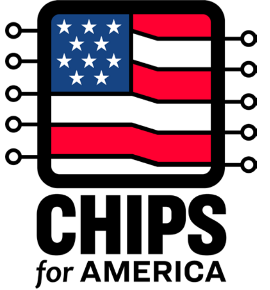
"Advances in equipment, tools, and processes are required, in conjunction with and compatible with advances in materials and substrates"

- To achieve goals in reducing patterned feature sizes on large areas, including through substrate vias as well as strategies to reliably assemble chiplets onto these finer substrates and passivate them.
- We expect that CMOS equipment and processes will be adapted to handle dies, wafers, and panels as appropriate.
- We expect the APPF to benefit from developments in equipment, tools, and processes.



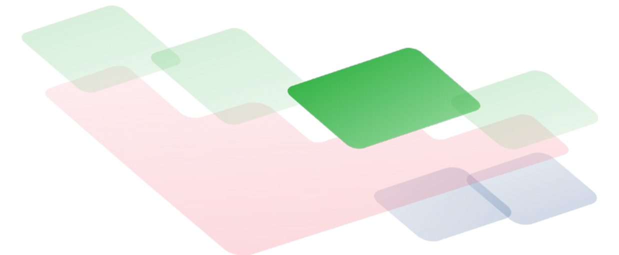
PACKAGING CHIPS for AMERICA

Power Delivery and Thermal Management

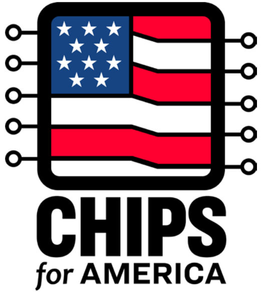


"These activities will require new thermal materials as well as novel circuit topologies that employ advanced substrates and heterogeneous integration."

- Advanced packaging makes severe demands on power density and can restrict heat spreading.
- Heterogenous integration will require multiple voltage domains and high granularity. Power delivery will likely require wide bandgap materials integrated into the substrate.
- This thrust will focus on the development and evaluation of innovative materials and solutions that are compatible with the materials, substrates and assembly processes used.
- Modeling and optimization to achieve high efficiency is a must.



Photonics and Connectors

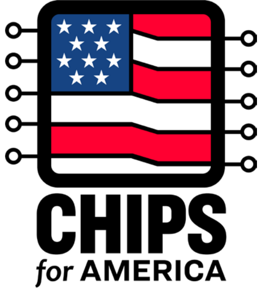


"The focus will be on reliable and manufacturable integrated connectors that include computational capability, data pre-processing, security, and ease of installation to the packaged assembly."

- Packaged assemblies to interact with other assemblies and the outside world (a few centimeters to several meters)
- Connectors can be wired, RF, and optical

PACKAGING CHIPS for AMERICA

Chiplet Ecosystem



> "Chiplet discovery methodologies will be developed to ensure a high level of reusability, design, and warehousing of these chiplets."

- The vision of advanced packaging relies on the availability of high reuse chiplets
  - this has not yet happened
- Chiplets need to be small and work better when connection pitches and distances are small
- Chiplet dicing and ESD-free transport
- Chiplet ecosystem requires standards and a warehousing infrastructure where bare dies are stocked
- NAPMP will focus on chiplet discovery methodologies, high value chiplet design, and integration methodologies
- Common protocols and protocol translator chiplets

PACKAGING
CHIPS
for AMERICA

The Chiplet/Dielet Golden Regime

Die yielding constraint

Mechanical constraints

Optimal pitch
2 to 10 µm

Optimal dielet size
1 to 100 mm²

Electrical/logical constraints

SerDes-like

SoC-like

Packaging-like

Die handling constraint

CMOS wire-like

50 nm
Gate pitch

Interconnect pitch

500 µm
BGA/LGA

Dielet/chiplet size (# of circuits)

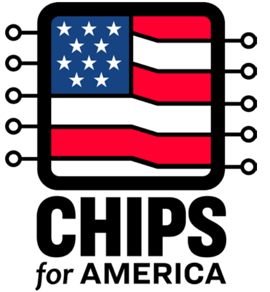
IP reuse

I/O complexity/power

Testing complexity

Iyer et al (2019)

Co-design

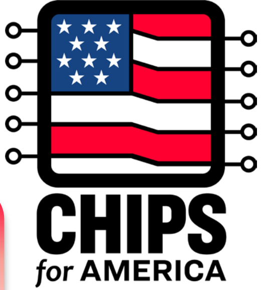


Holistic package co-design “will be adapted for advanced packaging with consideration for built-in test and repair, security, interoperability, and reliability, with a detailed understanding of the substrate and processes used.”

- The intimate connection between chiplets and advanced packaging constructs requires a co-design platform that comprehends:
  - Chiplet architectures and communication options
  - Design for test, repair, security, and reliability
  - Thermal and thermomechanical constraints
  - Substrate and assembly technology (no rework)
- The extension of chip design methodologies to advance packaging
- The NAPMP will support co-design efforts

PACKAGING CHIPS for AMERICA

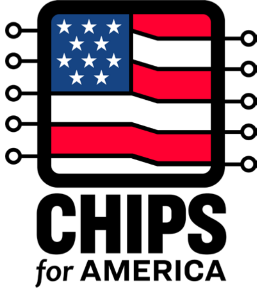
Packaging Workforce Development



"The NAPMP intends to integrate workforce education and training into all NAPMP efforts leveraging internships, co-ops, work-study programs, seminars, hands-on experiential learning, and other educational advancement activities within each investment area and in the APPF."

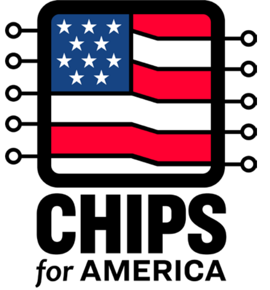
- Packaging is very interdisciplinary and requires multi-disciplinary teams
- Workforce development will be best achieved by embedding students and professionals in the thrusts and the APPF through extended internships at all levels, from vocational to doctoral

The Advanced Packaging Piloting Facility - Where it all comes together



- Investment Area Thrusts should connect activities with the APPF
- APPF will be focused on integrated process flows that can reach commercial scale
- APPF will be focused on validating new technology specifications, compatibility with other processes, yield, and reliability
- The APPF will be focused on assessing technologies for scaled transition to U.S. manufacturing

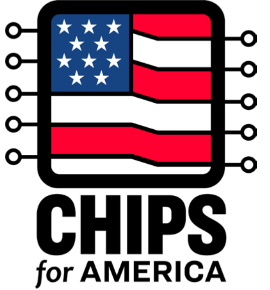
Collaboration is Critical for Success



- System houses and end users
- EDA vendors
- Chiplet designers
- Chiplet fabricators
- Materials and substrate suppliers
- Equipment and tool vendors
- Educational institutions
- Thermal and connector solutions
- OSATS and IDMs
- Prototypes

We encourage you to begin identifying your individual contributions to the ecosystem as well as partners who can help accomplish the vision and goals of the NAPMP.

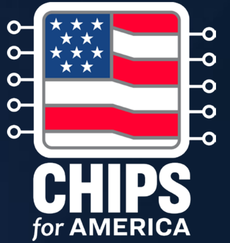
Substrates funding opportunity (~$300M)



- CHIPS National Advanced Packaging Manufacturing Program (NAPMP) Materials and Substrates Research and Development

- An in-person "Proposer's Day" meeting is being planned in the Gaithersberg Maryland area on Tuesday March 12th, 2024

PACKAGING CHIPS for AMERICA



Thank you for attending

Visit CHIPS.gov for future updates and additional information