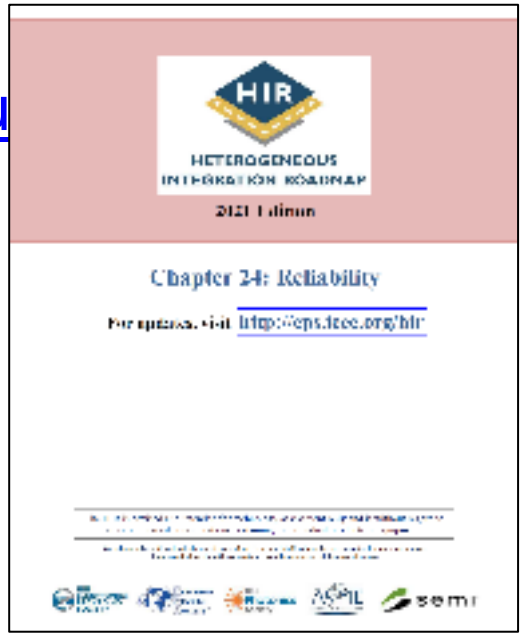
HETEROGENEOUS INTEGRATION ROADMAP

HIR Reliability TWG

Abhijit Dasgupta, Univ of Maryland
Richard Rao, Marvell Technology
Shubhada Sahasrabudhe, Intel

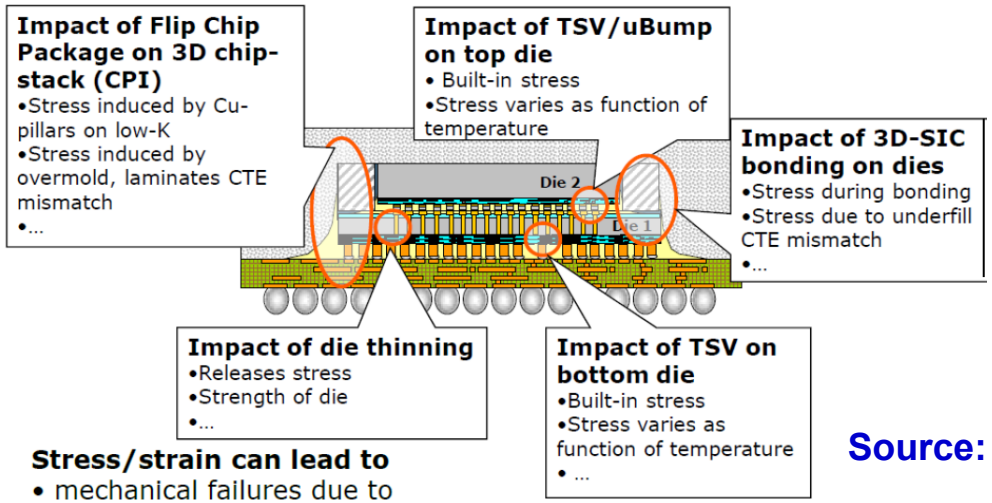
Acknowledgement to Current Members of HIR Reliability TWG

1. Abhijit Dasgupta, Univ of Maryland; dasgupta@umd.edu
2. Richard Rao, Marvell; richardrao@marvell.com
3. Shubhada Sahasrabudhe, Intel; shubhada.h.sahasrabudhe@intel.com
4. Willem D. van Driel; Signify; willem.van.driel@signify.com
5. Przemyslaw J. Gromala; Bosch; PrzemyslawJakub.Gromala@de.bosch.com
6. Hualiang Shi; Lyft; hualiang.shi@gmail.com
7. Albert Wang; Univ of California Riverside, aw@ece.ucr.edu
8. Pradeep Lall; Auburn University; lallpra@auburn.edu
9. Bo Ericsson, Ericsson, bo.e.eriksson@ericsson.com
10. Siva Shivashankar, Google, rsivasankar@google.com
11. Christo Bojkov, Christo.Bojkov@qorvo.com
12. Patrick McCluskey, UMD-CALCE, mcclupa@umd.edu



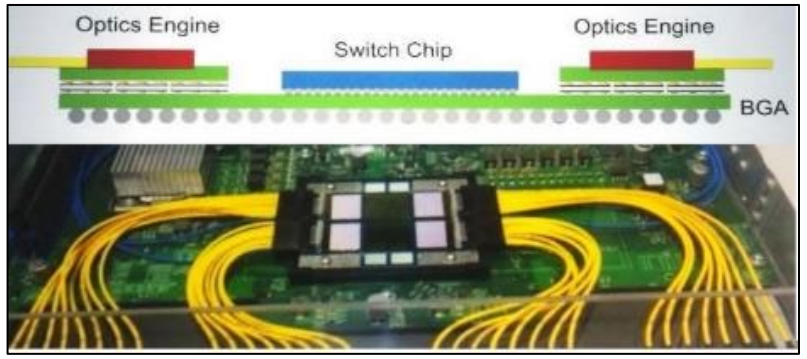
HI systems reliability failure modes/mechanisms

HETEROGENEOUS INTEGRATION ROADMAP



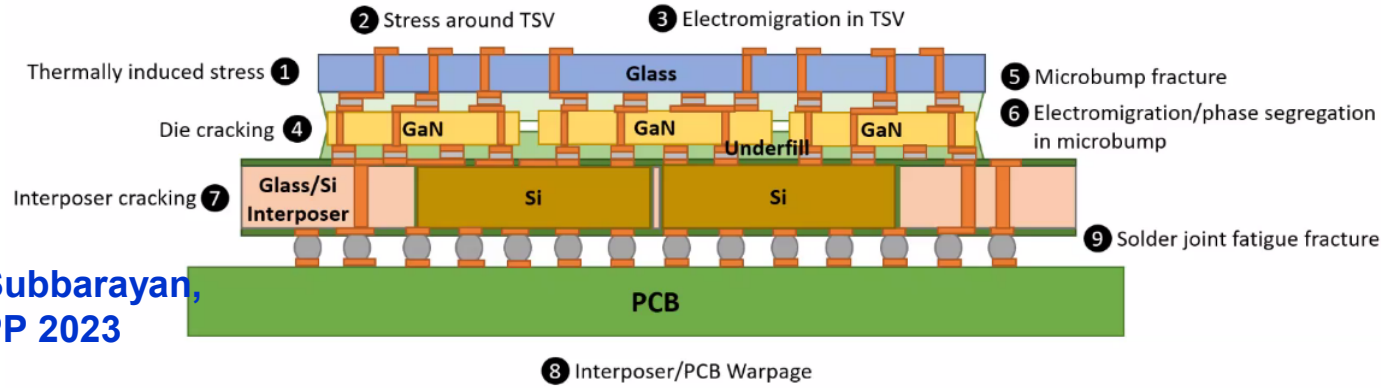
Stress/strain can lead to
- mechanical failures due to delamination, peel, fatigue, …
- electrical impact due to parameter shifts, increased variability, EM,…

Source: IMEC

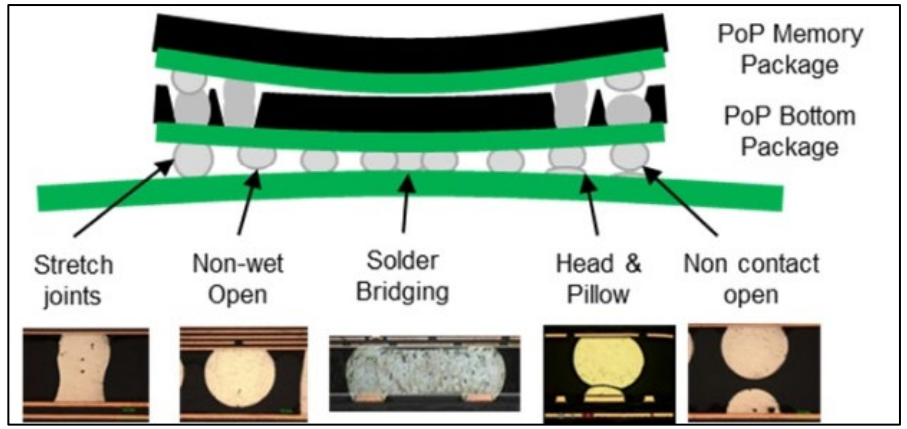


Photonic switching devices/SIP concepts

Multi-scale



Source: Subbarayan, IEEE REPP 2023



Package on package warpage induced defects and failures

1 Intrinsic Stress/Deformation
2 Interfacial Fracture
3 Phase Evolution

Driving forces are electrical, thermal, mechanical, and chemical!

Multi-physics

IEEE
IEEE photonics Society
semi
IEEE ELECTRONICS PACKAGING SOCIETY
ASME
ELECTRON DEVICES SOCIETY

Modes/Mechanisms/Models for degradation & failure

HETEROGENEOUS INTEGRATION ROADMAP

Electrical Thermal Moisture Thermo-mechanical Mechanical DfR Methods MfR Methods

Multiphysics

Multiscale

Devices

Interconnects

Packaging/ System

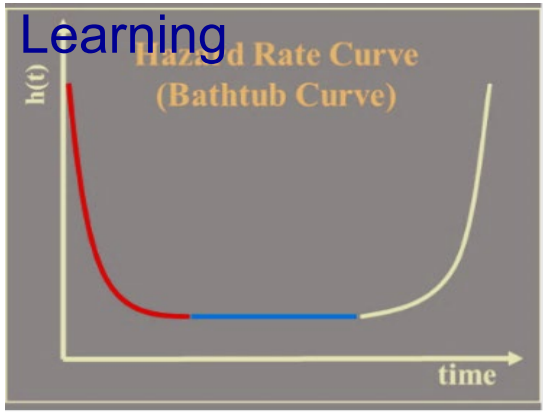
Module/System

Multiscale Integration	Multi Physics	Electrical Stress		SI/PI (Electrical Performance)	Thermal Analysis	Moisture		Thermal Mechanical Stress		Mechanical Stress		Thermal Interaction with SI/PI	Stress Interaction with SI/PI	Simulation/Modeling and Co-Design Flows		Manufacturing Variability	Material Property and Variability
		Failure Modes	Failure Mechanism and Reliability Models			Failure Modes	Failure Mechanism and Reliability Models	Failure Modes	Failure Mechanism and Reliability Models	Failure Modes	Failure Mechanism and Reliability Models			Failure Modes	EDA Flows	PDK/ADK	
Transistor	FinFET and GAA	Leakage current, ripple currents, unstable performance and ESD	N/PBTI models with recovery; HCI model; TDDB Weibull model; Oxide & junction breakdown model	Transistor SPICE	FinFET SHE	No known failures	None	FinFET SHE channel stress; µBump/C4 bump/TSV; system level stresses	FinFET SHE Models; CPI Model; Piezo-electrical models	No known failures	None	SHE effect on SPICE parameters	Influence of SI stress on SPICE parameters	Effects of degradation mechanisms and process variabilities on electrical functionality	Cadence; Relxpert; Mentor Graphics	Integrate of degradation models into Device SPICE Model		
Interconnects	MEOL/BEOL Metal/Via /ELK	Electromigration; Inter Layer Dielectric ELK Breakdown; MEOL Oxide Breakdown; EOS	Electromigration model; Dielectric breakdown model	Extraction of RLC Model	Joule Heating simulation; SHE effects on MEOL/BEOL	Pad and underline metal corrosion; Cu/ELK delamination 3. Cu loss/diffusion	Electrochemical corrosion; Interface degradation due to moisture absorption; Barrier metal oxidation	SHE failure in Cu/ELK, MEOL, BEOL, µBump, TSV; RDL failures from package stress, Cu fatigue; LowK/ELK layer cracking & delamination	Creep induced voiding; CTE mismatch; SHE induced localized thermal cycling	LowK/ELK layer cracking & delamination	Fatige by bending	Joule/SHE temp effects on RLC	Effect of Cu/ELK stress on RLC	CPI induced Cu/ELK cracking; JHE/SHE stresses; stress from bumps/TSV/RDL & Packaging	Ansys Mentor	Package material thermal/mechanical properties; Die metal stack and thermal/mech properties; µBump/C4 bump/TSV thermal mechanical properties; Cu/ELK fracture criteria; Void initiation and propagation criteria; Interconnect fatigue/creep model; Package interface fracture criteria; Moisture diffusion and vapor pressure model; IMC thermal/mech/electrical properties; Photonics optical properties		
	FBEOL RDL/Dielectric	RDL/UBM Electromigration	Electromigration	Extraction of RDL RLC Model	BEOL Joule/SHE effect on RDL temperature	Cu dedrite	Electro-chemical corrosion	RDL cracking	µbump/TSV/ Package/ Board effects on RDL stress			Effect of RDL temp on electrical model	Effect of RDL stress on electrical model	CPI/CBPI induced failures: RDL cracking & delamination	Effect of temp and stress on RDL EM			
	Au/Cu Wirebonding	Electromigration				IMC Corrosion		Bond wire fatigue		Cu/ELK cracking	Bonding force models							
	µBump/C4 Bump/UBM	Electromigration induced voids	Black's model; Multiphysics EM model including elctron, thermal gradient, stress gradient and atomic diffusion	µbump electrical model	Die Internal Joule/SHE temp effect & external temp effect on bump temperature	UBM delamination	Galvanic effect (electro-chemical reaction)	Bump joint cracking; Under Bump ELK cracking; Under pad cracking in substate	CTE mismatch induced stress; Fatigue	Tensile stress causes bump peel; cracks at µbump; UBM and interface	Fracture/fatigue from shock, drop, impact, Vibr; e.g. in die attach, dielectric layer, inter-poser, UBM, solder joints	Effect of temp on bump electrical model	Effect of bump stress on electrical model	Multi Physics Bump EM - local current, temp, temp gradient and stress effect on µbump EM	Bump fatigue: effect of local temp & stress on fatigue life			
	TSV/Interposer/ EMIB	Electromigration; Barrier Dielectric breakdown	Black's model; Multiphysics EM model including elctron, thermal gradient, stress gradient and atomic diffusion	TSV electrical model	Internal Joule/SHE temp effect on the TSV temp; External temp effect on TSV temp.			Cu pumping/TSV pop up	Cu extrsion due to CTE mismatch with Si; plastic rachetting at high temp			Effect of TSV temp on electrical model	Effect of TSV stress on electrical model	TSV EM response to local current, temp field and stress; TSV Pop out and effects on TSV/Si delaminaton	Barrier breakdown - How does voltage/current, temp and stress affect TSV barrier BD?			
Packaging /System	Passivation	Passivation cracking	ECS induced cracking			Passivation cracking & delamination; underfill/Mold compound delamination		Passivation cracking	CPI stress in SIN									
	Underfill					Underfill to die/substrate delamination; underfill swelling	Moisture degradation in underfill & at interfaces	Bump joint cracking	Solder joint fracture and fatigue due to underfill expansion									
	High Density Substrate	Metal trace electromigration		Package Substrate RLC model extraction	Co-thermal sim from die to package	Metal trace corrosion		Metal trace/via cracking				Thermal - electrical perfromance interactions	Mechanical-electrical performance interactions	Cu trace EM - effect of local current, temp and stress	Thermal & mechanical effect on Cu trace/via cracking			
	Wafer Level Package							Warpage										
	Fanout Package							Warpage										
	2.x/2.5D Interposer Package (CoWoS and EMIB, etc)							Warpage; Embedded die delamination from substrate & sidewall; µvia & µbump cracking & delamination; Solder/TIM delamination										
	3D Package (Foveros, etc)			Mold compound pop-corn; Anisotropic conductive adhesive cracks		Mold compound pop-corning		FinFET Ion shift (due to TSV/Si CTE mismatch, µBump stress, shrinkage of underfill & EMC); TSV effects on BTI/HCI; BEOL cracking; Cu pillar joint failure; Mold compound pop-corn; conductive adhesive cracking										
	Chiplet/KGD	ESD						Die edge cracking; Under bump ELK cracking										
Module/ System	Printed Circuit Board Assembly	Leakage current and shorts from Conductive filament formation	electro-chemical metal migration	PCB Board electrical model	\Co-thermal sim from die to package to system	leakage current and shorts from loss of surface insulation resistance & conductive filament formation	moisture ingress, leading to fiber-matrix debonding, and electro-chemical metal migration	Solder joint cracking ; Cracking of PTH plating; PCB delamination; trace cracking; Warpage	thermomechanical fatigue of trace and solder, IMC fracture; CTE mismatches between: component / PWB, metallization/ dielectrics	Solder joint cracking; pad cratering	Stress exceeds the material and interface strength	Effects of PCB temp and corrosion on electrical model?	Effects of PCB stress on electrical model?	Board level Solder Joint Reliability	ANSYS Mechanical	PCB thermal/ mechanical properties; Solder joint fatigue/creep model; Solder joint dynamic/ properties		

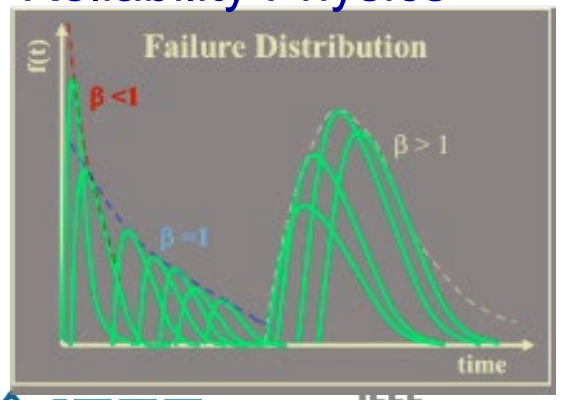
Reliable HI systems: Approach

HETEROGENEOUS INTEGRATION ROADMAP

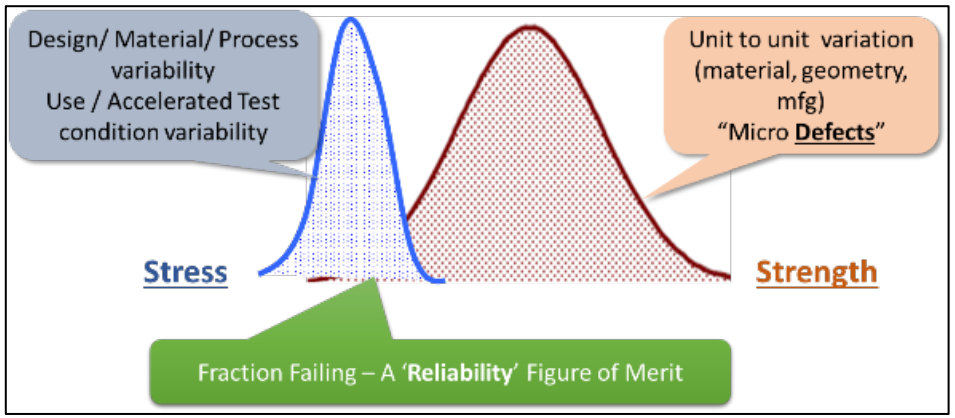
Top down:
Artificial Intelligence and Machine Learning



Bottom up:
Reliability Physics



Reliability Assurance Activities



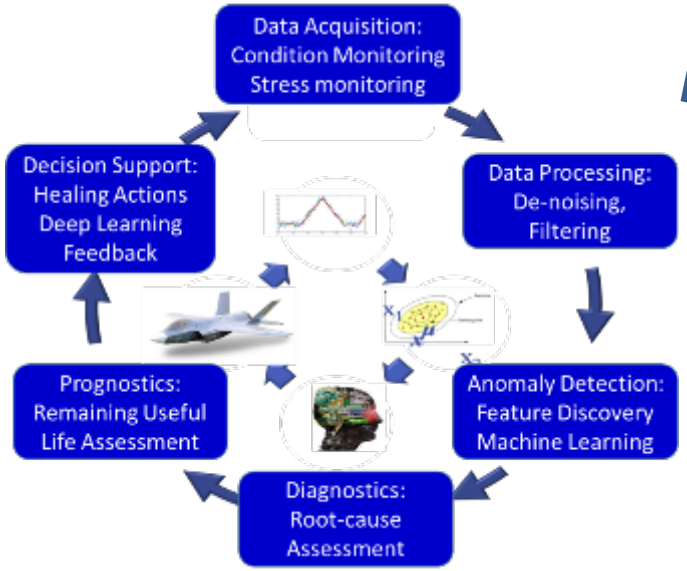
Multi-physics/multi-scale HI systems require holistic cradle-to-grave reliability methodology

- Reliability Targets
- Life Cycle Conditions
- Design for Reliability
- Manufacturing for Reliability
- Knowledge based Testing for Qualification
- Product Health Management
- Supply chain Integration

IEEE · IEEE photonics Society · semi · IEEE ELECTRONICS PACKAGING SOCIETY · ASME · ELECTRON DEVICES SOCIETY

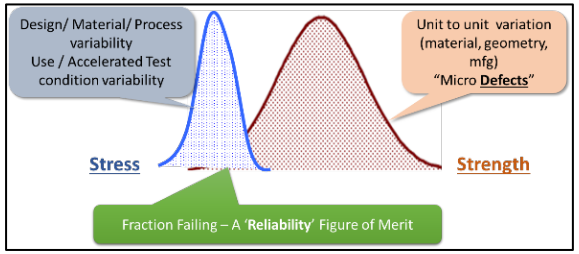
HI System reliability

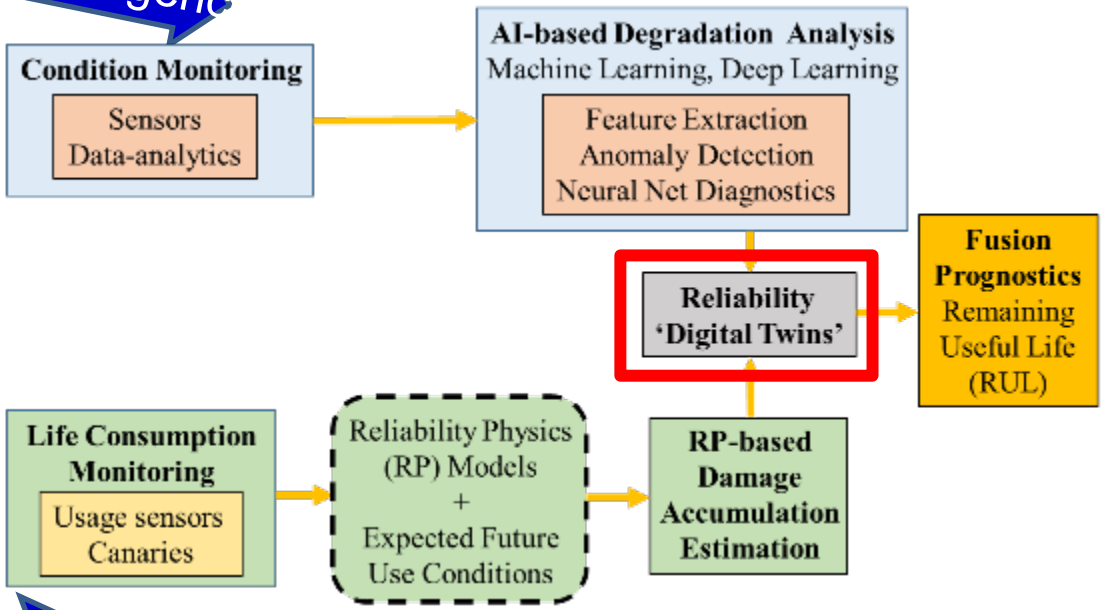
Prognostics and Health Management



Fusion of bottom-up physics and top-down AI approaches

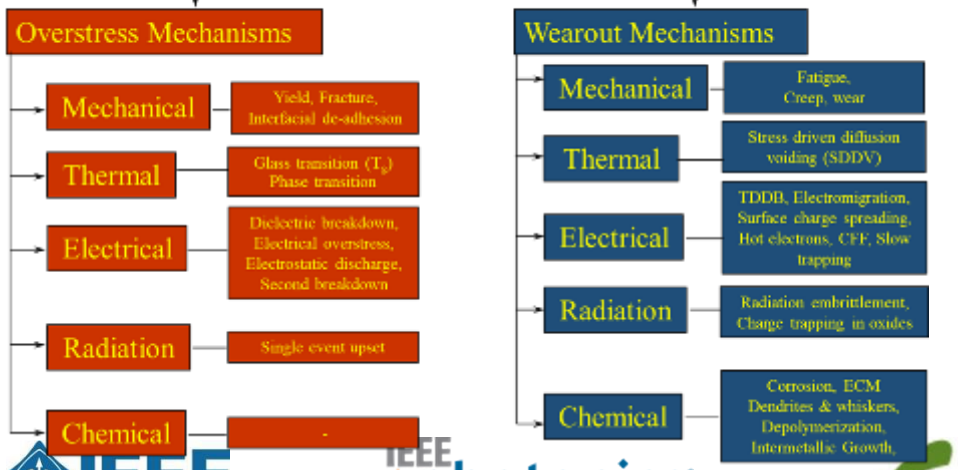
Machine Learning & Artificial Intelligenc





Reliability Physics

Degradation and Failure Mechanisms



Reliability challenges in HI systems: Future outlook

HIR HETEROGENEOUS

Digital Twins

		Reliability Targets	Life Cycle Conditions	Design for Reliability	Manufacturing for Reliability	Qualification for Reliability	Sustainment for Reliability	Supply Chain
Applications	Mobile							
	IoT							
	Medical, Health and wearables							
	Automotive							
	HPC & Data Centers							
	Aerospace and Defense							
Package Integration	WLP (FO/FI)							
	2.5D and 3D integration							
	Wafer Singulation and Thinning							
	Chip-package interactions (CPI)							
	Interconnects (TSV8s, µbumps, wirebonds, Flip Chip solder joints)							
	Substrates/Interposers							
	Board Assembly							
	SOC/SIP/SOP[9] formats							
Technologies	Microelectronics > 10 nm							
	Microelectronics <10 nm							
	Photonics & optics							
	MEMS and sensors							
	Power electronics							
	Energy souces (Batteries/PV[6]/FC[7])							
	RF/Analog Devices							

1-5 Years:

Multi-physics fusion approaches for reliability assurance

- Bottom-up *Reliability Physics* based approaches, tools, infrastructure
- Top-down *Machine Learning & AI* based approaches, tools, infrastructu

5-10 Years:

Fusion approaches for co-design (based on 'digital twins') and life-cycle PHM of next-gen robust HI systems

- Fault-tolerant systems
- Resilient systems

10-15 Years:

Fusion approaches for intelligent, adaptive, reconfigurable products with integrated autonomous life-cycle management capability

- Intelligent, self-cognizant systems
- Self-healing systems

IEEE IEEE photonics Society semi IEEE ELECTRONICS PACKAGING SOCIETY ASME ELECTRON DEVICES SOCIETY

HETEROGENEOUS INTEGRATION ROADMAP

Thank You

IEEE

IEEE photonics Society

semi

IEEE ELECTRONICS PACKAGING SOCIETY

ASME

ELECTRON DEVICES SOCIETY