Challenges and Opportunities in Manufacturing 3-Dimensional Heterogeneously Integrated (3DHI) Microsystems

Dr. Carl McCants, DARPA Special Assistant – Microelectronics Policy

Briefing Prepared for Heterogeneous Integration Roadmap Meeting

February 22, 2024

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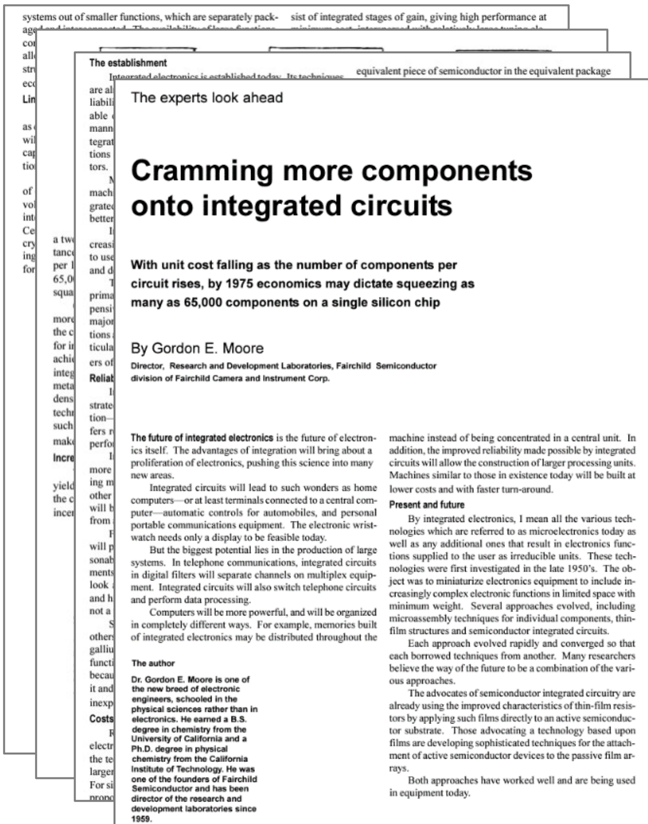
Disaggregation*



The experts look ahead

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas.

Integrated circuits will lead to such wonders as home computers—or at least terminals connected to a central computer—automatic controls for automobiles, and personal portable communications equipment. The electronic wristwatch needs only a display to be feasible today.

But the biggest potential lies in the production of large systems. In telephone communications, integrated circuits in digital filters will separate channels on multiplex equipment. Integrated circuits will also switch telephone circuits and perform data processing.

Computers will be more powerful, and will be organized in completely different ways. For example, memories built of integrated electronics may be distributed throughout the machine instead of being concentrated in a central unit. In addition, the improved reliability made possible by integrated circuits will allow the construction of larger processing units. Machines similar to those in existence today will be built at lower costs and with faster turn-around.

The author

Dr. Gordon E. Moore is one of the new breed of electronic engineers, schooled in the physical sciences rather than in electronics. He earned a B.S. degree in chemistry from the University of California and a Ph.D. degree in physical chemistry from the California Institute of Technology. He was one of the founders of Fairchild Semiconductor and has been director of the research and development laboratories since 1959.

Present and future

By integrated electronics, I mean all the various technologies which are referred to as microelectronics today as well as any additional ones that result in electronics functions supplied to the user as irreducible units. These technologies were first investigated in the late 1950's. The object was to miniaturize electronics equipment to include increasingly complex electronic functions in limited space with minimum weight. Several approaches evolved, including microassembly techniques for individual components, thin-film structures and semiconductor integrated circuits.

Each approach evolved rapidly and converged so that each borrowed techniques from another. Many researchers believe the way of the future to be a combination of the various approaches.

The advocates of semiconductor integrated circuitry are already using the improved characteristics of thin-film resistors by applying such films directly to an active semiconductor substrate. Those advocating a technology based upon films are developing sophisticated techniques for the attachment of active semiconductor devices to the passive film arrays.

Both approaches have worked well and are being used in equipment today.

Source: Electronics, Volume 38, Number 8, April 19, 1965

"It may prove more economical to **build large systems out of smaller functions, which are separately packaged and interconnected**. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically."

– Gordon Moore

*a.k.a.

- *Polylithic*
- *Pseudo-lithic*
- *Chiplet-based*
- *3DHI*

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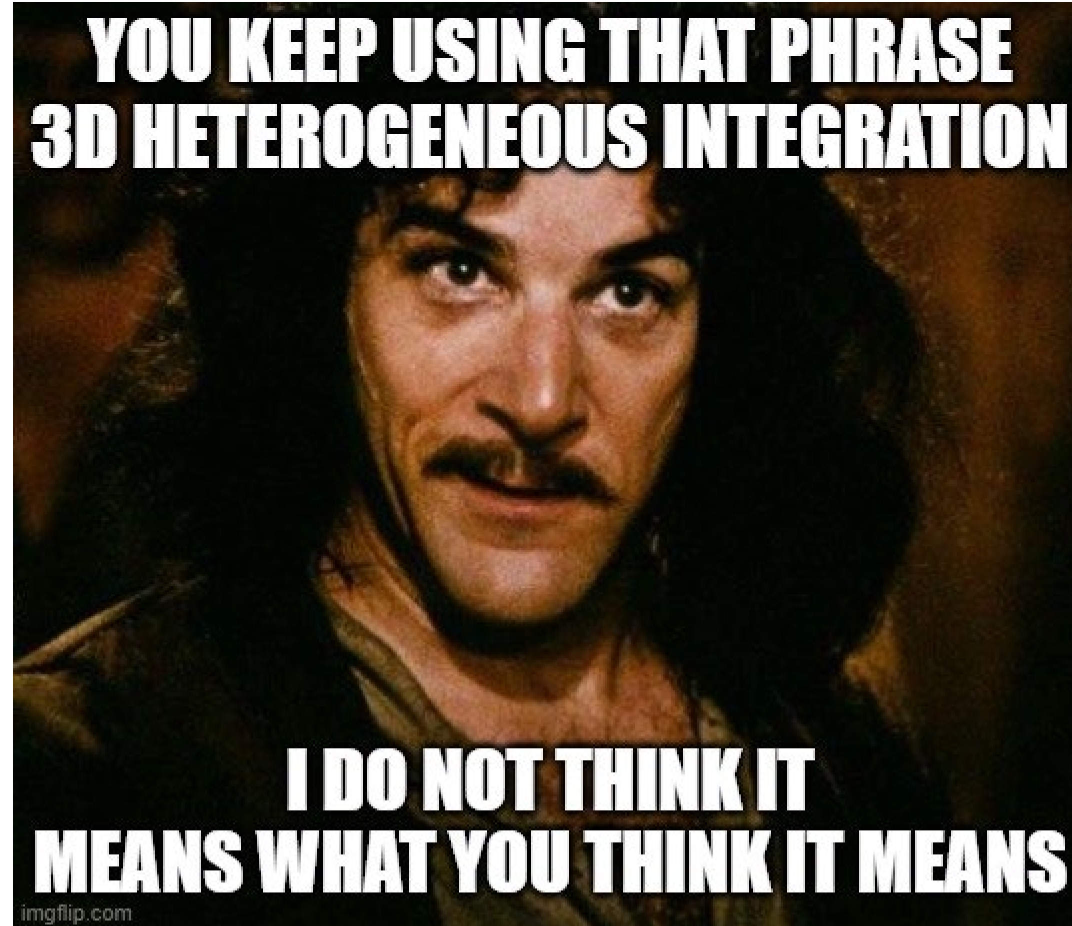
What is 3DHI?



Source: https://imgflip.com/memegenerator/Inigo-Montoya

3DHI: Three-dimensional heterogeneous integration

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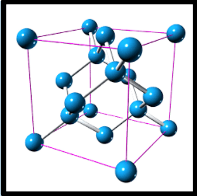
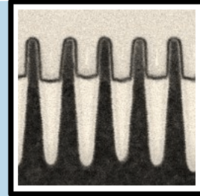
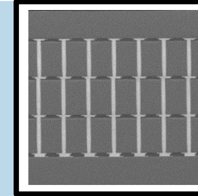
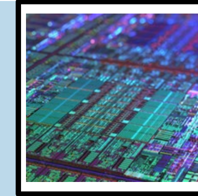
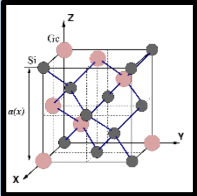
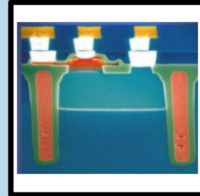
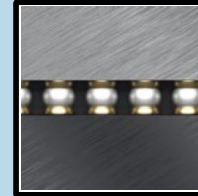
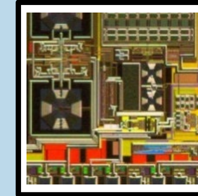
Heterogeneous Integration (HI) – Traditional Focus

Traditional Focus

Materials		Devices		Process		Function	
	Silicon		MOSFET, FinFET, GAAFET		Bump, μ-Bump, TSV, Hybrid		Logic, Memory
	Silicon germanium		Bi-CMOS, HBTs		Bump, μ-Bump, TSV, Hybrid		Analog, Mixed-Signal, RF

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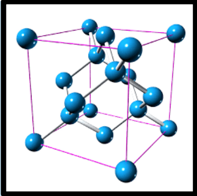
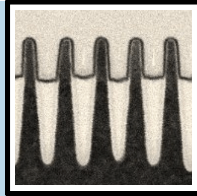
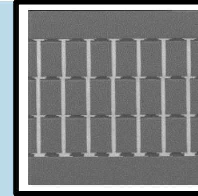
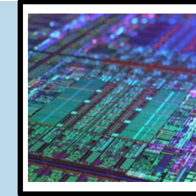
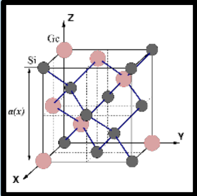
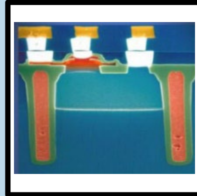
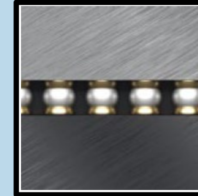
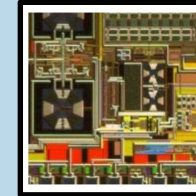
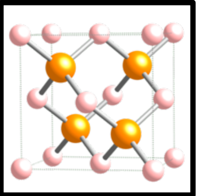
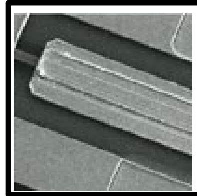
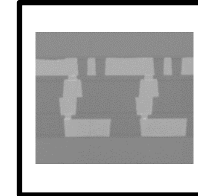
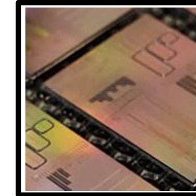
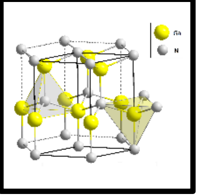
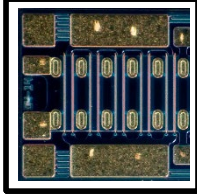
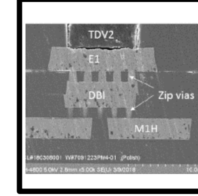
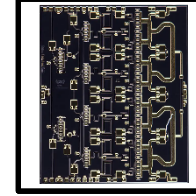
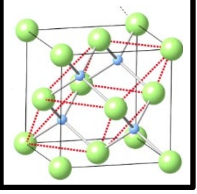
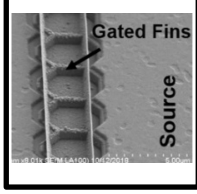
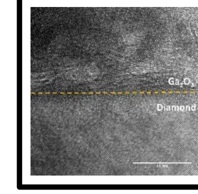
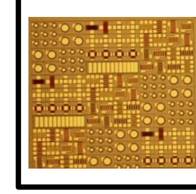
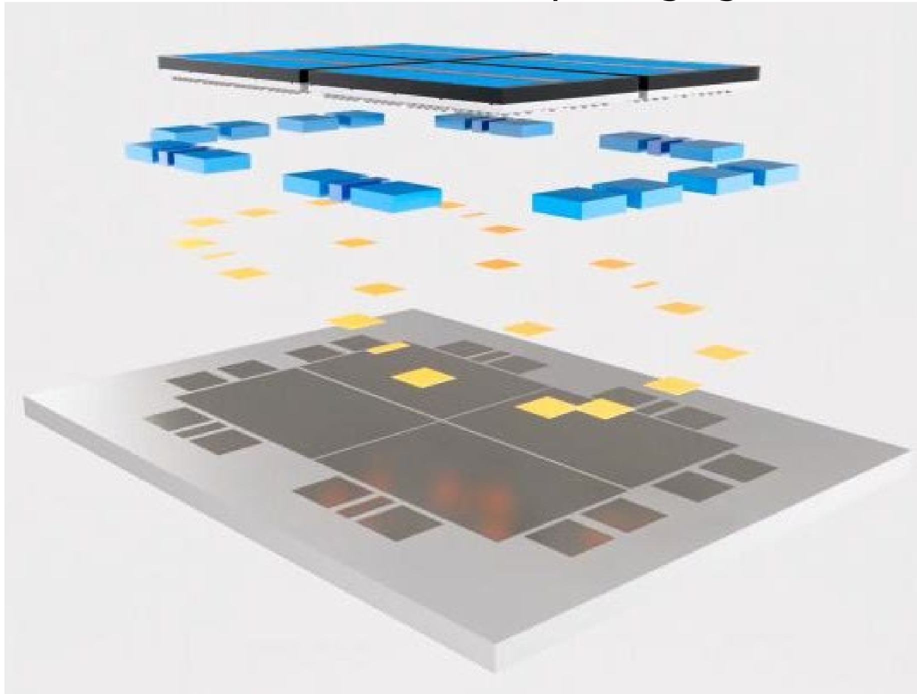
Heterogeneous Integration (HI) – DARPA Definition

	Materials		Devices		Process		Function	
Traditional Focus		Silicon		MOSFET, FinFET, GAAFET		Bump, μ-Bump, TSV, Hybrid		Logic, Memory
Traditional Focus		Silicon germanium		Bi-CMOS, HBTs		Bump, μ-Bump, TSV, Hybrid		Analog, Mixed-Signal, RF
Emerging Opportunities		III-V, II-VI (GaAs, InP, HgCdTe)		Laser, LED, Detector		Bump, μ-Bump, TSV, Hybrid		Photonics, RF
Emerging Opportunities		Wide bandgap (GaN, SiC)		HEMT, MESFET, JFET		Bump, μ-Bump, TSV, Hybrid		Photonics, RF, Power
Emerging Opportunities		Ultrawide bandgap (AlGaN, Diamond)		HEMT, MESFET, JFET		Bump, μ-Bump, TSV, Hybrid		Photonics, Power

What is 3DHI?

3D

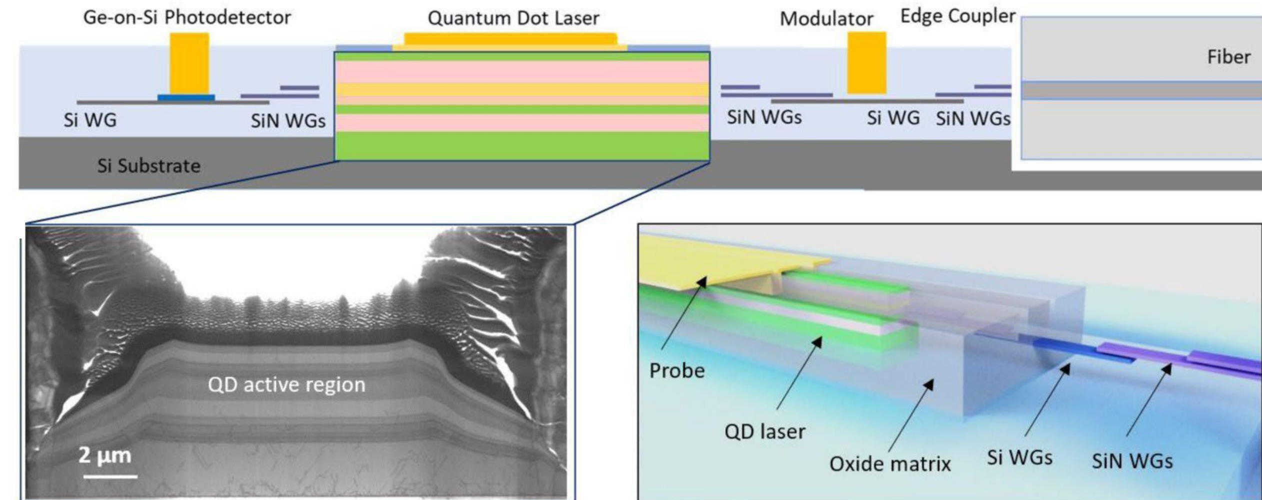
Intel 3D stacked packaging



Source: Intel

HI

High-performance lasers on a 300 mm silicon photonics wafer



Source: RF-SUNY, IQE, UCSB

3DHI: Three-dimensional heterogeneous integration
Ge: Germanium
QD: Quantum dot

Si: Silicon
SiN: Silicon nitride
WGs: Waveguides

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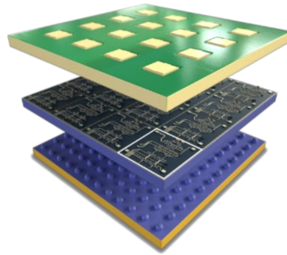
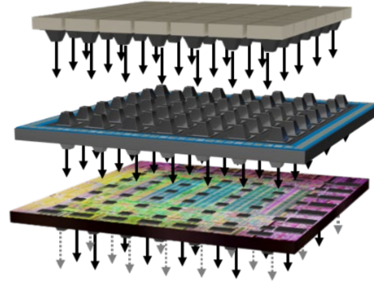
3DHI is across our current programs

A-PhI

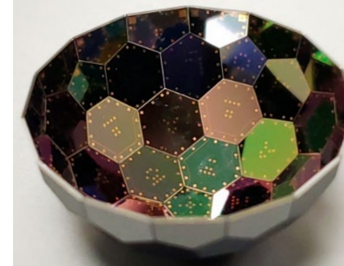
ELGAR



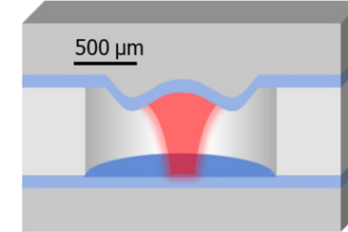
FENCE



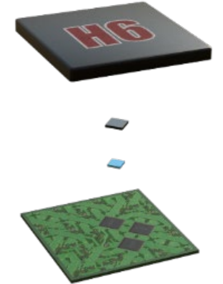
FOCII



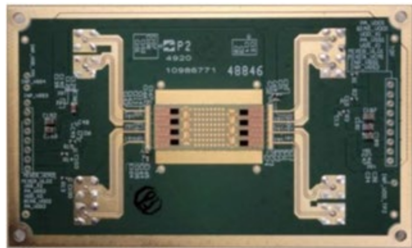
GRYPHON



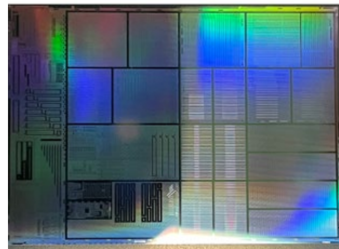
H6



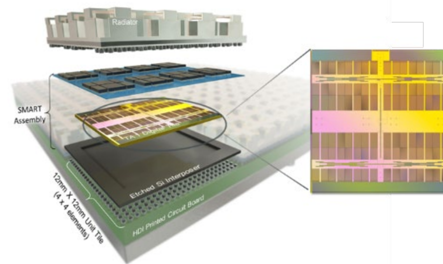
JUMP / JUMP 2.0



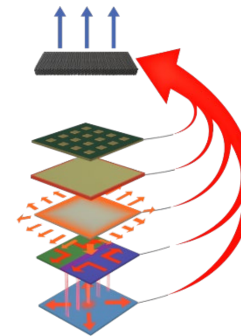
LUMOS



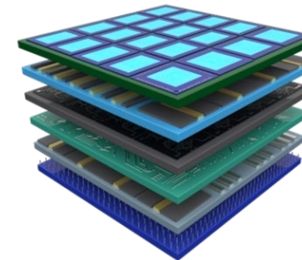
MIDAS



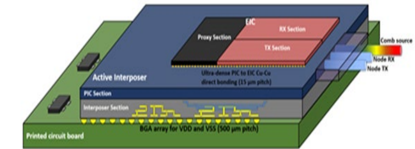
Minitherms3D



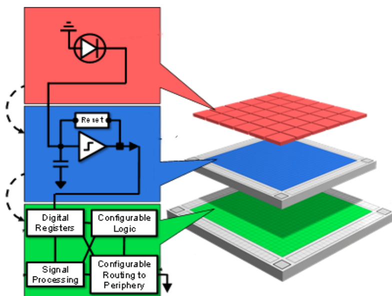
NGMM



PIPES



ReImagine



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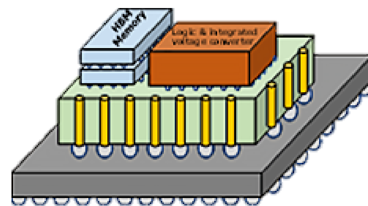
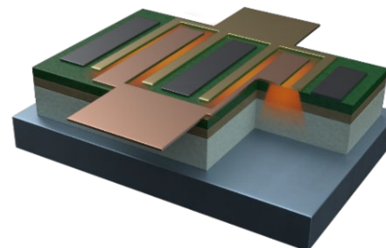
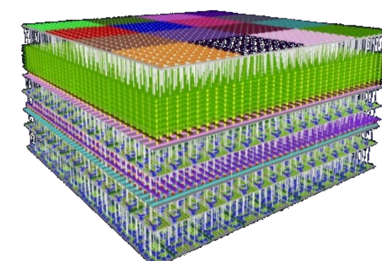


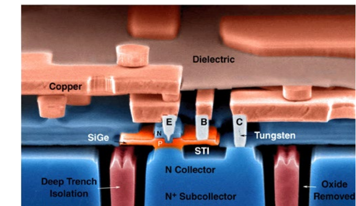
THREADS



3DSoC



T-MUSIC



3DHI: Three-dimensional heterogeneous integration

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ERI 2.0: A long-term vision for advanced microelectronics manufacturing

- OSD R&E
- Dept of Commerce
- DARPA

Integration Type: 3DHI, 3D, 2.5D, 2D

Performance: 100x, 30x, 3x, 1x

ERI 2.0

NGMM ⟷ BUILD, COMPOSE, SECURE, TALK, COMPUTE, DECIDE, HARDEN

3DHI Pilot Line

3DHI Manufacturing Science

SHIP + RESHAPE

NSTC + NAPMP

Domestic Fabrication and Packaging

ME Commons

Emerging Prototyping, Workforce Development

RAMP-C

Emerging Current Technology

SHIP: State-of-the-art Heterogeneous Integrated Packaging
RESHAPE: Reshore Ecosystem for Secure Heterogeneous Advanced Packaging Electronics
RAMP-C: Rapid Assured Microelectronics Prototypes – Commercial
NSTC: National Semiconductor Technology Center
NAPMP: National Advanced Packaging Manufacturing Program
ME Commons: Microelectronics Commons
NGMM: Next-Generation Microelectronics Manufacturing
ERI: Electronics Resurgence Initiative

Today — **Time to Technology Implementation** — Far-term

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NGMM encompasses a multi-threaded approach for developing a 3DHI capability

Phase 1	Phase 2	End Goal
Establish Baseline Process	Qualify / Operationalize Center	

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NGMM Research & Development

Process Modules

- Wafer post-processing
- Bonding layer fabrication
- Assembly
- Technical challenges
  - Dense, scaled interconnects
  - Standards for bonding layer interfaces
  - Thermal management
  - Diverse materials, including sub-200 mm wafers

Test Vehicles

- Validate microsystem performance, including
  - RF
  - Optical
  - Power
  - Thermal
  - Mechanical
- Smaller sub-components of larger micro-system
- Emphasized in Phase 1 for meeting interface metrics

3D-ADK

- Model and rule support required for EDA tools adapting to 3DHI methodology and requirements
- 3D-ADK includes:
  - Process design rules
  - Assembly design rules
  - Stack specifications, including material properties and dimensions
  - Device and interconnect models

EDA

- Adapt conventional capabilities to 3DHI microsystems
- Broad access
  - Support open data formats
  - Provide modular architecture to support third-party simulation tools
- By Phase 2, develop digital twin of a placed and routed 3DHI circuit to model circuit behavior

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CHIPS National Advanced Packaging & Manufacturing Program Vision

Technology investments are in green. Ecosystem investments are in blue.
The piloting facility, in red, will provide opportunities to validate new technologies for transition to U.S. manufacturing

Source: https://www.nist.gov/system/files/documents/2023/11/19/NAPMP-Vision-Paper-20231120.pdf

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Challenge – the Domestic Cost Differential

WWHA – What Would Heilmeier Ask?

- H1 – What are you trying to do?
- H2 – How is it done today and who does it? What are the limitations to the present approaches?
  - What is “it”?
  - How is “it” done today (name and concise description)?
  - What is the definition, description, and rationale for each technical challenge to fully describe the H2 limitations?
- H3 – What is new about our approach and why do we think it will succeed?
  - What is the name, description, and novelty of the technical approach?
  - What are the insights, rationale, and supporting evidence that the technical approach will overcome the technical challenge?
- H4 – If we succeed, what difference will it make?
  - What is the mission capability that will be enabled?
  - What is the description and CONOPS*, significance, and relevance to the specific mission capability?
- H5 – How long do we think it will take? What are our mid-term/final exams? How much will it cost?

*CONOPS – Concept of Operations

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Challenge – the Domestic Cost Differential

WWHA – What Would Heilmeier Ask?

- H1 – What are you trying to do? Bring the costs for domestic packaging to $\leq$1.1X overseas packaging costs
- H2 – How is it done today and who does it? What are the limitations to the present approaches?
  - What is "it"?
  - How is "it" done today (name and concise description)?
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