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Abstract should include original and previously unpublished, non-confidential and non-commercial information on new developments, technology and knowledge in the areas including, but not limited to those given below.

- Advanced Packaging – 2D, 2.5D, 3.0D, Chiplets, WLCSP, FOWLP, FOPLP & HI
- Thermal/Mechanical/Electrical Simulation & Characterization
- Material & Processing
- Emerging Packaging – Opto, Medical, Nano Technology, Wearable Electronics
- Interconnections Technologies – TSV, μ-bump, hybrid bond, FC and embedded
- LED, MEMS, NEMS & Sensor Packaging & IoT
- IC Testing Technology
- Surface Mount Technology
- Quality, Reliability & Failure Analysis
- High-Speed, Wireless & Components
KEYNOTE SPEAKERS:

Prof. Chris Bailey
Director of Computational Mechanics and Reliability Group
University of Greenwich

Mr Chew CH
Senior Director
OnSemi

Mr Terrence Tan
Senior Principal Engineer, Manufacturing and Product Engineering
Intel

Dr. Veer Dhandapani
Senior Director of Product Development
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Mr. Laurent Herard
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